

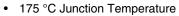


N-Channel 150 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	$V_{DS}(V)$ $R_{DS(on)}(\Omega)$			
150	0.095 at V _{GS} = 10 V	15		
	0.100 at V _{GS} = 6 V	15		

FEATURES

• TrenchFET® Power MOSFETS



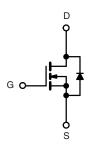


100 % R_g Tested

Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

· Primary Side Switch



N-Channel MOSFET

TO-252	
G D S	Drain Connected to Tab
Top View	

Ordering Information: SUD15N15-95-E3 (Lead (Pb) free)

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)					
Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	150	V	
Gate-Source Voltage	V _{GS}	± 20	V		
Out in the Darie Out of T	T _C = 25 °C	1	15		
Continuous Drain Current (T _J = 175 °C) ^b	T _C = 125 °C	I _D	8.7		
Pulsed Drain Current	I _{DM}	25	Α		
Continuous Source Current (Diode Conduction)	I _S	15			
Avalanche Current	I _{AR}	15			
Repetitive Avalanche Energy (Duty Cycle ≤ 1 %)	L = 0.1 mH	E _{AR}	11.3	mJ	
Mantagara Barana Biratian	T _C = 25 °C	Pn	62 ^b	W	
Maximum Power Dissipation	T _A = 25 °C	'D	2.7 ^a] vv	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 175	°C	

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Junction-to-Ambient ^a	t ≤ 10 s	- R _{thJA}	16	20	°C/W	
Junction-to-Ambient*	Steady State		45	55		
Junction-to-Case		R _{thJC}	2	2.4		

- a. Surface mounted on 1" x 1" FR4 board.
- b. See SOA curve for voltage derating.

SUD15N15-95

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Parameter	Symbol	Test Conditions		Typ. ^a	Max.	Unit	
Static					<u>l</u>		
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	150			V	
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$				V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
		V _{DS} = 120 V, V _{GS} = 0 V			1		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 120 V, V _{GS} = 0 V, T _J = 125 °C			50	μΑ	
		V _{DS} = 120 V, V _{GS} = 0 V, T _J = 175 °C			250		
On-State Drain Current ^b	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	25			Α	
		V _{GS} = 10 V, I _D = 15 A		0.077	0.095		
	В	V _{GS} = 10 V, I _D = 15 A, T _J = 125 °C			0.190	.250	
Drain-Source On-State Resistance ^b	R _{DS(on)}	V _{GS} = 10 V, I _D = 15 A, T _J = 175 °C			0.250		
		V _{GS} = 6 V, I _D = 10 A		0.081	0.100		
Forward Transconductance ^b	9 _{fs}	V _{DS} = 15 V, I _D = 15 A		25		S	
Dynamic ^a							
Input Capacitance	C _{iss}			900		pF	
Output Capacitance	C _{oss}	$V_{GS} = 0 \text{ V}, V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$		115			
Reverse Transfer Capacitance	C _{rss}			70			
Total Gate Charge ^c	Q_g			20	25		
Gate-Source Charge ^c	Q_{gs}	$V_{DS} = 75 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 15 \text{ A}$		5.5		nC	
Gate-Drain Charge ^c	Q_{gd}			7			
Gate Resistance	R _g		1		3.2	Ω	
Turn-On Delay Time ^c	t _{d(on)}			8	12		
Rise Time ^c	t _r	$V_{DD} = 75 \text{ V}, R_L = 5 \Omega$		35	55	no	
Turn-Off Delay Time ^c	t _{d(off)}	$I_D \cong 15 \text{ A}, V_{GEN} = 10 \text{ V}, R_G = 2.5 \Omega$		17	25	ns	
Fall Time ^c	t _f			30	45		
Source-Drain Diode Ratings and Cha	racteristic (T	C = 25 °C)		_			
Pulsed Current	I _{SM}				25	Α	
Diode Forward Voltage ^b	V_{SD}	$I_F = 15 \text{ A}, V_{GS} = 0 \text{ V}$		0.9	1.5	V	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 15 A, dI/dt = 100 A/μs		55	85	ns	

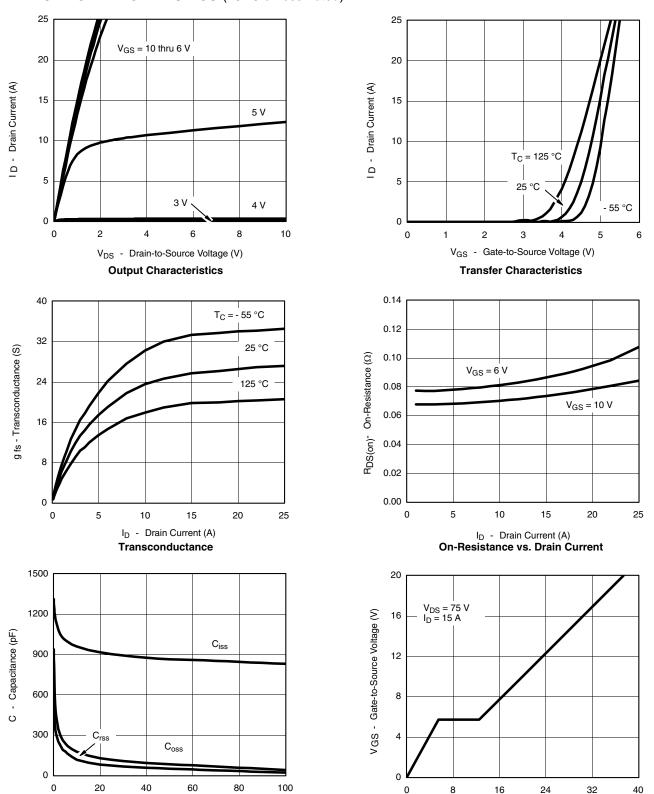
Notes:

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



TYPICAL CHARACTERISTICS (25 °C unless noted)

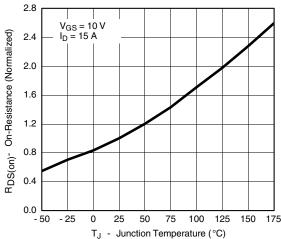


Qg - Total Gate Charge (nC)

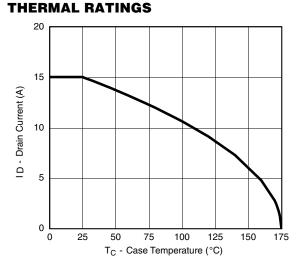
Gate Charge

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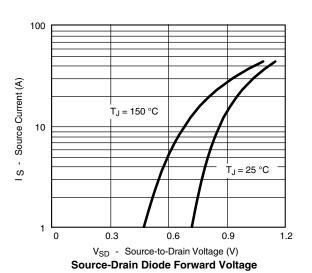
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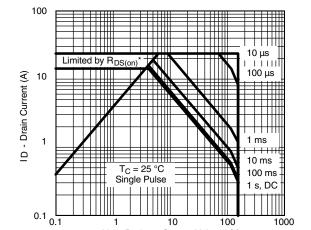


On-Resistance vs. Junction Temperature

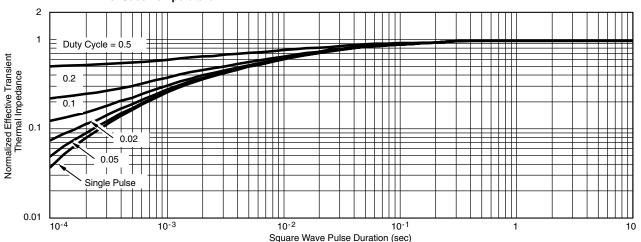


Maximum Avalanche Drain Current vs. Case Temperature





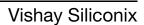
V_{DS} - Drain-to-Source Voltage (V) * V_{GS} > minimum V_{GS} at which R_{DS(on)} is specified Safe Operating Area



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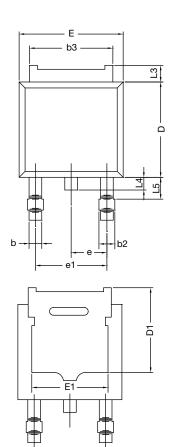
reliability data, see www.vishay.com/ppg?71641.

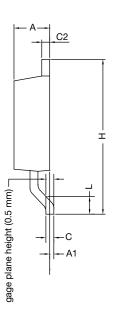
Normalized Thermal Transient Impedance, Junction-to-Case





TO-252AA Case Outline



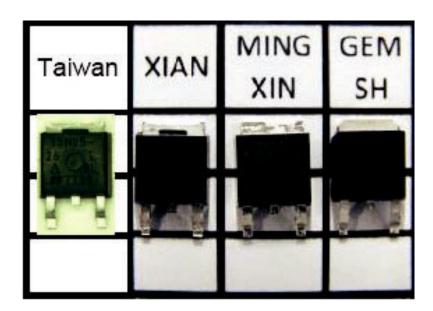


	MILLIMETERS		INC	HES	
DIM.	MIN.	MAX.	MIN.	MAX.	
Α	2.18	2.38	0.086	0.094	
A1	-	0.127	-	0.005	
b	0.64	0.88	0.025	0.035	
b2	0.76	1.14	0.030	0.045	
b3	4.95	5.46	0.195	0.215	
С	0.46	0.61	0.018	0.024	
C2	0.46	0.89	0.018	0.035	
D	5.97	6.22	0.235	0.245	
D1	4.10	-	0.161	-	
Е	6.35	6.73	0.250	0.265	
E1	4.32	-	0.170	-	
Н	9.40	10.41	0.370	0.410	
е	2.28 BSC		0.090 BSC		
e1	4.56 BSC		0.180 BSC		
L	1.40	1.78	0.055	0.070	
L3	0.89	1.27	0.035	0.050	
L4	=	1.02	-	0.040	
L5	1.01	1.52	0.040	0.060	
ECN: T13-0359-Rev. O, 03-Jun-13					

DWG: 5347

Notes

- Dimension L3 is for reference only.
- Xi'an, Mingxin, and GEM SH actual photo.



Revision: 03-Jun-13 Document Number: 71197



RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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Revision: 02-Oct-12 Document Number: 91000