RoHS

COMPLIANT

HALOGEN FREE





N-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY								
		I _D (A) ^a					
V _{DS} (V)	R _{DS(on)} (Ω) ^e	Silicon Limit	Package Limit	Q _g (Typ.)				
20	0.0016 at $V_{GS} = 10 \text{ V}$	220	60	46 nC				
20	0.0025 at $V_{GS} = 4.5 \text{ V}$	117	60	40110				

Package Drawing

www.vishay.com/doc?72945

PolarPAK G S D 2 3 2 4 5 Top View Bottom View

Top surface is connected to pins 1, 5, 6, and 10

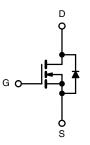
Ordering Information: SiE808DF-T1-E3 (Lead (Pb)-free) SiE808DF-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

- Halogen-free According to IEC 61249-2-21 **Definition**
- TrenchFET® Gen II Power MOSFET
- Ultra Low Thermal Resistance Using Top-Exposed PolarPAK® Package for Double-Sided Cooling
- Leadframe-Based New Encapsulated Package
 - Die Not Exposed
 - Same Layout Regardless of Die Size
- Low Q_{gd}/Q_{gs} Ratio Helps Prevent Shoot-Through 100 % R_g and UIS Tested
- Compliant to RoHS directive 2002/95/EC

APPLICATIONS

- VRM
- DC/DC Conversion: Low-Side
- Synchronous Rectification



N-Channel MOSEFT For Related Documents www.vishay.com/ppg?73739

ABSOLUTE MAXIMUM RATIN	IGS T _A = 25 °C,	unless otherwis	se noted	
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V _{GS}	± 20	v
	T _C = 25 °C		220 (Silicon Limit)	
	10 - 23 0		60 ^a (Package Limit)	
Continuous Drain Current (T _J = 150 °C)	T _C = 70 °C	I _D	60 ^a	
	T _A = 25 °C		45 ^{b, c}	
	T _A = 70 °C		36 ^{b, c}	A
Pulsed Drain Current		I _{DM}	100	
Ocation of Common Design Disable Commont	T _C = 25 °C		60 ^a	
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	4.3 ^{b, c}	
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	35	
Avalanche Energy	L=0.11IIII	E _{AS}	61	mJ
	T _C = 25 °C		125	
Maximum Dawar Dissination	T _C = 70 °C	P _D	80	w
Maximum Power Dissipation	T _A = 25 °C	- FD -	5.2 ^{b, c}	VV
	T _A = 70 °C		3.3 ^{b, c}	
Operating Junction and Storage Temperatur	ating Junction and Storage Temperature Range T _J , T _{stg} - 55 to 150		°C	
Soldering Recommendations (Peak Temperature) ^{d, e}			260	

- a. Package limited is 60 A.
- Surface Mounted on 1" x 1" FR4 board.
- See Solder Profile (www.vishay.com/doc?73257). The PolarPAK is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not requiréd to ensure adequate bottom side solder interconnection.
- e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

SiE808DF

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THERMAL RESISTANCE RATING	as				
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, b}	t ≤ 10 s	R _{thJA}	20	24	
Maximum Junction-to-Case (Drain Top)	Steady State	R _{thJC} (Drain)	0.8	1	°C/W
Maximum Junction-to-Case (Source) ^{a, c}	Sieady State	R _{thJC} (Source)	2.2	2.7	

Notes:

- a. Surface Mounted on 1" x 1" FR4 board.
- b. Maximum under Steady State conditions is 68 $^{\circ}\text{C/W}.$
- c. Measured at source pin (on the side of the package).

Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	20			V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = 250 μA		26.5		m\//9C
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 7.3		mV/°C
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_{D} = 250 \mu A$	1.5	2.3	3	V
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zava Cata Valtaga Drain Current	1	V _{DS} = 20 V, V _{GS} = 0 V			1	μΑ
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			10	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	25			Α
Durin Occurs On Otata Basistana a	D	V _{GS} = 10 V, I _D = 25 A		0.0013	0.0016	0
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 25 \text{ A}$		0.0021	0.0025	Ω
Forward Transconductance ^a	9 _{fs}	$V_{DS} = 10 \text{ V}, I_{D} = 25 \text{ A}$		95		S
Dynamic ^b						
Input Capacitance	C _{iss}			8800		
Output Capacitance	C _{oss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz		1600		pF
Reverse Transfer Capacitance	C _{rss}			600		
Total Gate Charge	Qg	$V_{DS} = 10 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 25 \text{ A}$		102	155	20
				46	70	
Gate-Source Charge	Q _{gs}	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 20 \text{ A}$		26		nC
Gate-Drain Charge	Q_{gd}			8		
Gate Resistance	R_{g}	f = 1 MHz		0.9	1.35	Ω
Turn-On Delay Time	t _{d(on)}			180	270	
Rise Time	t _r	V_{DD} = 10 V, R_L = 1 Ω		215	325	
Turn-Off Delay Time	t _{d(off)}	f = 1 MHz		50	75	
Fall Time	t _f	· ·		15	25	
Turn-On Delay Time	t _{d(on)}			25	40	ns
Rise Time	t _r	$V_{DD} = 10 \text{ V}, R_L = 1 \Omega$		55	85	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		55	85	
Fall Time	t _f	•		10	15	
Drain-Source Body Diode Characteristic	cs		,			
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			60	Δ.
Pulse Diode Forward Current ^a	I _{SM}				100	Α
Body Diode Voltage	V_{SD}	I _S = 10 A		0.8	1.2	V
Body Diode Reverse Recovery Time	t _{rr}			56	85	ns
Body Diode Reverse Recovery Charge	Q _{rr}	1 10 A dl/dt 100 A/vo T 05 00		60	90	nC
Reverse Recovery Fall Time	t _a	$I_F = 10 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$		26	İ	
Reverse Recovery Rise Time	t _b			30		ns

Notes:

- a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

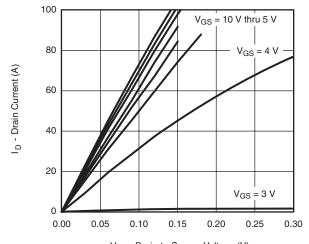


4.0



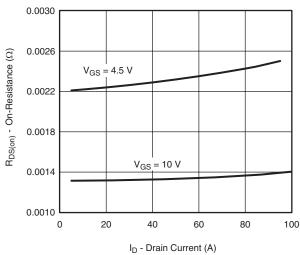


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

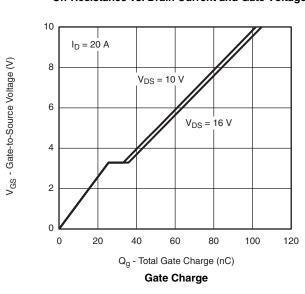


V_{DS} - Drain-to-Source Voltage (V)

Output Characteristics



On-Resistance vs. Drain Current and Gate Voltage



20
16
12
12
8
T_C = 125 °C
T_C = -55 °C

1.5

2.0

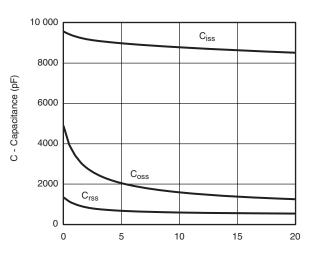
V_{GS} - Gate-to-Source Voltage (V)

3.0

3.5

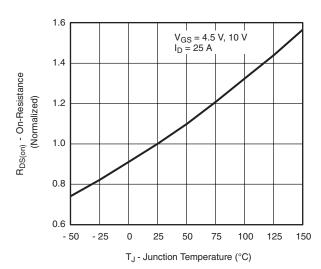
2.5

Transfer Characteristics



V_{DS} - Drain-to-Source Voltage (V)

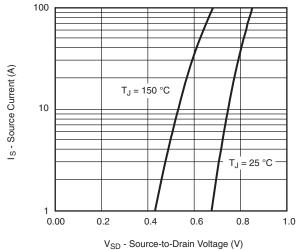
Capacitance



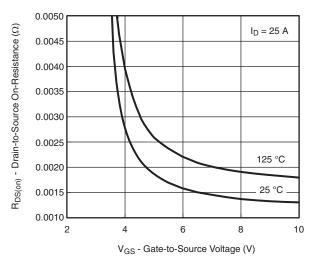
On-Resistance vs. Junction Temperature

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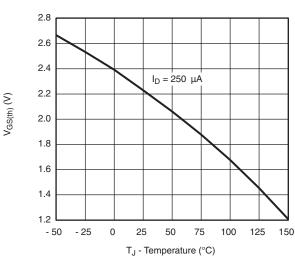
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



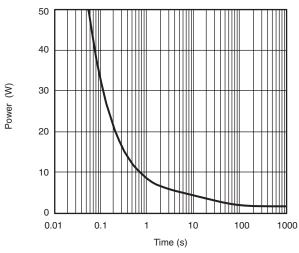
Source-Drain Diode Forward Voltage



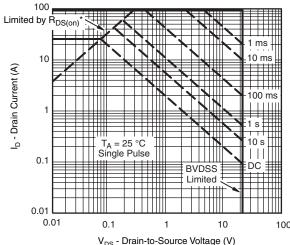
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient



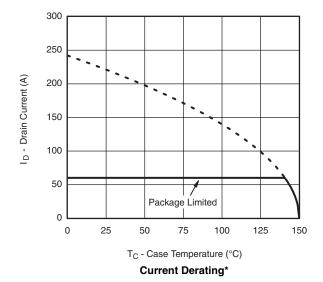
 $\rm V_{DS}$ - Drain-to-Source Voltage (V) $^{\star}\rm \, V_{DS}$ > minimum $\rm V_{GS}$ at which $\rm R_{DS(on)}$ is specified

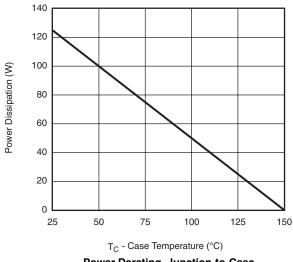
Safe Operating Area, Junction-to-Ambient





TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



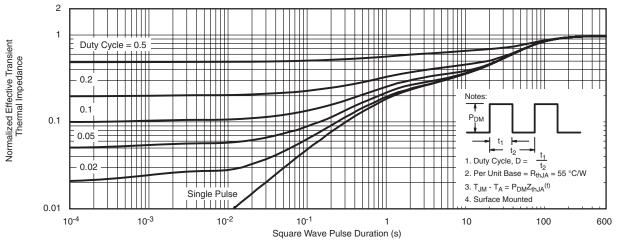


Power Derating, Junction-to-Case

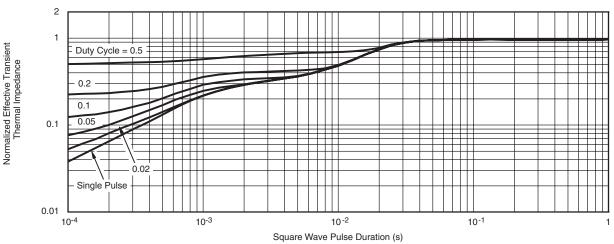
^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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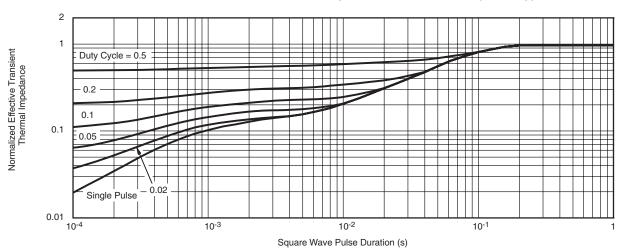
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case (Drain Top)

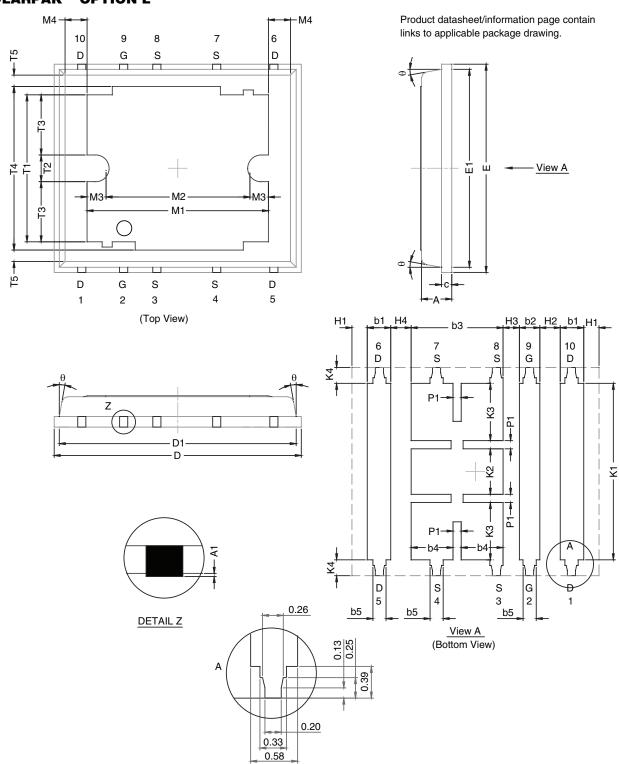


Normalized Thermal Transient Impedance, Junction-to-Source

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppq?73739.



POLARPAK™ OPTION L



Package Information

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DIM	MILLIMETERS			INCHES			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
Α	0.75	0.80	0.85	0.030	0.031	0.033	
A1	0.00	-	0.05	0.000	-	0.002	
b1	0.48	0.58	0.68	0.019	0.023	0.027	
b2	0.41	0.51	0.61	0.016	0.020	0.024	
b3	2.19	2.29	2.39	0.086	0.090	0.094	
b4	0.89	1.04	1.19	0.035	0.041	0.047	
b5	0.23	0.33	0.43	0.009	0.013	0.017	
С	0.20	0.25	0.30	0.008	0.010	0.012	
D	6.00	6.15	6.30	0.236	0.242	0.248	
D1	5.74	5.89	6.04	0.226	0.232	0.238	
E	5.01	5.16	5.31	0.197	0.203	0.209	
E1	4.75	4.90	5.05	0.187	0.193	0.199	
H1	0.23	-	-	0.009	-	-	
H2	0.45	-	0.56	0.018	-	0.022	
H3	0.31	0.41	0.51	0.012	0.016	0.020	
H4	0.45	-	0.56	0.018	-	0.022	
K1	4.22	4.37	4.52	0.166	0.172	0.178	
K2	1.08	1.13	1.18	0.043	0.044	0.046	
K3	1.37	-	-	0.054	-	-	
K4	0.24	-	-	0.009	-	-	
M1	4.30	4.50	4.70	0.169	0.177	0.185	
M2	3.43	3.58	3.73	0.135	0.141	0.147	
МЗ	0.22	-	-	0.009	-	-	
M4	0.05	-	-	0.002	-	-	
P1	0.15	0.20	0.25	0.006	0.008	0.010	
T1	3.48	3.64	4.10	0.137	0.143	0.161	
T2	0.56	0.76	0.95	0.022	0.030	0.037	
T3	1.20	-	-	0.047	-	-	
T4	3.90	-	-	0.153	-	-	
T5	0	0.18	0.36	0.000	0.007	0.014	
θ	0°	10°	12°	0°	10°	12°	

DWG: 5946

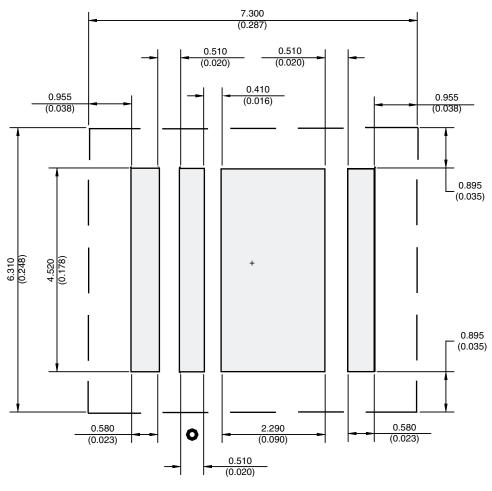
Notes

Millimeters govern over inches.

APPLICATION NOTE



RECOMMENDED MINIMUM PADS FOR PolarPAK® Option L and S



Recommended Minimum for PolarPAK Option L and S Dimensions in mm/(Inches) No External Traces within Broken Lines Dot indicates Gate Pin (Part Marking)

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Revision: 02-Oct-12 Document Number: 91000