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Specification

Part Number:	MC42005A6W-SPTLYI
Version:	1
Date:	17/05/2013

Revision

No.	Date	Description	Item	Page

Contents

Midas LCD Part Number System

MC	COG	132033	A	*	6	W	*	*	-	S	N	T	L	W	*	*
1	2	3	4	5	6	7	8	9	-	10	11	12	13	14	15	16

1 = **MC:** Midas Components

2 = **Blank:** COB (chip on board) **COG**: chip on glass

3 = **No of dots** (e.g. 240064 = 240 x 64 dots) (e.g. 21605 = 2 x 16 5mm C.H.)

4 = **Series**

5 = **Series Variant:** A to Z **– see addendum**

6 = **3:** 3 o'clock **6:** 6 o'clock **9**: 9 o'clock **12**: 12 o'clock

7 = S: Normal (0 to + 50 deg C) **W:** Wide temp. (-20 to + 70 deg C) **X:** Extended temp (-30 + 80 Deg C)

8 = **Character Set**

Blank: Standard (English/Japanese)
C: Chinese Simplified (Graphic Displays only)
CB: Chinese Big 5 (Graphic Displays only)
H: Hebrew
K: European (std) (English/German/French/Greek)
L: English/Japanese (special)
M: European (English/Scandinavian)
R: Cyrillic
W: European (English/Greek)
U: European (English/Scandinavian/Icelandic)

9 = **Bezel Height** (where applicable /available)

	Top of Bezel to Top of PCB	LED Connection Common (via pins 1 and 2)	Array or Edge Lit
Blank	9.5mm / not applicable	via pins 15+ 16-	Array
2	8.9 mm	Common	Array
3	7.8 mm	Separate	Array
4	7.8 mm	Common	Array
5	9.5 mm	Separate	Array
6	7 mm	Common	Array
7	7 mm	Separate	Array
8	6.4 mm	Common	Edge
9	6.4 mm	Separate	Edge
A	5.5 mm	Common	Edge
B	5.5 mm	Separate	Edge
D	6.0mm	Separate	Edge
E	5.0mm	Separate	Edge
F	4.7mm	Common	Edge
G	3.7mm	Separate	EL
H	7 mm	Separate	Edge

10 = **T:** TN S: STN **B:** STN Blue **G:** STN Grey **F:** FSTN **F2:** FFSTN **V:** VA (Vertically Aligned)

11 = **P:** Positive **N**: Negative

12 = **R:** Reflective **M**: Transmissive **T:** Transflective

13 = **Backlight: Blank:** Reflective **L:** LED

14 = **Backlight Colour: Y:** Yellow-Green **W:** White **B:** Blue **R:** Red **A:** Amber **O:** Orange **G:** Green **RGB:** R.G.B.

15 = **Driver Chip:** **Blank:** Standard **I:** I²C S: SPI **T:** Toshiba T6963C **A:** Avant SAP1024B **R:** Raio RA6963

16 = **Voltage Variant**: e.g. **3** = 3v

2. Precautions in use of LCD Modules

(1) Avoid applying excessive shocks to the module or making any alterations or modifications to it.
(2) Don't make extra holes on the printed circuit board, modify its shape or change the components of LCD module.
(3) Don't disassemble the LCM.
(4) Don't operate it above the absolute maximum rating.
(5) Don't drop, bend or twist LCM.
(6) Soldering: only to the I/O terminals.
(7) Storage: please storage in anti-static electricity container and clean environment.

3. General Specification

Item	Dimension	Unit
Number of Characters	20characters x 4 Lines	—
Module dimension (With LED Backlight)	98.0 x 60.0 x 13.5（MAX）	mm
View area	76.0 x 25.2	mm
Active area	70.40 x 20.80	mm
Dot size	0.55 x 0.55	mm
Dot pitch	0.60 x 0.60	mm
Character size	2.95 x 4.75	mm
Character pitch	3.55 x 5.35	mm
LCD type	STN, Yellow-green, Transflective	
Duty	1/16	
View direction	6 o'clock	
Backlight Type	Yellow-green LED backlight	

4. Absolute Maximum Ratings

Item		Symbol	Min	Max	Unit
Input Voltage		V_I	-0.3	VDD+0.3	V
Supply Voltage For Logic		VDD-V_{SS}	-0.3	5.5	V
Supply Voltage For LCD		V_{DD}-V_0	Vdd-7.0	Vdd+0.3	V
Wide Temperature LCM	Operating Temp.	Top	-20	70	°C
	Storage Temp.	Tstr	-30	80	°C

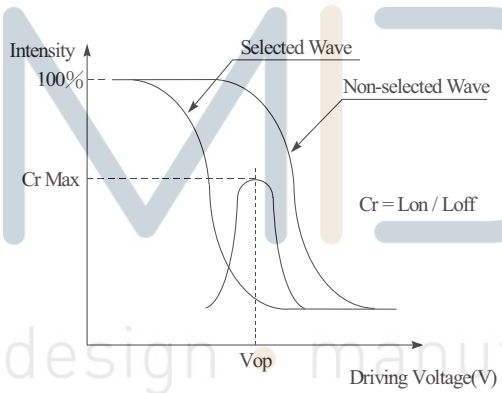
5. Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	V_{DD}-V_{SS}	—	4.5	5.0	5.5	V
Supply Voltage For LCD	V_{DD}-V_0	Ta=25°C	4.2	4.5	4.8	V
Input High Volt.	V_{IH}	—	0.7 V_{DD}	—	V_{DD}	V
Input Low Volt.	V_{IL}	—	V_{SS}	—	0.3 V_{DD}	V
Supply Current	I_{DD}	V_{DD}=5V	0.8	1.2	2.0	mA
Supply Voltage of Yellow-green backlight	V_{LED}	Forward current =180 mA Number of LED die 2x18= 36	3.8	4.2	4.3	V

6. Optical Characteristics

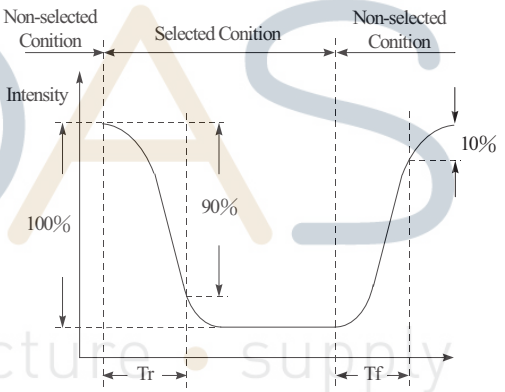
Item	Symbol	Condition	Min	Typ	Max	Unit
View Angle	(V)θ	CR≧2	-20	—	35	deg
	(H)φ	CR≧2	-30	—	30	deg
Contrast Ratio	CR	—	—	3	—	—
Response Time	T rise	—	—	—	250	ms
	T fall	—	—	—	250	ms

Definition of Operation Voltage (Vop)



[positive type]

Definition of Response Time (Tr , Tf)



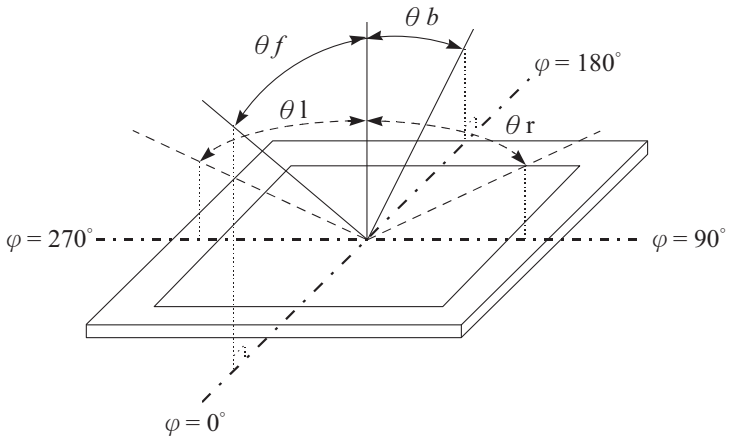
[positive type]

Conditions:

Operating Voltage: Vop　　Viewing Angle (θ，φ): 0°， 0°

Frame Frequency: 64 HZ　　Driving Waveform: 1/N duty, 1/a bias

Definition of viewing angle (CR≧2)

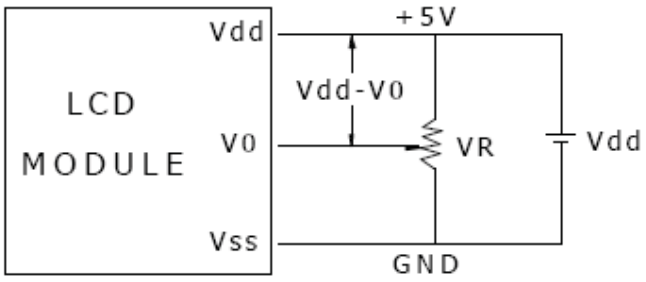


7. Interface Pin Function

Pin No.	Symbol	Level	Description
1	LED(+)		Anode of LED Backlight
2	LED(-)		Cathode of LED Backlight
3	V_{SS}	0V	Ground
4	V_{DD}	5.0V	Supply Voltage for logic
5	SDA	H/L	Serial Data
6	SCL	H/L	Serial Clock
7	V0	(Variable)	Operating voltage for LCD
8	NC		No Connection
9	NC		No Connection
10	NC		No Connection

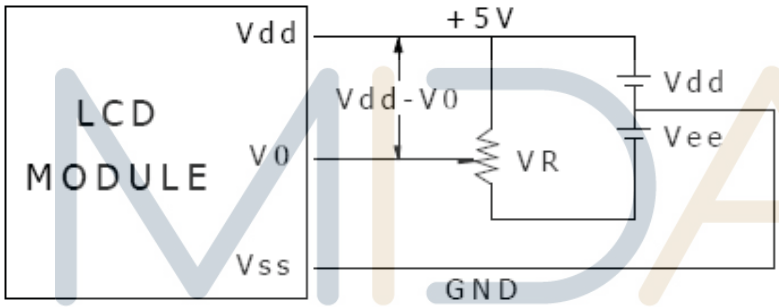
8. Power Supply

SINGLE SUPPLY VOLTAGE TYPE



Vdd-V0: LCD Driving Voltage
VR: 10K - 20K

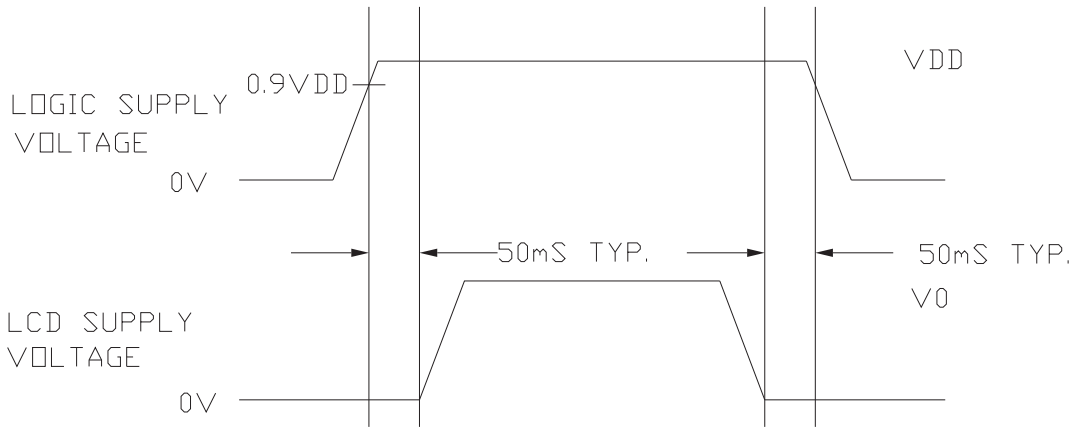
DUAL SUPPLY VOLTAGE TYPE



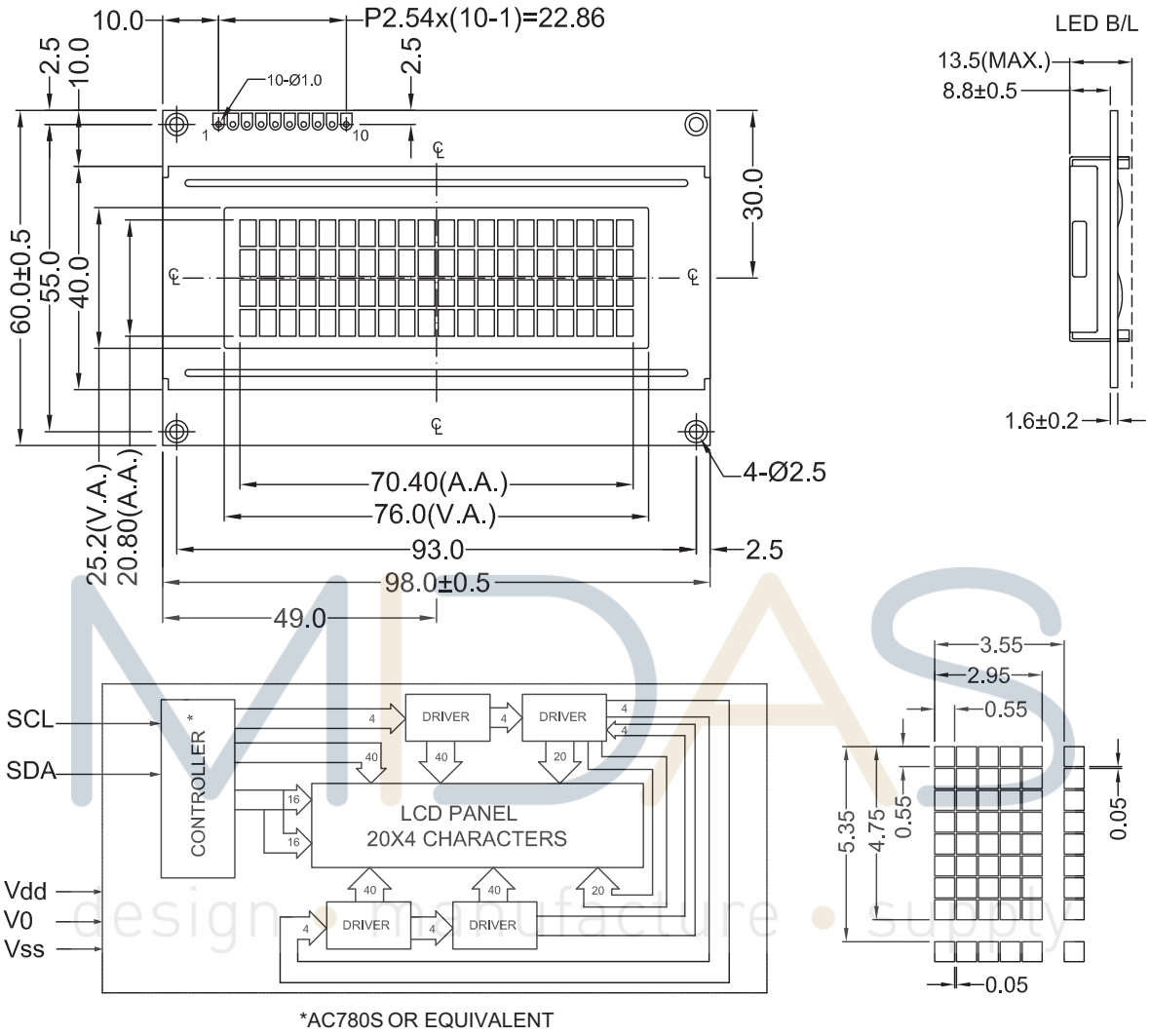
Vdd-V0: LCD Driving Voltage
VR: 10K - 20K

Timing Diagram of VDD Against V0.

Power on sequence shall meet the requirement of Figure 4, the timing diagram of VDD against V0.



9. Contour Drawing & Block Diagram



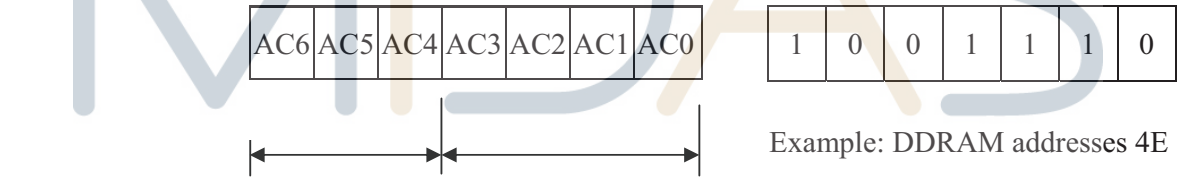
*AC780S OR EQUIVALENT

10. Function Description

The LCD display Module is built in a LSI controller, the controller has two 8-bit registers, an instruction register (IR) and a data register (DR).
The IR stores instruction codes, such as display clear and cursor shift, and address information for display data RAM (DDRAM) and character generator (CGRAM). The IR can only be written from the MPU. The DR temporarily stores data to be written or read from DDRAM or CGRAM. When address information is written into the IR, then data is stored into the DR from DDRAM or CGRAM.

Address Counter (AC)
The address counter (AC) assigns addresses to both DDRAM and CGRAM

Display Data RAM (DDRAM)
This DDRAM is used to store the display data represented in 8-bit character codes. Its extended capacity is 80×8 bits or 80 characters. Below figure is the relationships between DDRAM addresses and positions on the liquid crystal display.



Display position DDRAM address

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53
14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27
54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60	61	62	63	64	65	66	67

4-Line by 20-Character Display

Character Generator ROM (CGROM)
The CGROM generate 5×8 dot or 5×10 dot character patterns from 8-bit character codes. See Table 2.

Character Generator RAM (CGRAM)
In CGRAM, the user can rewrite character by program. For 5×8 dots, eight character patterns

can be written, and for 5×10 dots, four character patterns can be written.

Write into DDRAM the character code at the addresses shown as the left column of table 1. To show the character patterns stored in CGRAM.

Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character patterns

Table 1

For 5 * 8 dot character patterns

Character Codes (DDRAM data)	CGRAM Address	Character Patterns (CGRAM data)
7 6 5 4 3 2 1 0	5 4 3 2 1 0	7 6 5 4 3 2 1 0
High Low	High Low	High Low
0 0 0 0 * 0 0 0	0 0 0 0 0 0	* * * ■■■■ 0
	0 0 1	* * * ■ 0 0 0 ■
	0 1 0	* * * ■ 0 0 0 ■
	0 1 1	* * * ■■■■ 0
	1 0 0	* * * ■ 0 ■ 0 0
	1 0 1	* * * ■ 0 0 ■ 0
	1 1 0	* * * ■ 0 0 0 ■
	1 1 1	* * * 0 0 0 0 0
0 0 0 0 * 0 0 1	0 0 0	* * * ■ 0 0 0 ■
	0 0 1	* * * 0 ■ 0 ■ 0
	0 1 0	* * * ■■■■■
	0 1 1	* * * 0 0 ■ 0 0
	1 0 0	* * * ■■■■■
	1 0 1	* * * 0 0 ■ 0 0
	1 1 0	* * * 0 0 ■ 0 0
	1 1 1	* * * 0 0 0 0 0
	0 0 0	* * *
	0 0 1	
0 0 0 0 * 1 1 1	1 1 1 0 0 0	
	1 0 1	
	1 1 0	
	1 1 1	* * *

Character pattern(1)

Cursor pattern

Character pattern(2)

Cursor pattern

For 5 * 10 dot character patterns

Character Codes (DDRAM data)	CGRAM Address	Character Patterns (CGRAM data)
7 6 5 4 3 2 1 0	5 4 3 2 1 0	7 6 5 4 3 2 1 0
High Low	High Low	High Low
0 0 0 0 * 0 0 0	0 0 0 0 0 0 0	* * * 0 0 0 0 0
	0 0 0 1	* * * 0 0 0 0 0
	0 0 1 0	* * * ■ 0 ■■■ 0
	0 0 1 1	* * * ■■ 0 0 ■
	0 1 0 0	* * * ■ 0 0 0 ■
	0 1 0 1	* * * ■ 0 0 0 ■
	0 1 1 0	* * * ■■■■■ 0
	0 1 1 1	* * * ■ 0 0 0 0
	1 0 0 0	* * * ■ 0 0 0 0
	1 0 0 1	* * * ■ 0 0 0 0
	1 0 1 0	* * * 0 0 0 0 0
	1 1 1 1	* * * * * * * *

Character pattern

Cursor pattern

■ : " High "

11. Character Generator ROM Pattern

12. Instruction Table

Instruction	Instruction Code										Description	Execution time (fosc=210Khz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write “20H” to DDRAM and set DDRAM address to “00H” from AC	1.98ms
Return Home	0	0	0	0	0	0	0	0	1	—	Set DDRAM address to “00H” from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.98ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and enable the shift of entire display.	48μs
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor (C), and blinking of cursor (B) on/off control bit.	48μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	—	—	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.	48μs
Function Set	0	0	0	0	1	DL	N	F	—	—	Set interface data length (DL:8-bit/4-bit), numbers of display line (N:2-line/1-line)and, display font type (F:5×11 dots/5×8 dots)	48μs
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	48μs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	48μs
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	48μs

＊ ”—” : N/A

13. Interface with MPU

- **For serial interface data, bus lines (DB5(CSB)、DB6(SDA) and DB7(SCL)) are used. IIC interface**

The IIC interface receives and executes the commands sent via the IIC Interface. It also receives RAM data and sends it to the RAM.
The IIC Interface is for bi-directional, two-line communication between different ICs or modules. Serial data line SDA (DB6) and a Serial clock line SCL (DB7) must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.
*The CSB (DB5) Pin must be setting to "VSS".
* When IIC interface is selected, the DL register must be set to "1".

➢ **BIT TRANSFER**

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Fig.9.1

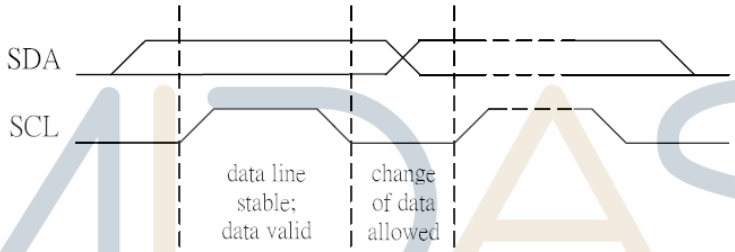


Fig .9.1 Bit transfer

➢ **START AND STOP CONDITIONS**

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig.9.2

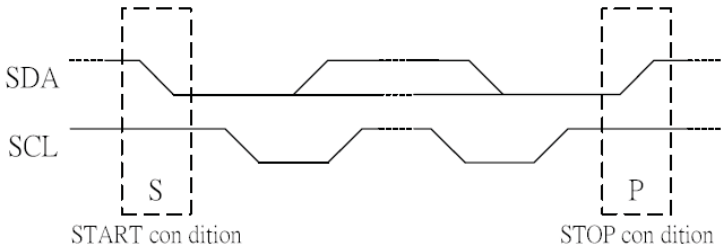


Fig .9.2 Definition of START and STOP conditions

➢ SYSTEM CONFIGURATION

The system configuration is illustrated in Fig.9.3
· Transmitter: the device, which sends the data to the bus
· Receiver: the device, which receives the data from the bus
· Master: the device, which initiates a transfer, generates clock signals and terminates a transfer
· Slave: the device addressed by a master
· Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message
· Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
· Synchronization: procedure to synchronize the clock signals of two or more devices.

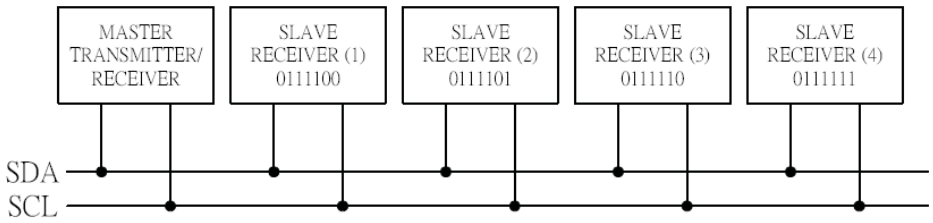


Fig .9.3 System configuration

➢ ACKNOWLEDGE

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an Acknowledge after the reception of each byte. A master receiver must also generate an Acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the Acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by not generating an Acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the IIC Interface is illustrated in Fig.9.4

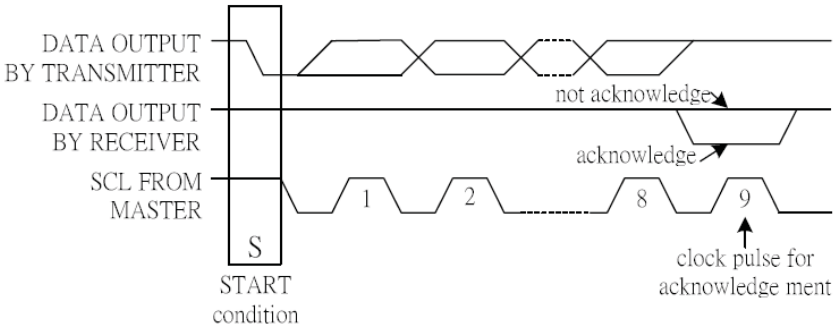


Fig .9.4 Acknowledgement on the 2-line Interface

➢ **IIC Interface protocol**

The RW1063 supports command, data write addressed slaves on the bus.
Before any data is transmitted on the IIC Interface, the device, which should respond, is addressed first.
Four 7-bit slave addresses (0111100, 0111101, 0111110 and 0111111) are reserved for the RW1063. The least significant bit of the slave address is set by connecting the input SA0 (DB0) and SA1 (DB1) to either logic 0 (VSS) or logic 1 (VDD).
The IIC Interface protocol is illustrated in Figure.9.5
The sequence is initiated with a START condition (S) from the IIC Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the IIC Interface transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves.
A command word consists of a control byte, which defines Co and A0, plus a data byte.
The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data bytes will follow. The state of the A0 bit defines whether the data byte is interpreted as a command or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte, depending on the A0 bit setting; either a series of display data bytes or command data bytes may follow. If the A0 bit is set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended RW1063 device. If the A0 bit of the last control byte is set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the IIC interface-bus master issues a STOP condition (P). If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

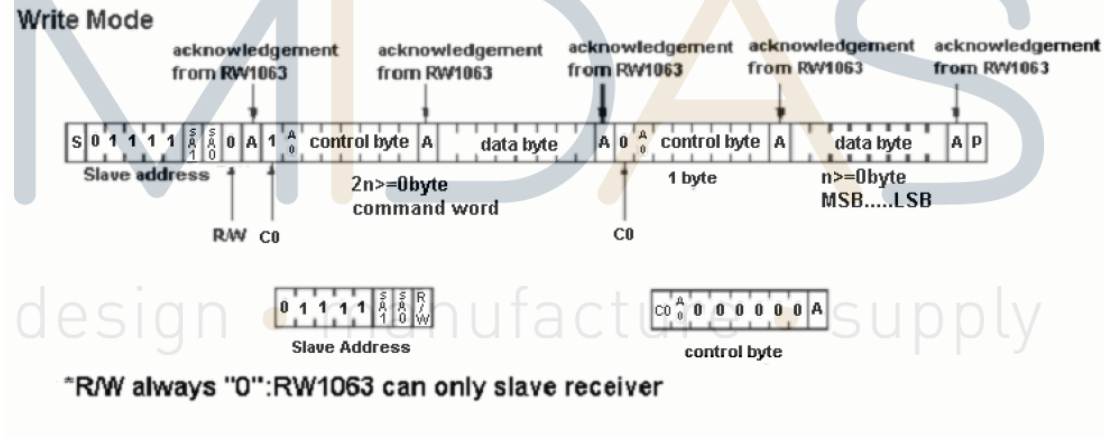


Fig .9.5 2-line Interface protocol

Co	0	Last control byte to be sent. Only a stream of data bytes is allowed to follow. This stream may only be terminated by s STOP or RE-START condition.
	1	Another control byte will follow the data byte unless a STOP or RE-START condition is received.

Slave Address Option:

J8,J10 short,J7,J9open, SA1=0,SA0=0(default setting);

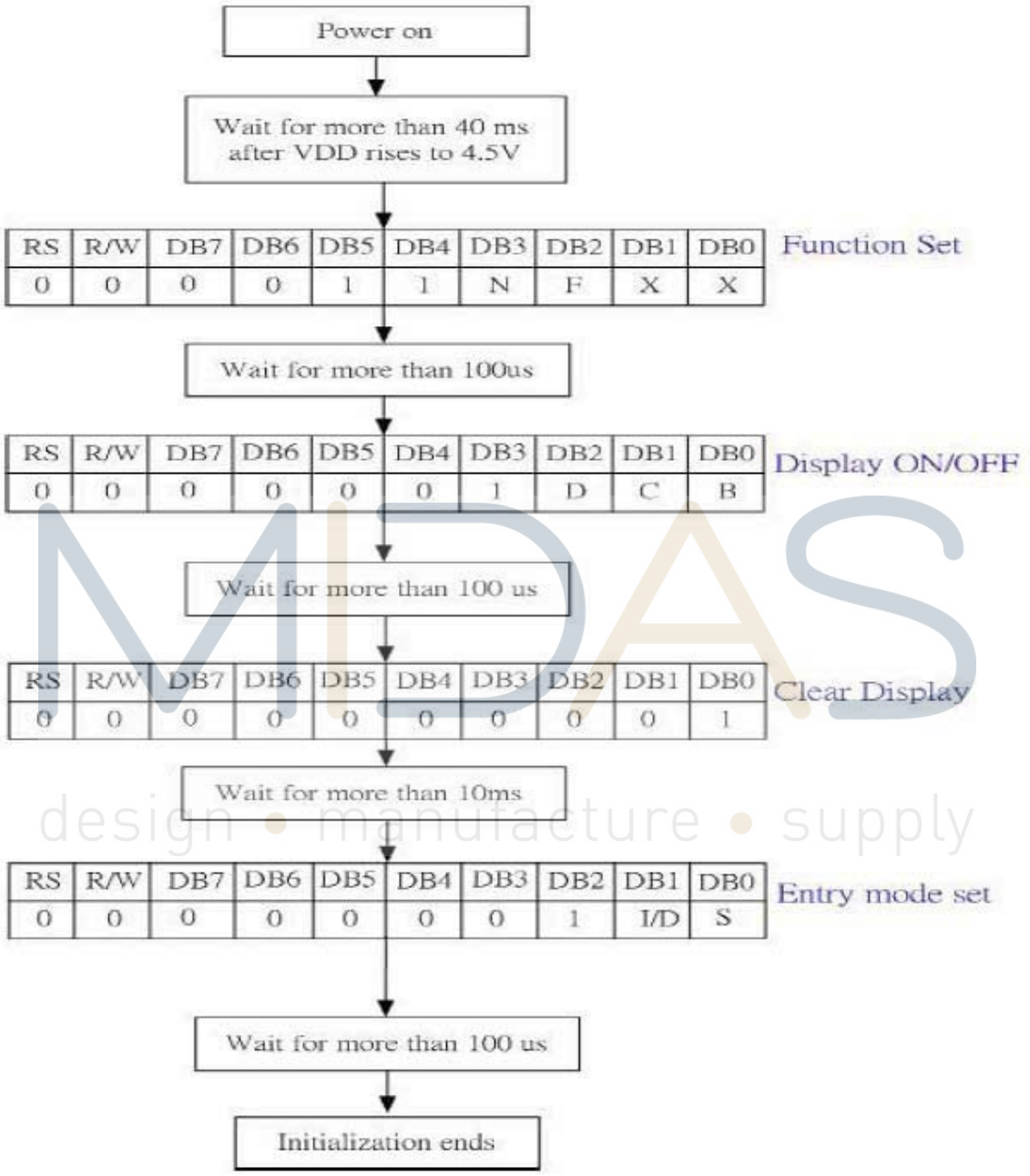
J8,J9 short,J7,J10open, SA1=0,SA0=1;

J7,J10 short,J8,J9open, SA1=1,SA0=0;

J7,J9 short,J8,J10open, SA1=1,SA0=1;

DB5(CSB)is connected to Vss by short J6.

14. Initializing of LCM



Initial Code:

```
void WriteData(BYTE byData)
{
	I2C_Start();
	I2C_Send(0x78);
	I2C_Ack();
	I2C_Send(0x40);
	I2C_Ack();
	I2C_Send(byData);
	I2C_Ack();
	I2C_Stop();
}

void WriteInst(BYTE byInst)
{
	I2C_Start();
	I2C_Send(0x78);
	I2C_Ack();
	I2C_Send(0x00);
	I2C_Ack();
	I2C_Send(byInst);
	I2C_Ack();
	I2C_Stop();
}

void InitRW1063(void)
{
	WriteInst (0x38);    //DL=1: 8 bits; N=1: 2 line; F=0: 5 x 8dots
	WriteInst (0x0c);    // D=1, display on; C=B=0; cursor off; blinking off;
	WriteInst (0x06);    // I/D=1: Increment by 1; S=0: No shift
}
```

15. Quality Assurance

Screen Cosmetic Criteria

Item	Defect	Judgment Criterion	Partition
1	Spots	A)Clear Size: d mm — Acceptable Qty in active area d ≦0.1 — Disregard 0.1<d≦0.2 — 6 0.2<d≦0.3 — 2 0.3<d — 0 Note: Including pin holes and defective dots which must be within one pixel size. B)Unclear Size: d mm — Acceptable Qty in active area d ≦0.2 — Disregard 0.2<d≦0.5 — 6 0.5<d≦0.7 — 2 0.7<d — 0	Minor
2	Bubbles in Polarizer	Size: d mm — Acceptable Qty in active area d≦0.3 — Disregard 0.3<d≦1.0 — 3 1.0<d≦1.5 — 1 1.5<d — 0	Minor
3	Scratch	In accordance with spots cosmetic criteria. When the light reflects on the panel surface, the scratches are not to be remarkable.	Minor
4	Allowable Density	Above defects should be separated more than 30mm each other.	Minor
5	Coloration	Not to be noticeable coloration in the viewing area of the LCD panels. Back-light type should be judged with back-light on state only.	Minor

16. Reliability

Content of Reliability Test

Environmental Test			
Test Item	**Content of Test**	**Test Condition**	**Applicable Standard**
High Temperature storage	Endurance test applying the high storage temperature for a long time.	80°C 96hrs	——
Low Temperature storage	Endurance test applying the high storage temperature for a long time.	-30°C 96hrs	——
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70°C 96hrs	——
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20°C 96hrs	——
High Temperature/ Humidity Storage	Endurance test applying the high temperature and high humidity storage for a long time.	80°C, 90%RH 96hrs	——
High Temperature/ Humidity Operation	Endurance test applying the electric stress (Voltage & Current) and temperature / humidity stress to the element for a long time.	70°C, 90%RH 96hrs	——
Temperature Cycle	Endurance test applying the low and high temperature cycle. -30°C 25°C 80°C 30min 5min 30min 1 cycle	-30°C →80°C 10 cycles	——
Mechanical Test			
Vibration test	Endurance test applying the vibration during transportation and using.	10~22Hz→1.5mmp-p 22~500Hz→1.5G Total 0.5hrs	——
Shock test	Constructional and mechanical endurance test applying the shock during transportation.	50G Half sign wave 11 msedc 3 times of each direction	——

***Supply voltage for logic system=5V. Supply voltage for LCD system =Operating voltage at 25°C