

Specification				
Part Number:		MC42005B6WK-SPTLY		
Version:		1		
Date:		10/03/2010		
Revision				
No.	Date	Description	Item	Page
1	08/1999	Initial Issued	-	-
2	03/2005	Modify the full specification	-	-
3	12/2005	Update the part number system	-	-
4	03/2006	Add Red backlight	-	-

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Midas 2006 version logo. Midas is an integrated manufacturer of flat panel display (FPD). Midas supplies TN, HTN, STN, FSTN monochrome LCD panel; COB, COG, TAB LCD module; and all kinds of LED backlight.



#### FAST RESPONSE TIME

This icon on the cover indicates the product is with high response speed; Otherwise not.



#### PROTECTION CIRCUIT

This icon on the cover indicates the product is with protection circuit; Otherwise not.



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This icon on the cover indicates the product is with high contrast; Otherwise not.



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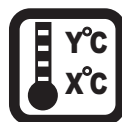
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#### RoHS COMPLIANCE

This icon on the cover indicates the product meets ROHS requirements; Otherwise not.



#### OPERATION TEMPERATURE RANGE

This icon on the cover indicates the operating temperature range (X-Y).



#### 3TIMES 100% QC EXAMINATION

This icon on the cover indicates the product has passed Midas thrice 100% QC. Otherwise not.



#### TWICE SELECTION OF LED MATERIALS

This icon on the cover indicates the LED had passed Midas twice strict selection which promises the product's identical color and brightness; Otherwise not.



#### V1cm = 3.0V

This icon on the cover indicates the product can work at 3.0V exactly; otherwise not.



#### N SERIES TECHNOLOGY (2008 developed)

New structure, new craft, new technology and new materials inside both LCD module and LCD panel to improve the "RainBow"

# Contents

- 1.Module Classification Information
- 2.Precautions in use of LCD Modules
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# Midas LCD Part Number System

MC	COG	132033	A	*	6	W	*	*	-	S	N	T	L	W	*	*
1	2	3	4	5	6	7	8	9	-	10	11	12	13	14	15	16

1 = **MC:** Midas Components

2 = **Blank:** COB (chip on board) **COG:** chip on glass

3 = **No of dots** (e.g. 240064 = 240 x 64 dots) (e.g. 21605 = 2 x 16 5mm C.H.)

4 = **Series**

5 = **Series Variant:** A to Z – see addendum

6 = **3:** 3 o'clock **6:** 6 o'clock **9:** 9 o'clock **12:** 12 o'clock

7 = **S:** Normal (0 to + 50 deg C) **W:** Wide temp. (-20 to + 70 deg C) **X:** Extended temp (-30 + 80 Deg C)

8 = **Character Set**

**Blank:** Standard (English/Japanese)

**C:** Chinese Simplified (Graphic Displays only)

**CB:** Chinese Big 5 (Graphic Displays only)

**H:** Hebrew

**K:** European (std) (English/German/French/Greek)

**L:** English/Japanese (special)

**M:** European (English/Scandinavian)

**R:** Cyrillic

**W:** European (English/Greek)

**U:** European (English/Scandinavian/Icelandic)

9 = **Bezel Height** (where applicable /available)

	Top of Bezel to Top of PCB	LED Connection Common (via pins 1 and 2) via pins 15+ 16-	Array or Edge Lit
<b>Blank</b>	9.5mm / not applicable		Array
<b>2</b>	8.9 mm	Common	Array
<b>3</b>	7.8 mm	Separate	Array
<b>4</b>	7.8 mm	Common	Array
<b>5</b>	9.5 mm	Separate	Array
<b>6</b>	7 mm	Common	Array
<b>7</b>	7 mm	Separate	Array
<b>8</b>	6.4 mm	Common	Edge
<b>9</b>	6.4 mm	Separate	Edge
<b>A</b>	5.5 mm	Common	Edge
<b>B</b>	5.5 mm	Separate	Edge
<b>D</b>	6.0mm	Separate	Edge
<b>E</b>	5.0mm	Separate	Edge
<b>F</b>	4.7mm	Common	Edge
<b>G</b>	3.7mm	Separate	EL
<b>H</b>	7 mm	Separate	Edge

10 = **T:** TN **S:** STN **B:** STN Blue **G:** STN Grey **F:** FSTN **F2:** FFSTN **V:** VA (Vertically Aligned)

11 = **P:** Positive **N:** Negative

12 = **R:** Reflective **M:** Transmissive **T:** Transflective

13 = **Backlight:** **Blank:** Reflective **L:** LED

14 = **Backlight Colour:** **Y:** Yellow-Green **W:** White **B:** Blue **R:** Red **A:** Amber **O:** Orange **G:** Green **RGB:** R.G.B.

15 = **Driver Chip:** **Blank:** Standard **I:** I<sup>2</sup>C **S:** SPI **T:** Toshiba T6963C **A:** Avant SAP1024B **R:** Raio RA6963

16 = **Voltage Variant:** e.g. **3** = 3v

## **2. Precautions in use of LCD Modules**

- (1) Avoid applying excessive shocks to the module or making any alterations or modifications to it.
- (2) Don't make extra holes on the printed circuit board, modify its shape or change the components of LCD module.
- (3) Don't disassemble the LCM.
- (4) Don't operate it above the absolute maximum rating.
- (5) Don't drop, bend or twist LCM.
- (6) Soldering: only to the I/O terminals.
- (7) Storage: please storage in anti-static electricity container and clean environment.

## **3. General Specification**

Item	Dimension	Unit
Number of Characters	20characters x 4 Lines	—
Module dimension(No Backlight )	98.0 x 60.0 x 10.0 (MAX)	mm
Module dimension(With LED Backlight )	98.0 x 60.0 x 15.0 (MAX)	mm
View area	76.0 x 25.2	mm
Active area	70.40 x 20.80	mm
Dot size	0.55 x 0.55	mm
Dot pitch	0.60 x 0.60	mm
Character size	2.95 x 4.75	mm
Character pitch	3.55 x 5.35	mm
LCD type	STN	
Duty	1/16	
View direction	6 o'clock or 12 o'clock	
Backlight Type	[ gmqy II tggp"LED dce mki j v"	

## 4. Absolute Maximum Ratings

Item		Symbol	Min	Max	Unit
Input Voltage		$V_I$	-0.3	$V_{DD}+0.3$	V
Supply Voltage For Logic		$V_{DD}-V_{SS}$	-0.3	7.0	V
Supply Voltage For LCD		$V_{DD}-V_0$	$V_{dd}-13.5$	0	V
Standard	Operating Temp.	Top	0	50	°C
Temperature LCM	Storage Temp.	Tstr	-10	60	°C
Wide Temperature	Operating Temp.	Top	-20	70	°C
LCM	Storage Temp.	Tstr	-30	80	°C

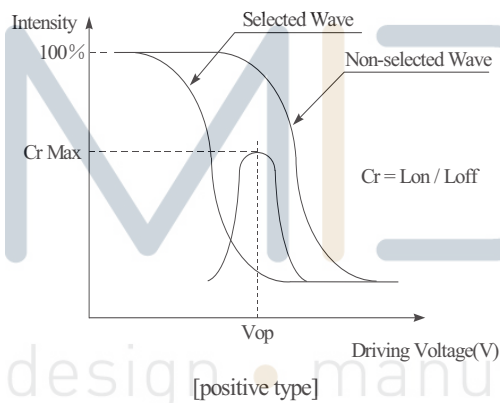
## 5. Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	$V_{DD}-V_{SS}$	—	4.5	5.0	5.5	V
Supply Voltage For LCD	$V_{DD}-V_0$	$T_a=25^{\circ}\text{C}$	4.5	5.0	5.5	V
Input High Volt.	$V_{IH}$	—	$0.7 V_{DD}$	—	$V_{DD}$	V
Input Low Volt.	$V_{IL}$	—	$V_{SS}$	—	$0.3 V_{DD}$	V
Supply Current	$I_{DD}$	$V_{DD}=5\text{V}$	0.7	0.75	1.5	mA
Supply Voltage of Yellow-green backlight	$V_{LED}$	Forward current =180 mA Number of LED die 2x18= 36	4.0	4.2	4.4	V
Supply Voltage of White backlight	$V_{LED}$	Forward current =30 mA Number of LED die 2	3.8	4.0	4.2	V
Supply Voltage of RED backlight	$V_{LED}$	Forward current =180 mA Number of LED die 2x18= 36	3.5	3.9	4.1	V

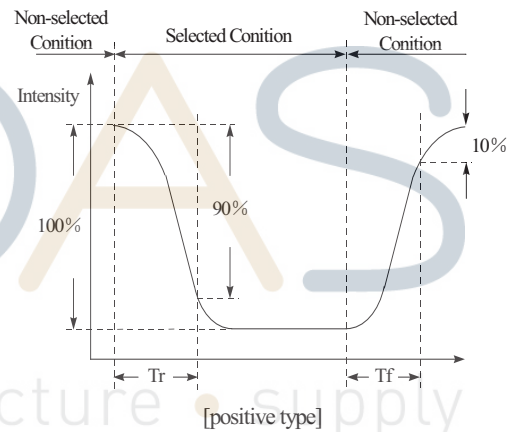
## 6. Optical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
View Angle	(V) $\theta$	$CR \geq 2$	-20	—	35	deg
	(H) $\phi$	$CR \geq 2$	-30	—	30	deg
Contrast Ratio	CR	—	—	3	—	—
Response Time	T rise	—	—	—	250	ms
	T fall	—	—	—	250	ms

### Definition of Operation Voltage (Vop)



### Definition of Response Time (Tr , Tf)



### Conditions :

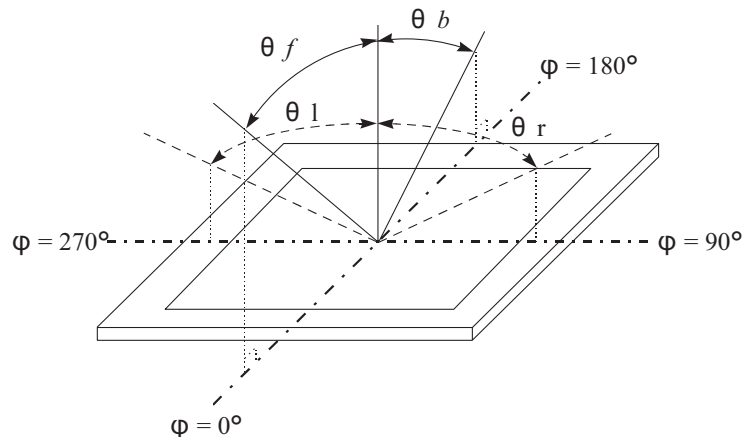
Operating Voltage : Vop

Viewing Angle( $\theta$  ,  $\phi$ ) :  $0^\circ$  ,  $0^\circ$

Frame Frequency : 64 HZ

Driving Waveform : 1/N duty , 1/a bias

### Definition of viewing angle( $CR \geq 2$ )



## **7. Interface Pin Function**

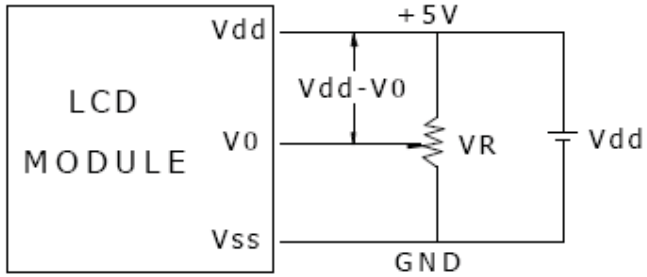
Pin No.	Symbol	Level	Description
1	V <sub>SS</sub>	0V	Ground
2	V <sub>DD</sub>	5.0V	Supply Voltage for logic
3	V <sub>0</sub>	(Variable)	Operating voltage for LCD
4	RS	H/L	H: DATA, L: Instruction code
5	R/W	H/L	H: Read(MPU→Module) L: Write(MPU→Module)
6	E	H,H→L	Chip enable signal
7	DB0	H/L	Data bit 0
8	DB1	H/L	Data bit 1
9	DB2	H/L	Data bit 2
10	DB3	H/L	Data bit 3
11	DB4	H/L	Data bit 4
12	DB5	H/L	Data bit 5
13	DB6	H/L	Data bit 6
14	DB7	H/L	Data bit 7
15	LED(+)		Anode of LED Backlight
16	LED(-)		Cathode of LED Backlight

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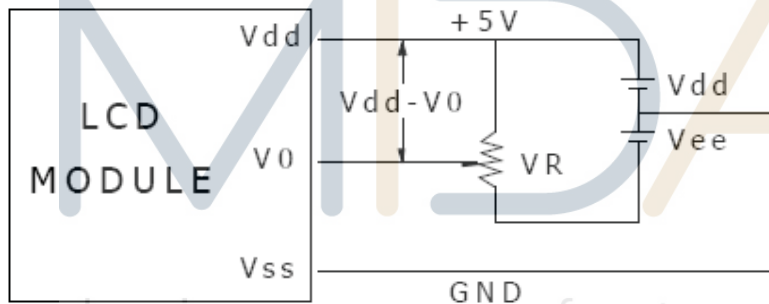
## 8. POWER SUPPLY

### SINGLE SUPPLY VOLTAGE TYPE



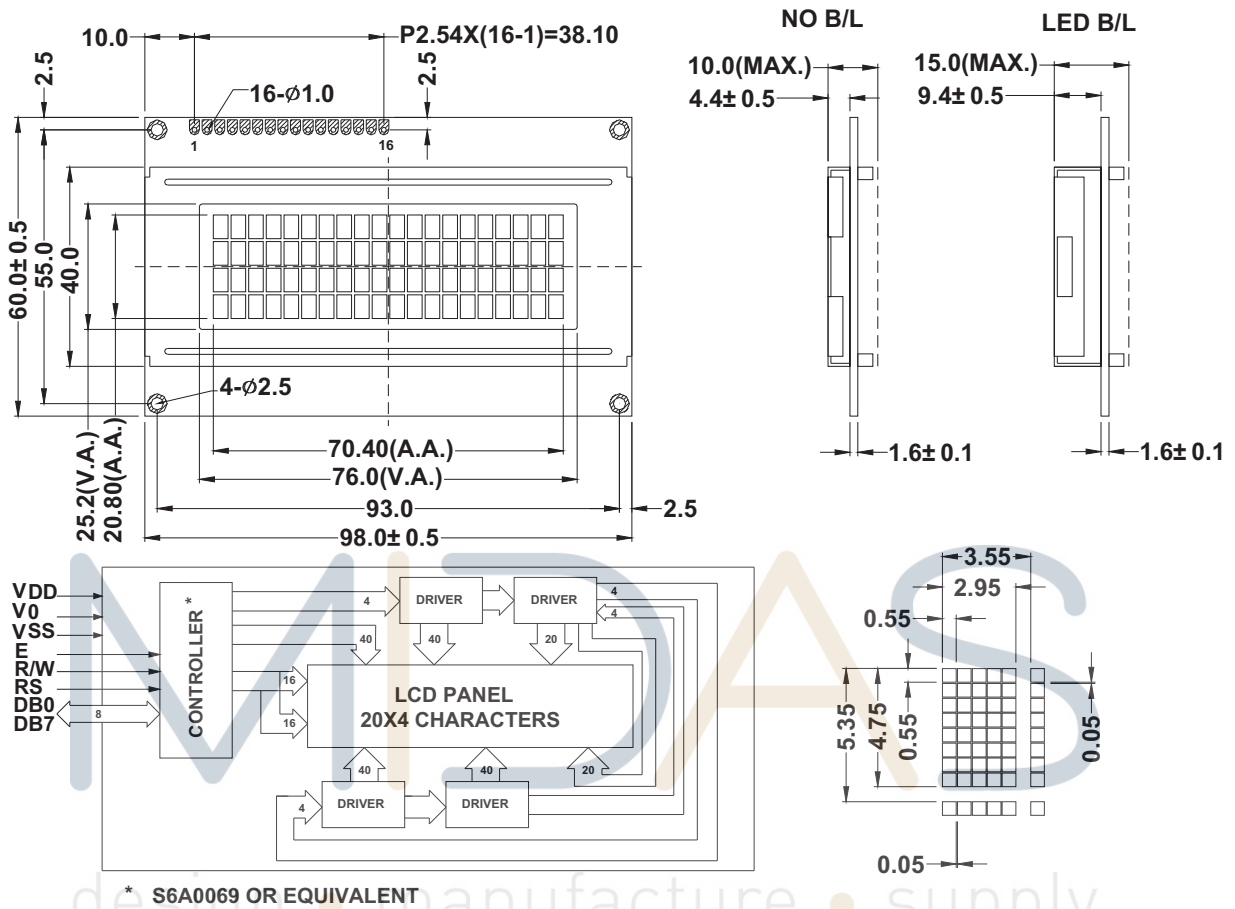
Vdd-V0: LCD Driving Voltage  
VR: 10K - 20K

### DUAL SUPPLY VOLTAGE TYPE



Vdd-V0: LCD Driving Voltage  
VR: 10K - 20K

## 9. Contour Drawing & Block Diagram



## 10. Function Description

The LCD display Module is built in a LSI controller, the controller has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for display data RAM (DDRAM) and character generator (CGRAM). The IR can only be written from the MPU. The DR temporarily stores data to be written or read from DDRAM or CGRAM. When address information is written into the IR, then data is stored into the DR from DDRAM or CGRAM. By the register selector (RS) signal, these two registers can be selected.

RS	R/W	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB7) and address counter (DB0 to DB7)
1	0	Write data to DDRAM or CGRAM (DR to DDRAM or CGRAM)
1	1	Read data from DDRAM or CGRAM (DDRAM or CGRAM to DR)

### Busy Flag (BF)

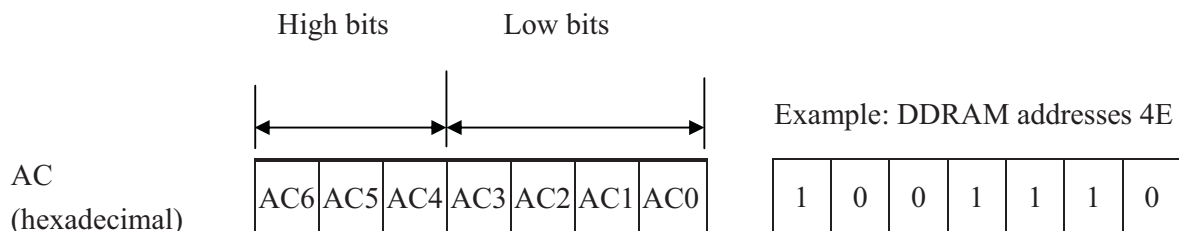
When the busy flag is 1, the controller LSI is in the internal operation mode, and the next instruction will not be accepted. When RS=0 and R/W=1, the busy flag is output to DB7. The next instruction must be written after ensuring that the busy flag is 0.

### Address Counter (AC)

The address counter (AC) assigns addresses to both DDRAM and CGRAM

### Display Data RAM (DDRAM)

This DDRAM is used to store the display data represented in 8-bit character codes. Its extended capacity is 80×8 bits or 80 characters. Below figure is the relationships between DDRAM addresses and positions on the liquid crystal display.



### Display position DDRAM address

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20

00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53
80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93
C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3

4-Line by 20-Character Display

### Character Generator ROM (CGROM)

The CGROM generate  $5 \times 8$  dot or  $5 \times 10$  dot character patterns from 8-bit character codes. See Table 2.

### Character Generator RAM (CGRAM)

In CGRAM, the user can rewrite character by program. For  $5 \times 8$  dots, eight character patterns can be written, and for  $5 \times 10$  dots, four character patterns can be written.

Write into DDRAM the character code at the addresses shown as the left column of table 1. To show the character patterns stored in CGRAM.

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## Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character patterns

**Table 1.**

For 5 \* 8 dot character patterns

Character Codes ( DDRAM data )		CGRAM Address		Character Patterns ( CGRAM data )	
7 6 5 4 3 2 1 0		5 4 3 2 1 0		7 6 5 4 3 2 1 0	
High Low		High Low		High Low	
0 0 0 0 * 0 0 0		0 0 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1 0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 1	* *	0 0
0 0 0 0 * 0 0 1		0 0 1	1 0 0 1 0 1 1 1 0 1 1 1	* * * * * * * * * * * *	0 0 0 0 0 0 0 0 0 0
0 0 0 0 * 1 1 1		1 1 1	1 0 0 1 0 1 1 1 0 1 1 1	* * * * * * * * * * * *	0 0 0 0 0 0 0 0 0 0

Character pattern( 1 )

Cursor pattern

Character pattern( 2 )

Cursor pattern

For 5 \* 10 dot character patterns

Character Codes ( DDRAM data )		CGRAM Address		Character Patterns ( CGRAM data )	
7 6 5 4 3 2 1 0		5 4 3 2 1 0		7 6 5 4 3 2 1 0	
High Low		High Low		High Low	
0 0 0 0 * 0 0 0		0 0	0 0 0 0 0 0 0 1 0 0 1 0 0 0 1 1 0 1 0 0 0 1 0 1 0 1 1 0 0 1 1 1 1 0 0 0 1 0 0 1 1 0 1 0	* *	0 0
			1 1 1 1	* * * * * *	* * * * * *

Character pattern

Cursor pattern

■ : " High "

# 11. Character Generator ROM Pattern

		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Lower 4-bit (D0 to D3) of Character Code (Hexadecimal)	0	CG RAM (1)			0	a	P	`	p				—	3	E	o	p
	1	CG RAM (2)		!	1	A	O	a	a			a	7	*	4	a	g
	2	CG RAM (3)		"	2	B	R	b	r			"	4	"	x	p	o
	3	CG RAM (4)		#	3	C	S	c	s			#	5	7	e	e	o
	4	CG RAM (5)		\$	4	D	T	t	t			\$	6	8	p	a	a
	5	CG RAM (6)		%	5	E	L	e	u			%	7	*	1	e	o
	6	CG RAM (7)		&	6	F	V	v	v			&	8	2	9	p	z
	7	CG RAM (8)		'	7	G	W	w	w			'	9	3	0	g	n
	8	CG RAM (1)		(	8	H	X	x	x			(	0	4	1	v	x
	9	CG RAM (2)		)	9	I	Y	y	y			)	1	5	2	~	y
	A	CG RAM (3)		*	A	J	Z	z	z			*	2	6	3	j	*
	B	CG RAM (4)		+	B	K	[	k	[			+	3	7	4	*	*
	C	CG RAM (5)		,	C	L	]	l	l			,	4	8	5	o	a
	D	CG RAM (6)		-	D	M	^	m	^			-	5	9	6	+	÷
	E	CG RAM (7)		.	E	N	_	n	_			.	6	0	7	^	^
	F	CG RAM (8)		/	F	O	~	o	~			/	7	1	8	o	■

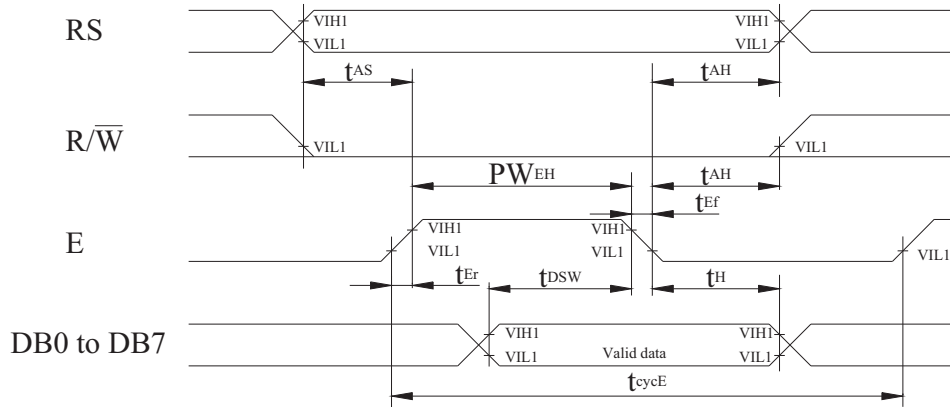
## 12. Instruction Table

Instruction	Instruction Code										Description	Execution time (fosc=270Khz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "00H" to DDRAM and set DDRAM address to "00H" from AC	1.53ms
Return Home	0	0	0	0	0	0	0	0	1	—	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.53ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and enable the shift of entire display.	39μs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor (C), and blinking of cursor (B) on/off control bit.	39μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	—	—	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.	39μs
Function Set	0	0	0	0	1	DL	N	F	—	—	Set interface data length (DL:8-bit/4-bit), numbers of display line (N:2-line/1-line)and, display font type (F:5×11 dots/5×8 dots)	39μs
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	39μs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	39μs
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0μs
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43μs
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	43μs

\* "—" : don't care

## 13. Timing Characteristics

### 13.1 Write Operation

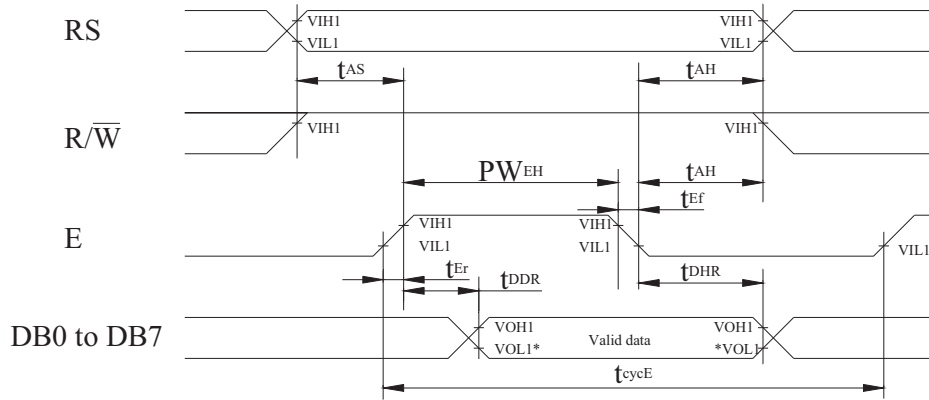


Ta=25°C, VDD=5.0±0.5V

Item	Symbol	Min	Typ	Max	Unit
Enable cycle time	t <sub>cycE</sub>	1200	—	—	ns
Enable pulse width (high level)	PW <sub>EH</sub>	140	—	—	ns
Enable rise/fall time	t <sub>Er</sub> , t <sub>Ef</sub>	—	—	25	ns
Address set-up time (RS, R/W to E)	t <sub>AS</sub>	0	—	—	ns
Address hold time	t <sub>AH</sub>	10	—	—	ns
Data set-up time	t <sub>Dsw</sub>	40	—	—	ns
Data hold time	t <sub>H</sub>	10	—	—	ns



## 13.2 Read Operation



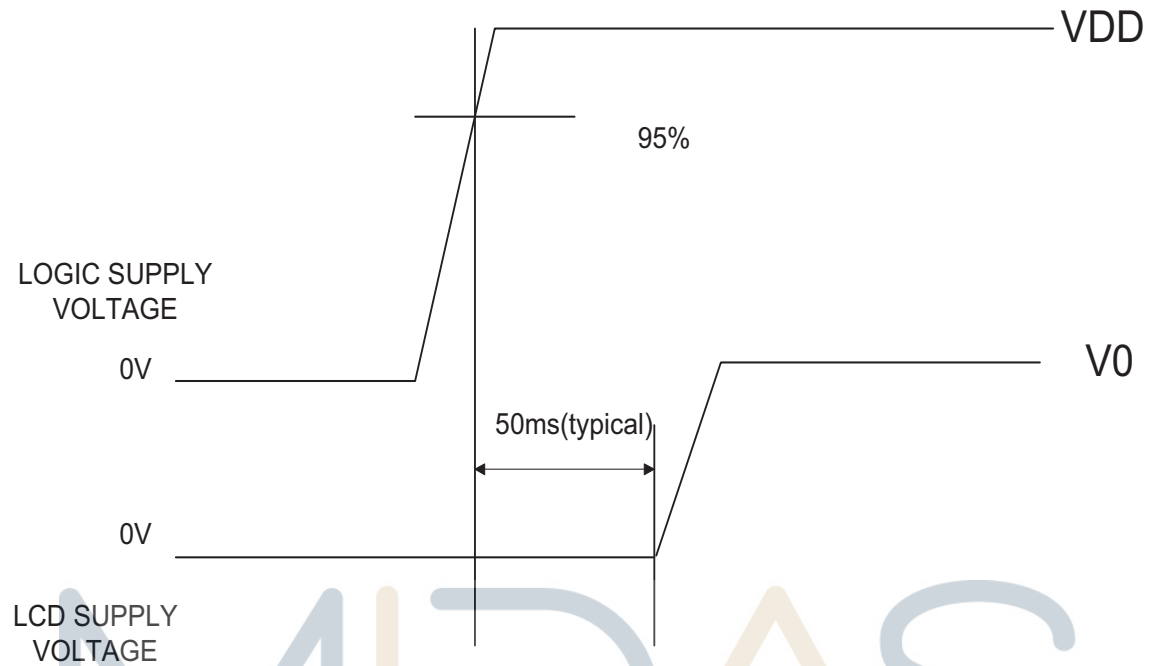
NOTE: \*VOL1 is assumed to be 0.8V at 2 MHz operation.

$T_a=25^{\circ}\text{C}$ ,  $V_{DD}=5.0\pm 0.5\text{V}$

Item	Symbol	Min	Typ	Max	Unit
Enable cycle time	$t_{cycE}$	1200	—	—	ns
Enable pulse width (high level)	$PW_{EH}$	140	—	—	ns
Enable rise/fall time	$t_{Er}, t_{Ef}$	—	—	25	ns
Address set-up time (RS, R/W to E)	$t_{AS}$	0	—	—	ns
Address hold time	$t_{AH}$	10	—	—	ns
Data delay time	$t_{DDR}$	—	—	100	ns
Data hold time	$t_{DHR}$	10	—	—	ns

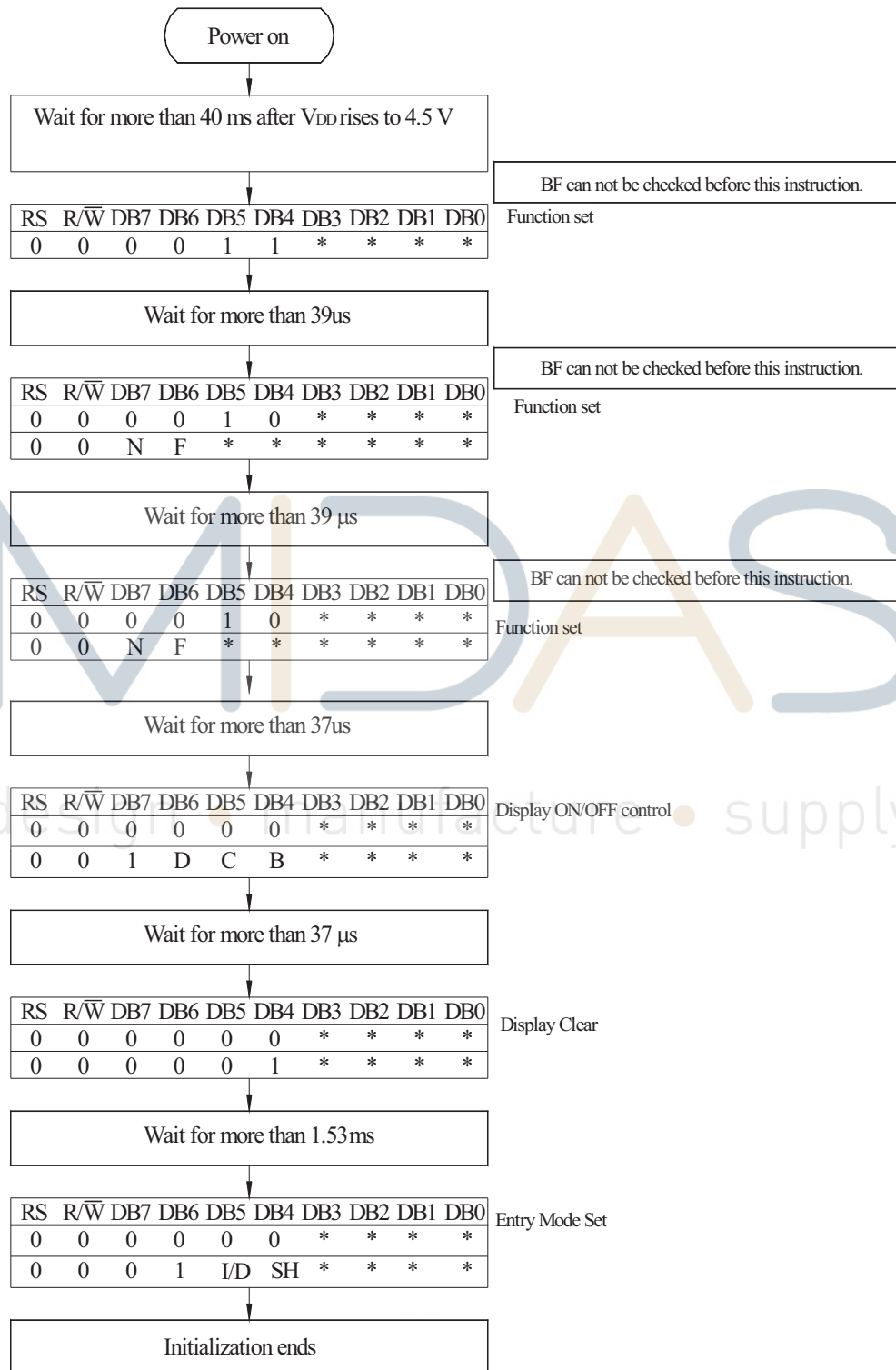
### 13.3 Timing Diagram of VDD Against V0.

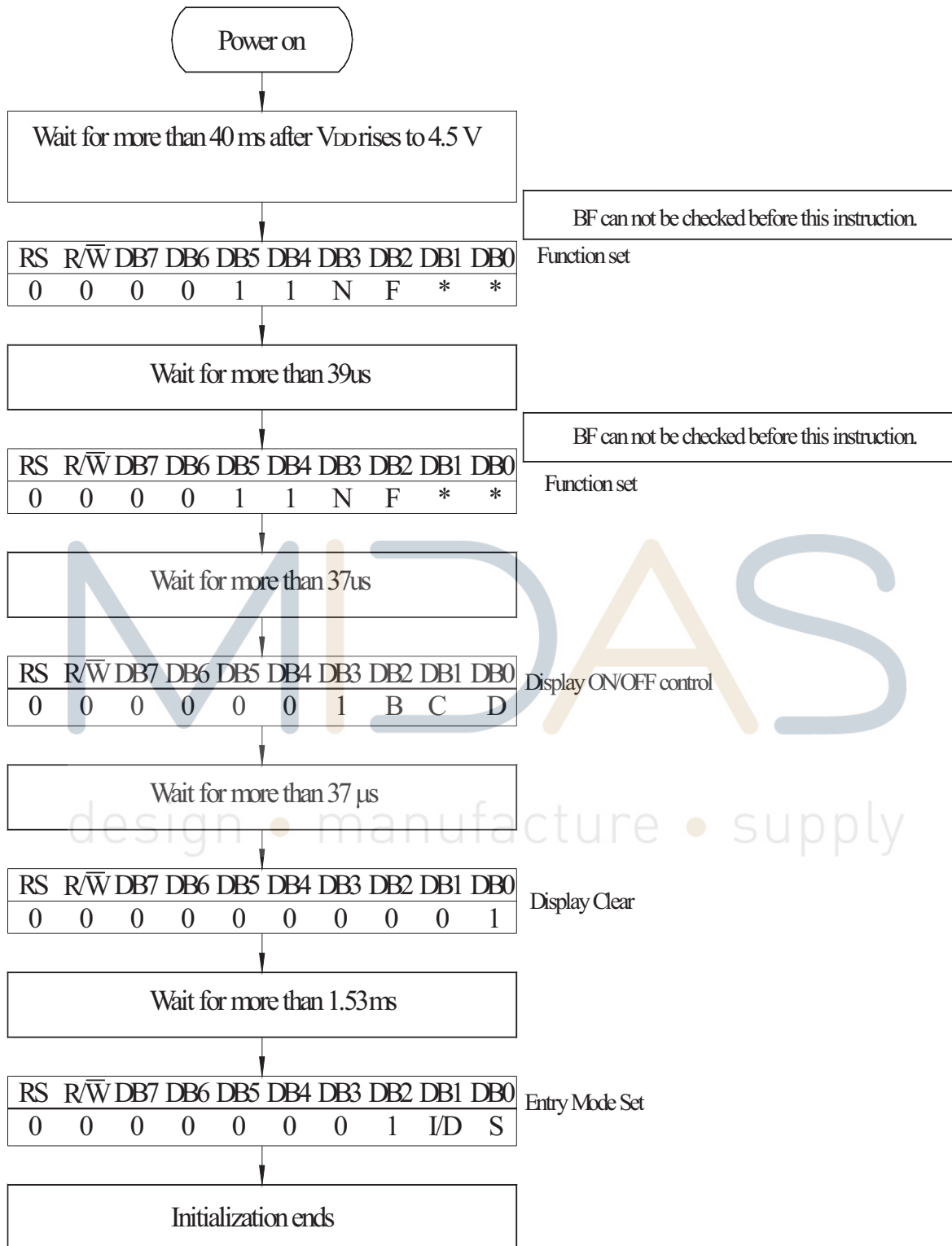
Power on sequence shall meet the requirement of Figure 4, the timing diagram of VDD against V0.



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# 14.Initializing of LCM





8-Bit Ineterface

## 15.Quality Assurance

### Screen Cosmetic Criteria

Item	Defect	Judgment Criterion	Partition																				
1	Spots	A)Clear <table><tr><th>Size: d mm</th><th>Acceptable Qty in active area</th></tr><tr><td><math>d \leq 0.1</math></td><td>Disregard</td></tr><tr><td><math>0.1 &lt; d \leq 0.2</math></td><td>6</td></tr><tr><td><math>0.2 &lt; d \leq 0.3</math></td><td>2</td></tr><tr><td><math>0.3 &lt; d</math></td><td>0</td></tr></table> <p>Note: Including pin holes and defective dots which must be within one pixel size.</p> <p>B)Unclear <table><tr><th>Size: d mm</th><th>Acceptable Qty in active area</th></tr><tr><td><math>d \leq 0.2</math></td><td>Disregard</td></tr><tr><td><math>0.2 &lt; d \leq 0.5</math></td><td>6</td></tr><tr><td><math>0.5 &lt; d \leq 0.7</math></td><td>2</td></tr><tr><td><math>0.7 &lt; d</math></td><td>0</td></tr></table></p>	Size: d mm	Acceptable Qty in active area	$d \leq 0.1$	Disregard	$0.1 < d \leq 0.2$	6	$0.2 < d \leq 0.3$	2	$0.3 < d$	0	Size: d mm	Acceptable Qty in active area	$d \leq 0.2$	Disregard	$0.2 < d \leq 0.5$	6	$0.5 < d \leq 0.7$	2	$0.7 < d$	0	Minor
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2	Bubbles in Polarizer	<table><tr><th>Size: d mm</th><th>Acceptable Qty in active area</th></tr><tr><td><math>d \leq 0.3</math></td><td>Disregard</td></tr><tr><td><math>0.3 &lt; d \leq 1.0</math></td><td>3</td></tr><tr><td><math>1.0 &lt; d \leq 1.5</math></td><td>1</td></tr><tr><td><math>1.5 &lt; d</math></td><td>0</td></tr></table>	Size: d mm	Acceptable Qty in active area	$d \leq 0.3$	Disregard	$0.3 < d \leq 1.0$	3	$1.0 < d \leq 1.5$	1	$1.5 < d$	0	Minor										
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3	Scratch	In accordance with spots cosmetic criteria. When the light reflects on the panel surface, the scratches are not to be remarkable.	Minor																				
4	Allowable Density	Above defects should be separated more than 30mm each other.	Minor																				
5	Coloration	Not to be noticeable coloration in the viewing area of the LCD panels. Back-light type should be judged with back-light on state only.	Minor																				

design • manufacture • supply

# 16. Reliability

## Content of Reliability Test

Environmental Test			
Test Item	Content of Test	Test Condition	Applicable Standard
High Temperature storage	Endurance test applying the high storage temperature for a long time.	60°C 96hrs	—
Low Temperature storage	Endurance test applying the high storage temperature for a long time.	-10°C 96hrs	—
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	50°C 96hrs	—
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	0°C 96hrs	—
High Temperature/ Humidity Storage	Endurance test applying the high temperature and high humidity storage for a long time.	60°C, 90%RH 96hrs	—
High Temperature/ Humidity Operation	Endurance test applying the electric stress (Voltage & Current) and temperature / humidity stress to the element for a long time.	50°C, 90%RH 96hrs	—
Temperature Cycle	Endurance test applying the low and high temperature cycle. <div style="text-align: center;"> <p>-10°C      25°C      60°C 30min      5min      30min 1 cycle</p> </div>	-10°C/60°C 10 cycles	—
Mechanical Test			
Vibration test	Endurance test applying the vibration during transportation and using.	10~22Hz→1.5mmp-p 22~500Hz→1.5G Total 0.5hrs	—
Shock test	Constructional and mechanical endurance test applying the shock during transportation.	50G Half sign wave 11 msdc 3 times of each direction	—

\*\*\*Supply voltage for logic system=5V. Supply voltage for LCD system =Operating voltage at 25°C