

HEF4521B

24-stage frequency divider and oscillator

Rev. 7 — 30 March 2016

Product data sheet

1. General description

The HEF4521B consists of a chain of 24 toggle flip-flops with an overriding asynchronous master reset input (MR), and an input circuit that allows three modes of operation. The single inverting stage (A2 to Y2) functions as: a crystal oscillator, an input buffer for an external oscillator or in combination with A1 as an RC oscillator. The crystal oscillator operates in Low-power mode when pins V_{SS1} and V_{DD1} are supplied via external resistors.

Each flip-flop divides the frequency of the previous flip-flop by two, consequently the HEF4521B counts up to $2^{24} = 16777216$. The counting advances on the HIGH-to-LOW transition of the clock (A2). The outputs from each of the last seven stages (2^{18} to 2^{24}) are available for additional flexibility.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

2. Features and benefits

- Low power crystal oscillator operation
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B

3. Ordering information

Table 1. Ordering information

All types operate from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$.

Type number	Package		
	Name	Description	Version
HEF4521BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1



4. Functional diagram

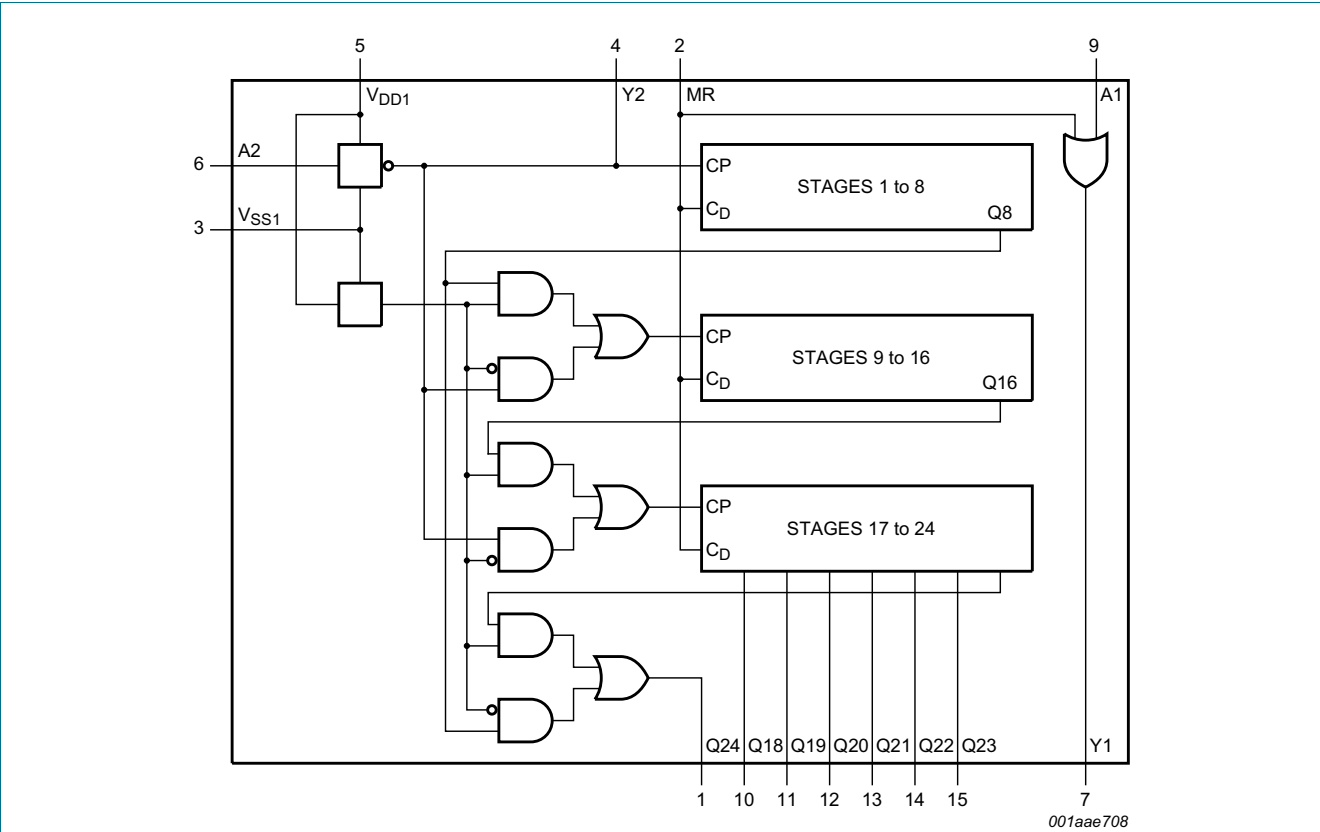


Fig 1. Functional diagram

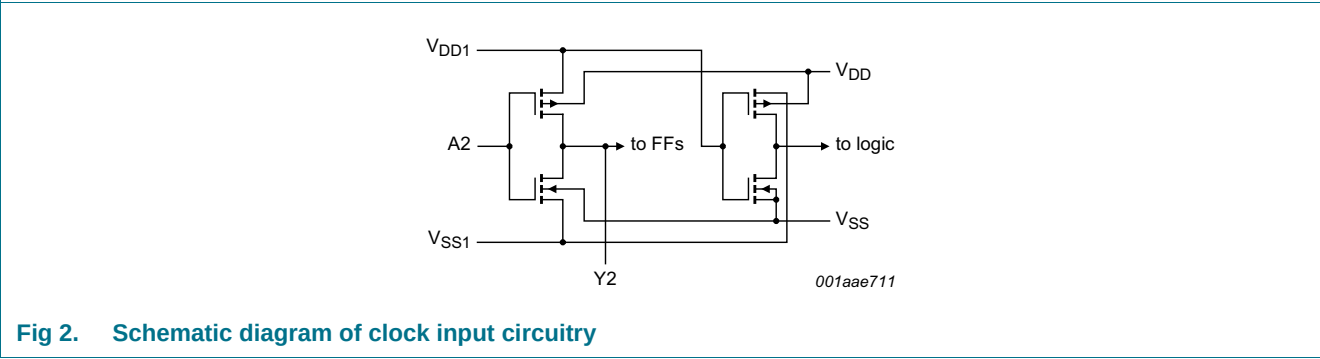


Fig 2. Schematic diagram of clock input circuitry

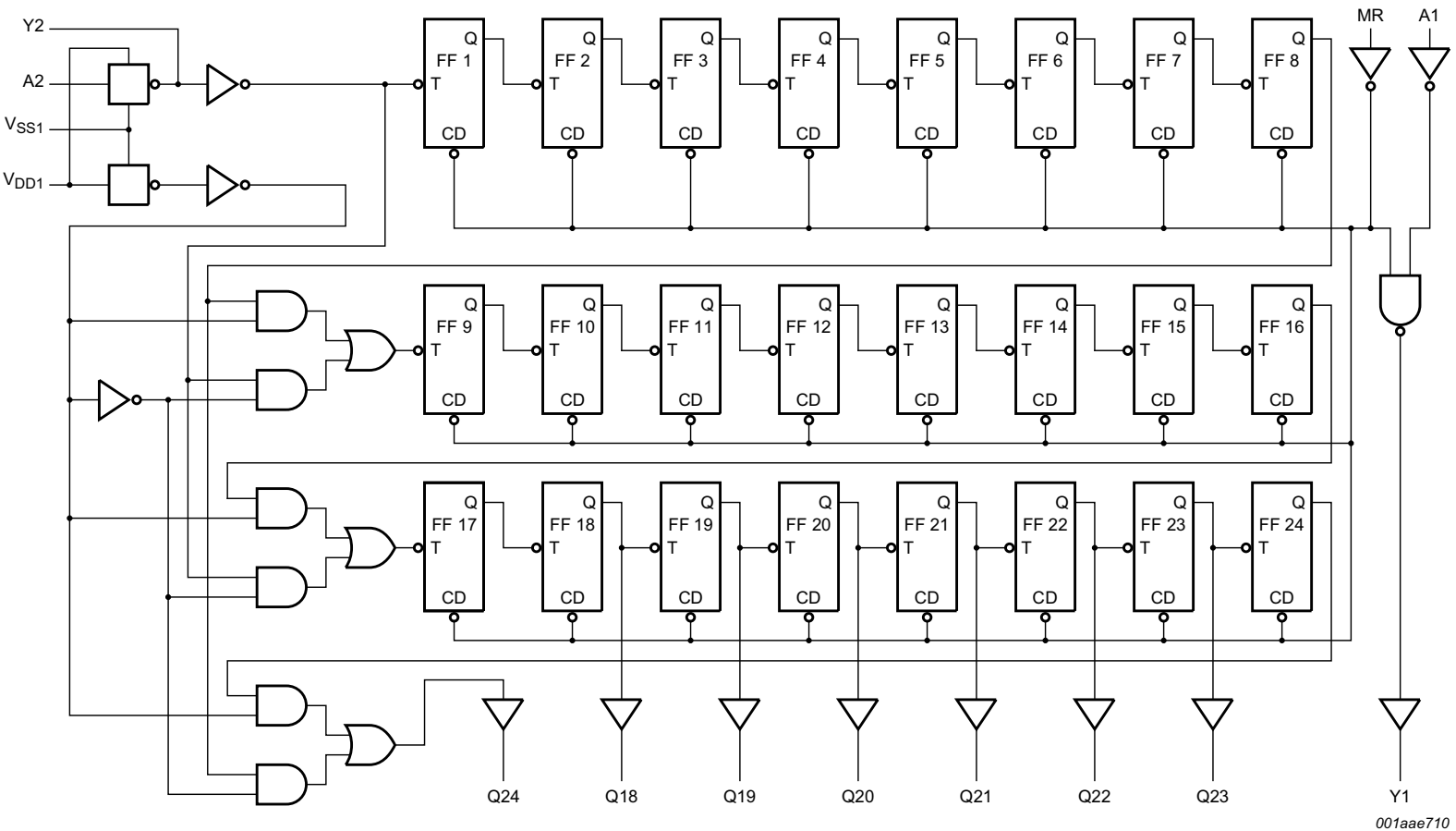


Fig 3. Logic diagram

5. Pinning information

5.1 Pinning

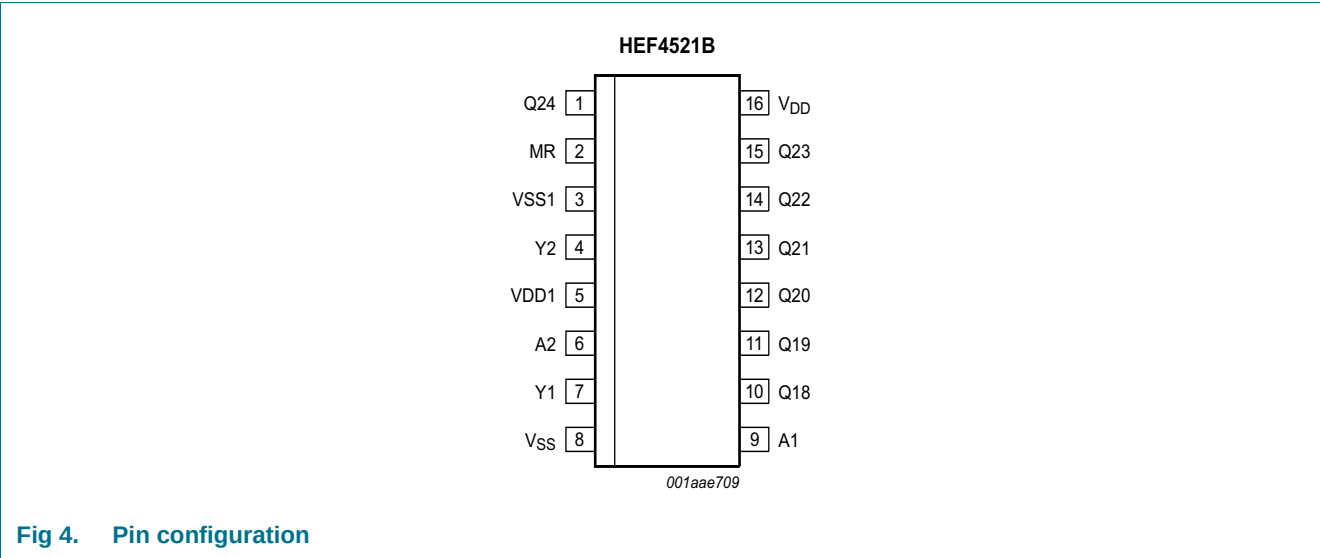


Fig 4. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
MR	2	master reset input
V _{SS1}	3	ground supply voltage 1
V _{DD1}	5	supply voltage 1
Y1, Y2	7, 4	external oscillator connection
V _{SS}	8	ground supply voltage
A1, A2	9, 6	external oscillator connection
Q18 to Q24	10, 11, 12, 13, 14, 15, 1	output
V _{DD}	16	supply voltage

6. Count capacity

Table 3. Count capacity

Output	Count capacity
Q18	2 ¹⁸ = 262 144
Q19	2 ¹⁹ = 524 288
Q20	2 ²⁰ = 1 048 576
Q21	2 ²¹ = 2 097 152
Q22	2 ²² = 4 194 304
Q23	2 ²³ = 8 388 608
Q24	2 ²⁴ = 16 777 216

7. Functional test

A test function has been included to reduce the test time required to test all 24 counter stages. This test function divides the counter into three 8-stage sections by connecting V_{SS1} to V_{DD} and V_{DD1} to V_{SS} . 255 counts are loaded into each of the 8-stage sections in parallel via A2 (connected to Y2). All flip-flops are now at a HIGH level. The counter is now returned to the normal 24-stage in series configuration by connecting V_{SS1} to V_{SS} and V_{DD1} to V_{DD} . Entering one more pulse into input A2 causes the counter to ripple from an all HIGH state to an all LOW state.

Table 4. Functional test sequence^[1]

Inputs		Control terminals			Outputs	Remarks
MR	A2	Y2	V_{SS1}	V_{DD1}	Q18 to Q24	
H	L	L	V_{DD}	V_{SS}	L	counter is in three 8-stage sections in parallel mode; A2 and Y2 are interconnected (Y2 is now input); counter is reset by MR.
L	^[2]	^[2]	V_{DD}	V_{SS}	H	
L	L	L	V_{SS}	V_{SS}	H	V_{SS1} is connected to V_{SS} .
L	H	L	V_{SS}	V_{SS}	H	the input A2 is made HIGH.
L	H	L	V_{SS}	V_{DD}	H	V_{DD1} is connected to V_{DD} ; Y2 is now made floating and becomes an output; the device is now in the 2 ²⁴ mode.
L	↓		V_{SS}	V_{DD}	L	counter ripples from an all HIGH state to an all LOW state.

[1] H = HIGH voltage level; L = LOW voltage level; ↓ = HIGH to LOW transition.

[2] 255 pulses are clocked into A2, Y2. The counter advances on the LOW to HIGH transition.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{DD} + 0.5\text{ V}$	-	±10	mA
V_I	input voltage		-0.5	$V_{DD} + 0.5$	V
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{DD} + 0.5\text{ V}$	-	±10	mA
$I_{I/O}$	input/output current		-	±10	mA
I_{DD}	supply current	to any supply terminal	-	±100	mA
T_{stg}	storage temperature		-65	+150	°C
T_{amb}	ambient temperature		-40	+85	°C
P_{tot}	total power dissipation	SO16 package ^[1]	-	500	mW
P	power dissipation	per output	-	100	mW

[1] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10\text{ V}$	-	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15\text{ V}$	-	-	0.08	$\mu\text{s/V}$

10. Static characteristics

Table 7. Static characteristics

$V_{SS} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	$T_{amb} = -40\text{ °C}$		$T_{amb} = 25\text{ °C}$		$T_{amb} = 85\text{ °C}$		Unit
				Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	$V_O = 2.5\text{ V}$	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		$V_O = 4.6\text{ V}$	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		$V_O = 9.5\text{ V}$	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		$V_O = 13.5\text{ V}$	15 V	-	-3.6	-	-3.0	-	-2.4	mA
I_{OL}	LOW-level output current	$V_O = 0.4\text{ V}$	5 V	0.52	-	0.44	-	0.36	-	mA
		$V_O = 0.5\text{ V}$	10 V	1.3	-	1.1	-	0.9	-	mA
		$V_O = 1.5\text{ V}$	15 V	3.6	-	3.0	-	2.4	-	mA
I_I	input leakage current		15 V	-	± 0.3	-	± 0.3	-	± 1.0	μA
I_{DD}	supply current	$I_O = 0\text{ A}$	5 V	-	20	-	20	-	150	μA
			10 V	-	40	-	40	-	300	μA
			15 V	-	80	-	80	-	600	μA
C_I	input capacitance		-	-	-	-	7.5	-	-	pF

11. Dynamic characteristics

Table 8. Dynamic characteristics

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; for test circuits see [Figure 6](#); unless otherwise specified.

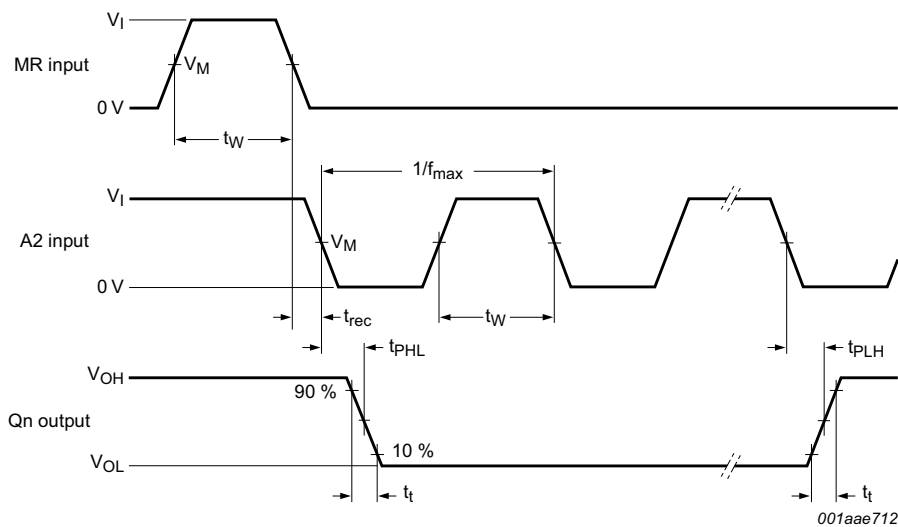
Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	A2 to Q18; see Figure 5	5 V	$923\text{ ns} + (0.55\text{ ns/pF})C_L$	-	950	1900	ns
			10 V	$339\text{ ns} + (0.23\text{ ns/pF})C_L$	-	350	700	ns
			15 V	$212\text{ ns} + (0.16\text{ ns/pF})C_L$	-	220	440	ns
		Qn to Qn + 1; see Figure 5	5 V	$13\text{ ns} + (0.55\text{ ns/pF})C_L$	-	40	80	ns
			10 V	$4\text{ ns} + (0.23\text{ ns/pF})C_L$	-	15	30	ns
			15 V	$2\text{ ns} + (0.16\text{ ns/pF})C_L$	-	10	20	ns
		MR to Qn	5 V	$93\text{ ns} + (0.55\text{ ns/pF})C_L$	-	120	240	ns
			10 V	$44\text{ ns} + (0.23\text{ ns/pF})C_L$	-	55	110	ns
			15 V	$32\text{ ns} + (0.16\text{ ns/pF})C_L$	-	40	80	ns
		A1 to Y1; see Figure 5	5 V	$63\text{ ns} + (0.55\text{ ns/pF})C_L$	-	90	180	ns
			10 V	$24\text{ ns} + (0.23\text{ ns/pF})C_L$	-	35	70	ns
			15 V	$17\text{ ns} + (0.16\text{ ns/pF})C_L$	-	25	50	ns
t_{PLH}	LOW to HIGH propagation delay	A2 to Q18; see Figure 5	5 V	$923\text{ ns} + (0.55\text{ ns/pF})C_L$	-	950	1900	ns
			10 V	$339\text{ ns} + (0.23\text{ ns/pF})C_L$	-	350	700	ns
			15 V	$212\text{ ns} + (0.16\text{ ns/pF})C_L$	-	220	440	ns
		Qn to Qn + 1; see Figure 5	5 V	$13\text{ ns} + (0.55\text{ ns/pF})C_L$	-	40	80	ns
			10 V	$4\text{ ns} + (0.23\text{ ns/pF})C_L$	-	15	30	ns
			15 V	$2\text{ ns} + (0.16\text{ ns/pF})C_L$	-	10	20	ns
		A1 to Y1; see Figure 5	5 V	$33\text{ ns} + (0.55\text{ ns/pF})C_L$	-	60	120	ns
			10 V	$19\text{ ns} + (0.23\text{ ns/pF})C_L$	-	30	60	ns
			15 V	$12\text{ ns} + (0.16\text{ ns/pF})C_L$	-	20	40	ns
t_t	transition time	Qn; see Figure 5	5 V	$10\text{ ns} + (1.00\text{ ns/pF})C_L$	-	60	120	ns
			10 V	$9\text{ ns} + (0.42\text{ ns/pF})C_L$	-	30	60	ns
			15 V	$6\text{ ns} + (0.28\text{ ns/pF})C_L$	-	20	40	ns
t_w	pulse width	A2 HIGH; minimum width; see Figure 5	5 V		80	40	-	ns
			10 V		40	20	-	ns
			15 V		30	15	-	ns
		MR HIGH; minimum width; see Figure 5	5 V		70	35	-	ns
			10 V		40	20	-	ns
			15 V		30	15	-	ns
t_{rec}	recovery time	MR; see Figure 5	5 V		+20	-10	-	ns
			10 V		+15	-5	-	ns
			15 V		15	0	-	ns
f_{max}	maximum frequency	A1; see Figure 5	5 V		6	12	-	MHz
			10 V		12	25	-	MHz
			15 V		17	35	-	MHz

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

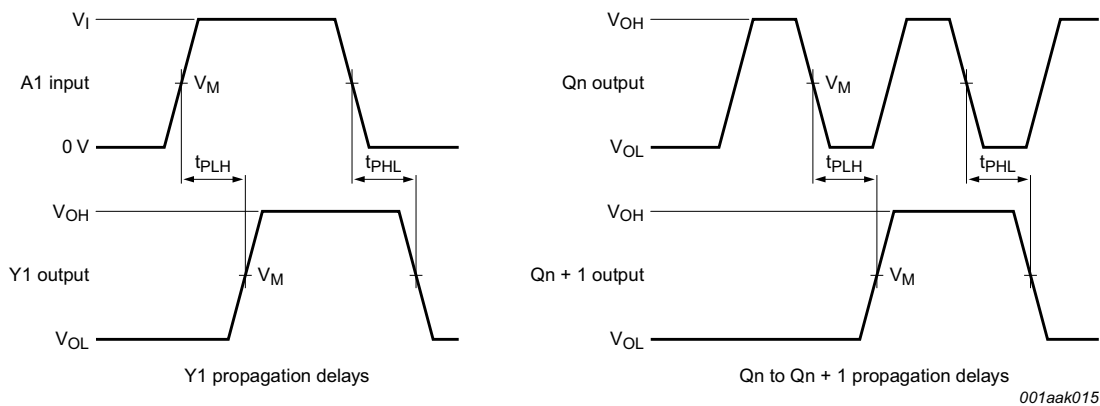
Table 9. Dynamic power dissipation P_D
 P_D can be calculated from the formulas shown. $V_{SS} = 0\text{ V}$; $t_r = t_f \leq 20\text{ ns}$; $T_{amb} = 25\text{ }^\circ\text{C}$.

Symbol	Parameter	V_{DD}	Typical formula for P_D (μW)	where:
P_D	dynamic power dissipation	5 V	$P_D = 1200 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_i = input frequency in MHz, f_o = output frequency in MHz, C_L = output load capacitance in pF, V_{DD} = supply voltage in V, $\Sigma(C_L \times f_o)$ = sum of the outputs.
		10 V	$P_D = 5100 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	
		15 V	$P_D = 13050 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	

12. Waveforms



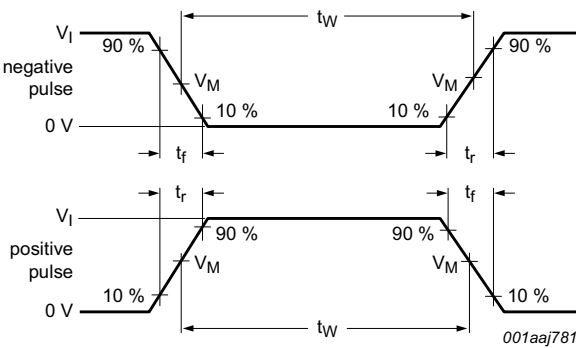
a. Pulse widths, maximum frequency, recovery and transition times and A2 to Qn propagation delays



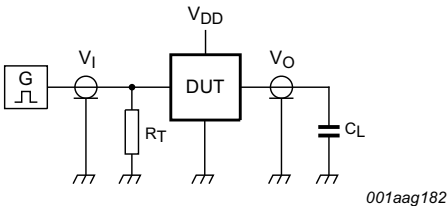
b. A1 to Y1, MR to Qn and Qn to Qn + 1 propagation delays

Measurement points are given in [Table 10](#).
The logic levels V_{OH} and V_{OL} are typical output voltage levels that occur with the output load.

Fig 5. Waveforms showing measurement of dynamic characteristics



a. Input waveforms



b. Test circuit

Test data is given in [Table 10](#).

Definitions for test circuit:

Device Under Test (DUT);

C_L = Load capacitance including jig and probe capacitance;

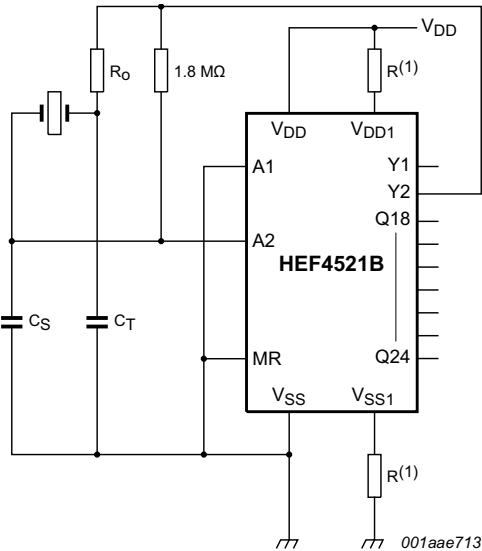
R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig 6. Test circuit for measuring switching times

Table 10. Measurement points and test data

Supply voltage	Input			Load
V_{DD}	V_I	V_M	t_r, t_f	C_L
5 V to 15 V	V_{DD}	$0.5V_I$	≤ 20 ns	50 pF

13. Application information



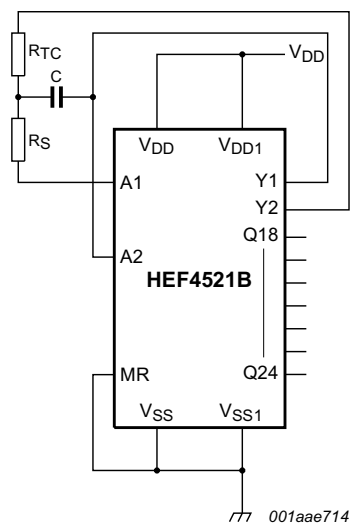
(1) Optional for low power operation.

Fig 7. Crystal oscillator circuit

Table 11. Typical characteristics for crystal oscillator

See Figure 7.

Parameter		500 kHz circuit	50 kHz circuit	Unit
Crystal characteristics				
	Resonance frequency	500	50	kHz
	Crystal cut	S	N	-
	Equivalent resistance; RS	1	6.2	kΩ
External resistor/capacitor values				
	RO	47	750	kΩ
	CT	82	82	pF
	CS	20	20	pF



$$f \approx \frac{1}{2.3 \times R_{TC} \times C} ; R_S \geq 2R_{TC}, \text{ where:}$$

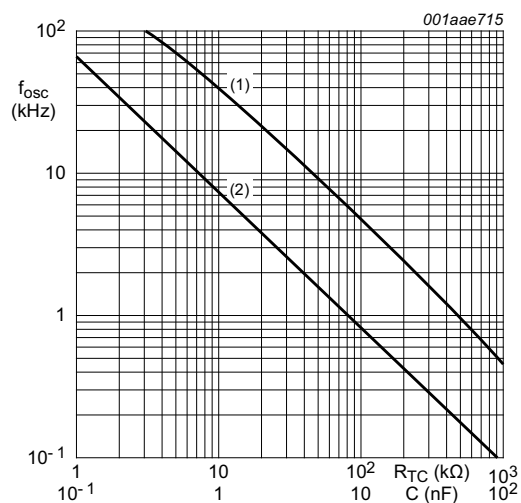
f is in Hz, R is in Ω , and C is in F.

$$R_S + R_{TC} < \frac{V_{IL(max)}}{I_I}, \text{ where:}$$

$V_{IL(max)}$ = maximum input voltage LOW; and

I_1 = input leakage current.

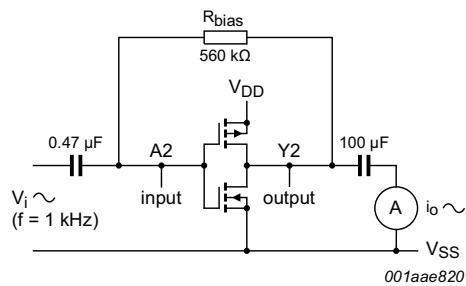
Fig 8. RC oscillator circuit



$V_{DD} = 10\text{ V}$; The test circuit is shown in [Figure 8](#).

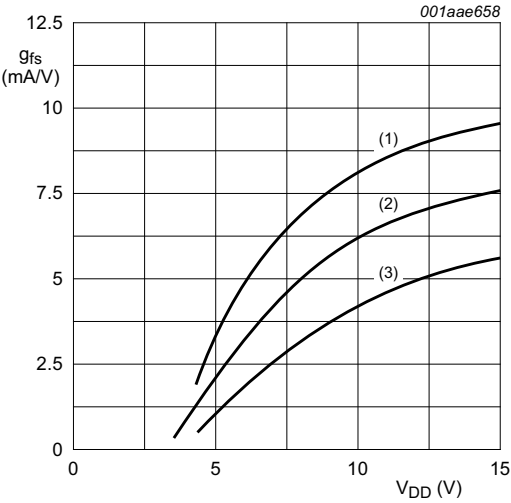
- (1) R_{TC} ; $C = 1 \text{ nF}$; $R_S \approx 2 R_{TC}$.
- (2) C ; $R_{TC} = 56 \text{ k}\Omega$; $R_S = 120 \text{ k}\Omega$.

Fig 9. Oscillator frequency as a function of R_{TC} and C



$g_{fs} = d_{i_o}/d_{v_i}$ with v_o constant (see [Figure 11](#)).

Fig 10. Test setup for measuring forward transconductance



- (1) Average + 2s.
 - (2) Average.
 - (3) Average - 2s.
- Where 's' is the observed standard deviation.

Fig 11. Typical forward transconductance g_{fs} as a function of the supply voltage at $T_{amb} = 25\text{ °C}$

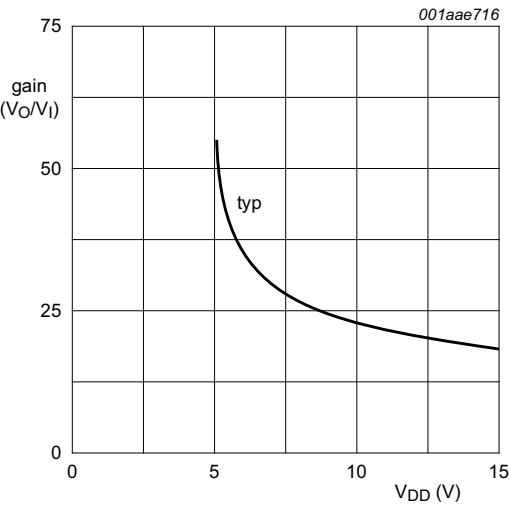


Fig 12. Voltage gain V_o/V_i as a function of supply voltage

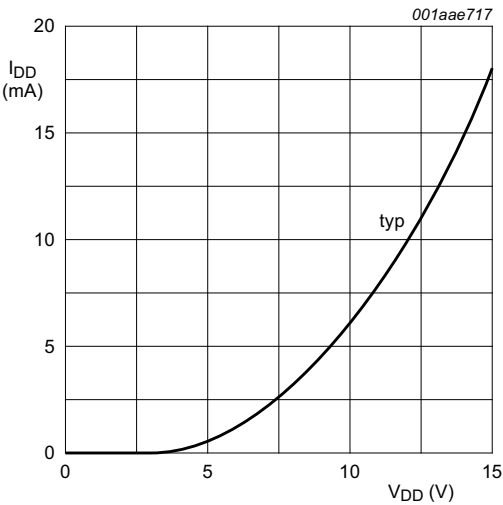


Fig 13. Supply current as a function of supply voltage

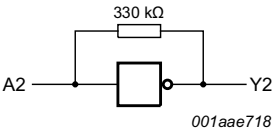


Fig 14. Test setup for measuring the [Figure 12](#) and [Figure 13](#) graphs

14. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

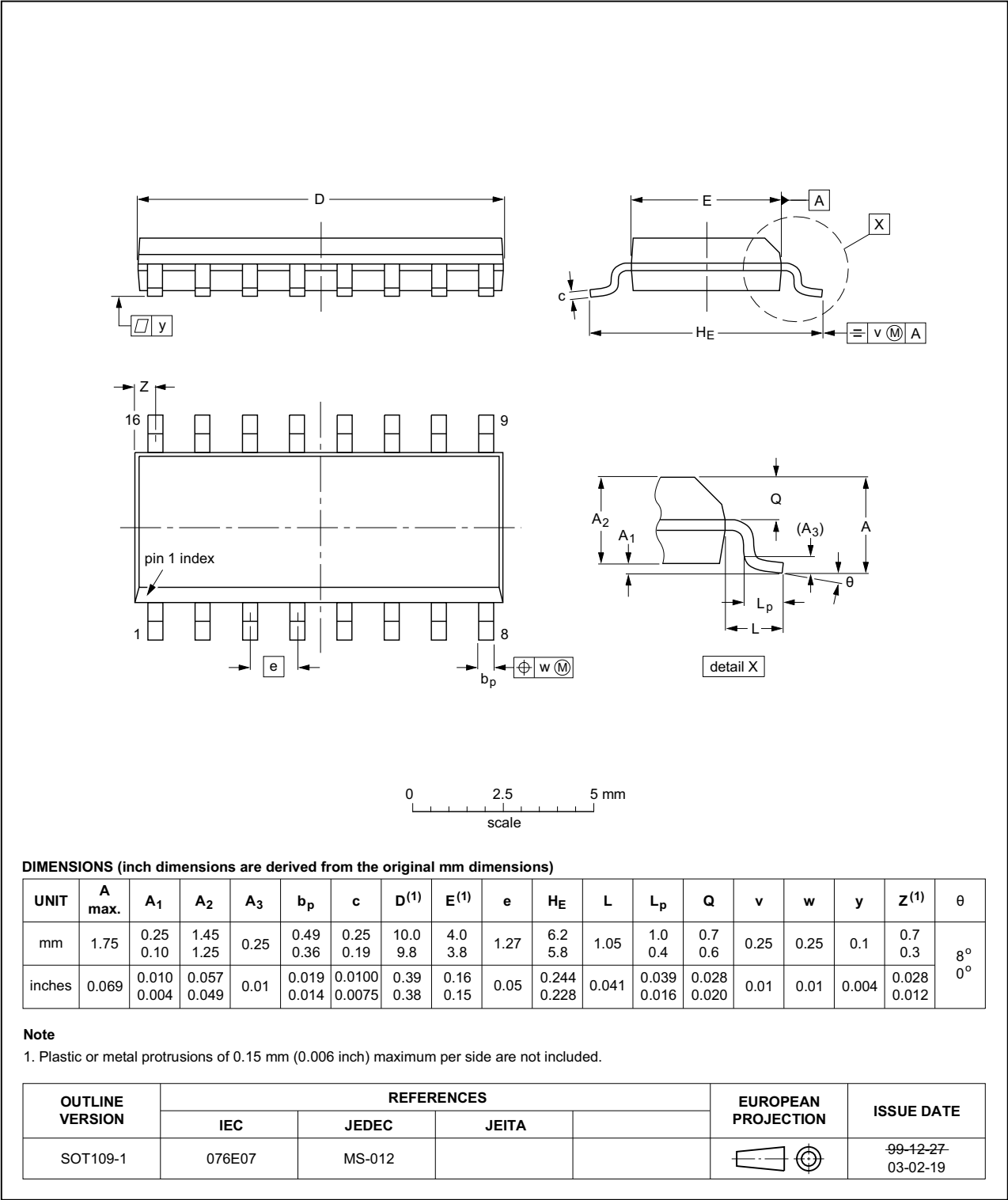


Fig 15. Package outline SOT109-1 (SO16)

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4521B v.7	20160330	Product data sheet	-	HEF4521B v.6
Modifications:	Type number HEF4521BP (SOT38-4) removed.			
HEF4521B v.6	20111121	Product data sheet	-	HEF4521B v.5
Modifications:	- Section Applications removed Table 4: added references to Table note [1] and Table note [2] Table 7: I_{OH} minimum values changed to maximum Figure 11, Figure note [1] and Figure note [3]: space between '2' and 's' removed			
HEF4521B v.5	20091105	Product data sheet	-	HEF4521B v.4
HEF4521B v.4	20090421	Product data sheet	-	HEF4521B_CNV v.3
HEF4521B_CNV v.3	19950101	Product specification	-	HEF4521B_CNV v.2
HEF4521B_CNV v.2	19950101	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

16.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

17. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

18. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	1
4	Functional diagram	2
5	Pinning information	4
5.1	Pinning	4
5.2	Pin description	4
6	Count capacity	4
7	Functional test	5
8	Limiting values	5
9	Recommended operating conditions	6
10	Static characteristics	6
11	Dynamic characteristics	7
12	Waveforms	8
13	Application information	10
14	Package outline	13
15	Revision history	14
16	Legal information	15
16.1	Data sheet status	15
16.2	Definitions	15
16.3	Disclaimers	15
16.4	Trademarks	16
17	Contact information	16
18	Contents	17

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP Semiconductors N.V. 2016.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 30 March 2016

Document identifier: HEF4521B