BGM15HA12

High-Band LNA Multiplexer Module

Data Sheet

Revision 3.0 - 2015-07-24

Power Management & Multimarket

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Revision History

Document No.: BGM15HA12__v3.0.pdf	
Revision History: Rev. v3.0	
Previous Version: Preliminary, Revision v2.4 - 2014-08-21	
Page	**Subjects (major changes since last revision)**
all	“Preliminary” status removed
22	Package Outline Drawing: Minimum package height specified
22	Marking Specification added
23	Footprint Recommendation added

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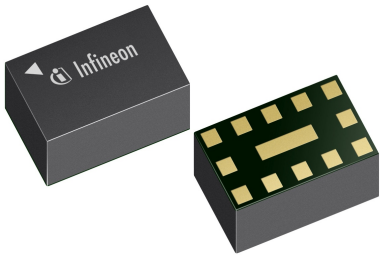
1 Features



- Power gain: 16.3 dB
- Low noise figure: 1.2 dB
- Low current consumption: 4.9 mA
- Frequency range from 2.3 to 2.7 GHz
- RF output internally matched to 50 Ω
- Low external component count
- High port-to-port-isolation
- Suitable for LTE / LTE-Advanced and 3G applications
- No decoupling capacitors required if no DC applied on RF lines
- On chip control logic including ESD protection
- Supply voltage: 2.2 to 3.3 V
- Integrated MIPI RFFE interface operating in 1.1 to 1.95 V voltage range
- Software programmable MIPI RFFE USID
- Small form factor 1.1 mm x 1.9 mm
- High EMI robustness
- RoHS and WEEE compliant package

RoHS

2 Product Description

The BGM15HA12 is a LNA multiplexer module for LTE high-band frequencies that increases the data rate while keeping flexibility and low footprint. It is a perfect solution for multimode handsets based on LTE-Advanced and WCDMA. The device configuration is shown in Fig. 12.

Table 1: Ordering Information

Type	Package	Marking
BGM15HA12	ATSLP-12-3	H3

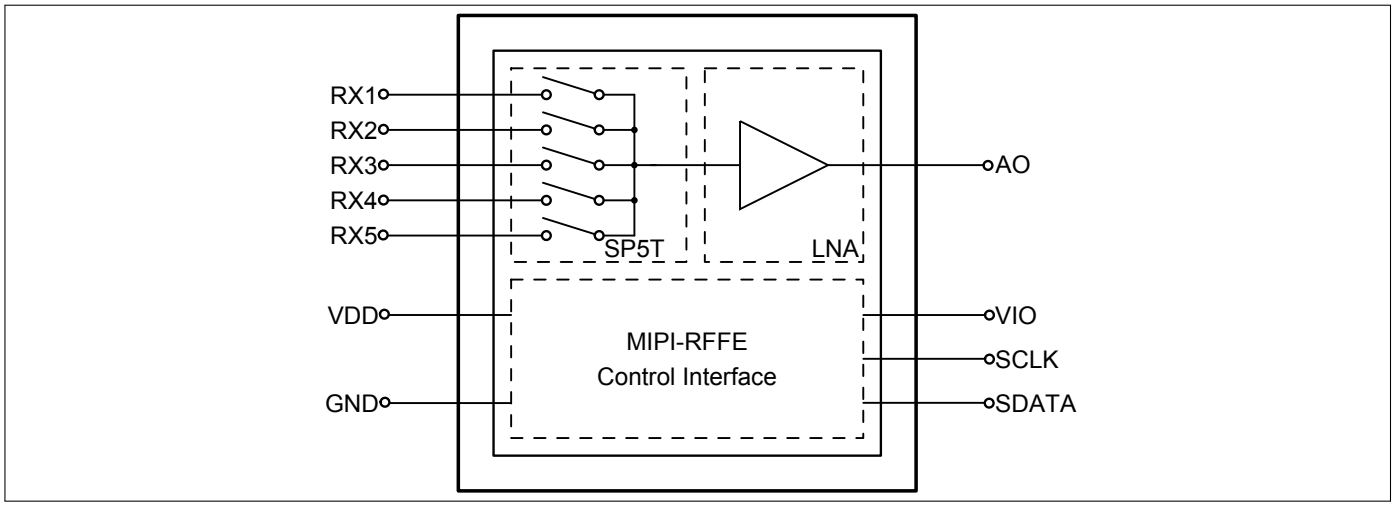


Figure 1: BGM15HA12 Block diagram

3 Maximum Ratings

Table 2: Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply Voltage VDD	V_{DD}	0.3	–	3.6	V	[1]
Voltage at RF pins Rx	V_{Rx}	-0.3	–	0.9	V	–
Voltage at RF output pin AO	V_{AO}	-0.3	–	V_{DD}+0.3	V	–
Voltage at GND pins	V_{GND}	-0.3	–	0.3	V	–
Current into pin VDD	I_{DD}	–	–	16	mA	–
RF input power	P_{IN}	–	–	0	dBm	–
Total power dissipation	P_{tot}	–	–	60	mW	
Junction temperature	T_J	–	–	150	°C	–
Ambient temperature range	T_A	-40	–	85	°C	–
Storage temperature range	T_{STG}	-65	–	150	°C	–
ESD capability, HBM	V_{ESD_HBM}	–	–	1000	V	according to JESD22A-114
RFFE Supply Voltage	V_{IO}	-0.5	–	3.6	V	–
RFFE Supply Voltage Levels	V_{SCLK}, V_{SDATA}	-0.7	–	V_{IO}+0.7 (max. 3.6)	V	–

[1] All voltages refer to GND-Nodes unless otherwise noted

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

4 DC Characteristics

Table 4: RF Characteristics at T_A = 25 °C

Parameter [1]	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply Voltage	V_{DD}	2.2	–	3.3	V	–
Supply Current	I_{DD}	–	4.9	5.9	mA	ON-mode
		–	0.1	2	µA	OFF-Mode
RFFE supply voltage	V_{IO}	1.1	1.8	1.95	V	–
RFFE input high voltage[2]	V_{IH}	0.7*V_{IO}	–	V_{IO}	V	–
RFFE input low voltage[2]	V_{IL}	0	–	0.3*V_{IO}	V	–
RFFE output high voltage[2]	V_{OH}	0.8*V_{IO}	–	V_{IO}	V	–
RFFE output low voltage[2]	V_{OL}	0	–	0.2*V_{IO}	V	–
RFFE control input capacitance	C_{Ctrl}	–	–	2	pF	–
RFFE supply current	I_{VIO}	–	15	–	µA	Idle State

[1] Based on the application described in Chapter 7
[2] SCLK and SDATA

5 RF Characteristics

5.1 BAND 7

Table 5: RF Characteristics Band 7 at T_A = 25 °C, V_{DD} = 2.8 V, f = 2620 – 2690 MHz, with matching described in Chapter 7 (C=1.1 pF, L=2.7 nH)

Parameter [1]	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion power gain[2]	$\|S_{21}\|^2$	13.2	14.7	16.2	dB	–
Noise figure[2]	NF	–	1.2	1.7	dB	Z_S=50 Ω
Input return loss[2] [3]	RL_{in}	10	13	–	dB	–
Output return loss[2] [3]	RL_{out}	10	15	–	dB	–
Reverse isolation AO to RX port[2] [3]	$1/\|S_{12}\|^2$	16	21	–	dB	–
Inband input 1dB-compression point[2] [3]	IP_{1dB}	-10	-7	–	dBm	–
Inband input 3rd-order intercept point[2] [3] [4]	IIP_3	-4	0	–	dBm	f_1=2650 MHz, f_2=2660 MHz, f_{12}=2640 MHz
Isolation RX to RX port[2] [5]	ISO	19	24	–	dB	
Isolation RX to AO port [2] [5]	ISO	7	14	–	dB	forward direction
Stability[5]	k	>1	–	–		f=20 MHz–10 GHz
RF Rise Time RX Port On/Off[5]	$t_{on/off}$	0.5	1	5	µs	10 % to 90 % ON; 90 % to 10 % ON
Power Up Settling Time[5]	t_{BC}	–	10	25	µs	After power down mode

[1] The parameter values are valid at any RX port using the matching described in Chapter 7
[2] PCB losses are subtracted
[3] Verification based on AQL; not 100% tested in production
[4] Input power = –30 dBm for each tone
[5] Guaranteed by device design; not tested in production

5.2 BAND 38

Table 6: RF Characteristics Band 38 at T_A = 25 °C, V_{DD} = 2.8 V, f = 2570 – 2620 MHz, with matching described in Chapter 7 (C=1.0 pF, L=2.7 nH)

Parameter [1]	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion power gain[2]	$\|S_{21}\|^2$	13.4	14.9	16.4	dB	–
Noise figure[2]	NF	–	1.3	1.8	dB	Z_S=50 Ω
Input return loss[2 3]	RL_{in}	9	12	–	dB	–
Output return loss [2 3]	RL_{out}	11	16	–	dB	–
Reverse isolation AO to RX port [2 3]	$1/\|S_{12}\|^2$	17	21	–	dB	–
Inband input 1dB-compression point[2 3]	IP_{1dB}	-10	-7	–	dBm	–
Inband input 3rd-order intercept point[2 3 4]	IIP_3	-4	0	–	dBm	f_1=2590 MHz, f_2=2600 MHz, f_{12}=2580 MHz
Isolation RX to RX port[2 5]	ISO	20	25	–	dB	
Isolation RX to AO port[2 5]	ISO	8	15	–	dB	forward direction
Stability[5]	k	>1	–	–		f=20 MHz–10 GHz
RF Rise Time RX Port On/Off[5]	$t_{on/off}$	0.5	1	5	µs	10 % to 90 % ON; 90 % to 10 % ON
Power Up Settling Time[5]	t_{BC}	–	10	25	µs	After power down mode

[1] The parameter values are valid at any RX port using the matching described in Chapter 7
[2] PCB losses are subtracted
[3] Verification based on AQL; not 100% tested in production
[4] Input power = –30 dBm for each tone
[5] Guaranteed by device design; not tested in production

5.3 BAND 40

Table 7: RF Characteristics Band 40 at T_A = 25 °C, V_{DD} = 2.8 V, f = 2300 – 2400 MHz, with matching described in Chapter 7 (C=1.3 pF, L=2.9 nH)

Parameter [1]	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion power gain[2]	$\|S_{21}\|^2$	14.2	15.7	17.2	dB	–
Noise figure[2]	NF	–	1.35	1.85	dB	Z_S=50 Ω
Input return loss[2 3]	RL_{in}	7	11	–	dB	–
Output return loss[2 3]	RL_{out}	11	15	–	dB	–
Reverse isolation AO to RX port[2 3]	$1/\|S_{12}\|^2$	17	22	–	dB	–
Inband input 1dB-compression point[2 3]	IP_{1dB}	-11	-8	–	dBm	–
Inband input 3rd-order intercept point[2 3 4]	IIP_3	-6	-2	–	dBm	f_1=2345 MHz, f_2=2355 MHz, f_{12}=2335 MHz
Isolation RX to RX port[2 5]	ISO	19	24	–	dB	
Isolation RX to AO port[2 5]	ISO	7	14	–	dB	forward direction
Stability[5]	k	>1	–	–		f=20 MHz–10 GHz
RF Rise Time RX Port On/Off[5]	$t_{on/off}$	0.5	1	5	µs	10 % to 90 % ON; 90 % to 10 % ON
Power Up Settling Time[5]	t_{BC}	–	10	25	µs	After power down mode

[1] The parameter values are valid at any RX port using the matching described in Chapter 7
[2] PCB losses are subtracted
[3] Verification based on AQL; not 100% tested in production
[4] Input power = –30 dBm for each tone
[5] Guaranteed by device design; not tested in production

6 MIPI RFFE Specification

All sequences are implemented according to the 'MIPI Alliance Specification for RF Front-End Control Interface' document version 1.10 - 26. July 2011.

Table 8: MIPI Features

Feature	Supported	Comment
Register write command sequence	Yes	
Register read command sequence	Yes	
Extended register write command sequence	No	Up to 4 Bytes
Extended register read command sequence	No	Up to 4 Bytes
Register 0 write command sequence	Yes	
Trigger function	Yes	Trigger assignment to each control register is supported
Programmable USID	Yes	3 register command sequence and extended register command sequence
Status Register	Yes	Register for debugging
Reset	Yes	By VIO, Power Mode and RFFE_STATUS
Group SID	Yes	
USID_Sel pin	No	External pin for changing USID is not implemented
Full speed write	Yes	
Half speed read	Yes	
Full speed read	Yes	

Table 9: Startup Behavior

Feature	State	Comment
Power status	LOW POWER	The chip is in low power mode after startup
Trigger function	ENABLED	Trigger function is enabled after startup. Trigger function can be disabled via PM_TRIG register.

Table 10: MIPI RFFE Operating Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLK Frequency	FSCLK	0.032	–	26	MHz	Full speed
		0.032	–	13	MHz	Half speed
SCLK Period	TSCLK	0.038	–	32	µs	Full speed
		0.077	–	32	µs	Half speed
SCLK Low Period	TSCLKIL	11.25	–	–	ns	Full speed, see Fig. 2
		24	–	–	ns	Half speed, see Fig. 2
SCLK High Period	TSCLKIH	11.25	–	–	ns	Full speed, see Fig. 2
		24	–	–	ns	Half speed, see Fig. 2
SDATA Setup Time	TS	1	–	–	ns	Full speed, see Fig. 3
		2	–	–	ns	Half speed, see Fig. 3
SDATA Hold Time	TH	5	–	–	ns	Full speed, see Fig. 3
		5	–	–	ns	Half speed, see Fig. 3
SDATA Release Time	TSDATAZ	–	–	10	ns	Full speed, see Fig. 4
		–	–	18	ns	Half speed, see Fig. 4
Time for Data Output	TD	–	–	10.25	ns	Full speed, see Fig. 5
		–	–	22	ns	Half speed, see Fig. 5
SDATA Rise/Fall Time	TSDATAOTR	2.1	–	6.5	ns	Full speed, see Fig. 5
		2.1	–	10	ns	Half speed, see Fig. 5
VIO Rise Time	TVIO-R	10	–	450	µs	See Fig. 6
VIO Reset Time	TVIO-RST	10	–	–	µs	See Fig. 6
Reset Delay Time	TSIGOL	0.12	–	–	µs	See Fig. 6

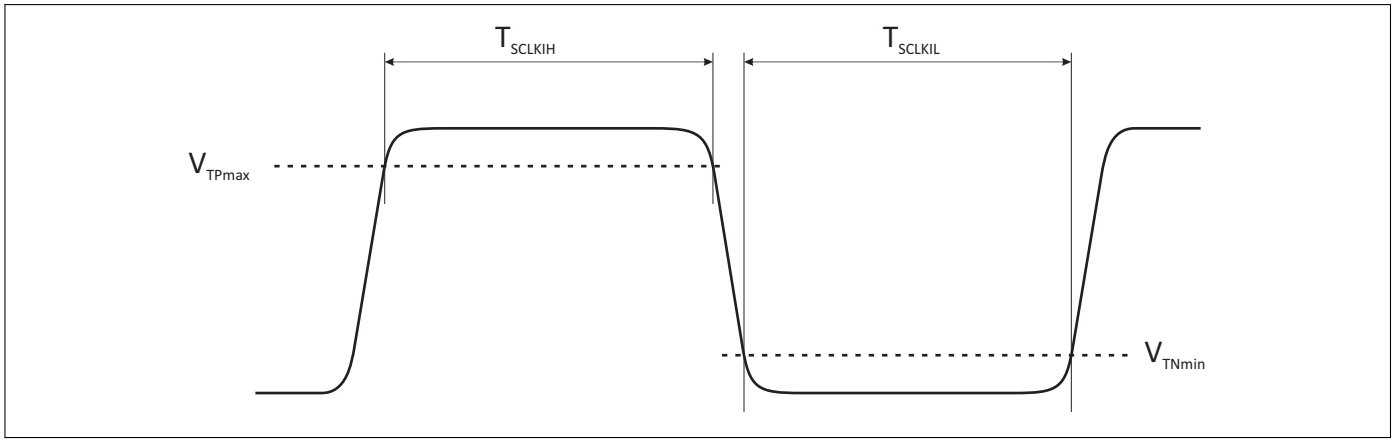


Figure 2: Received clock signal constraints

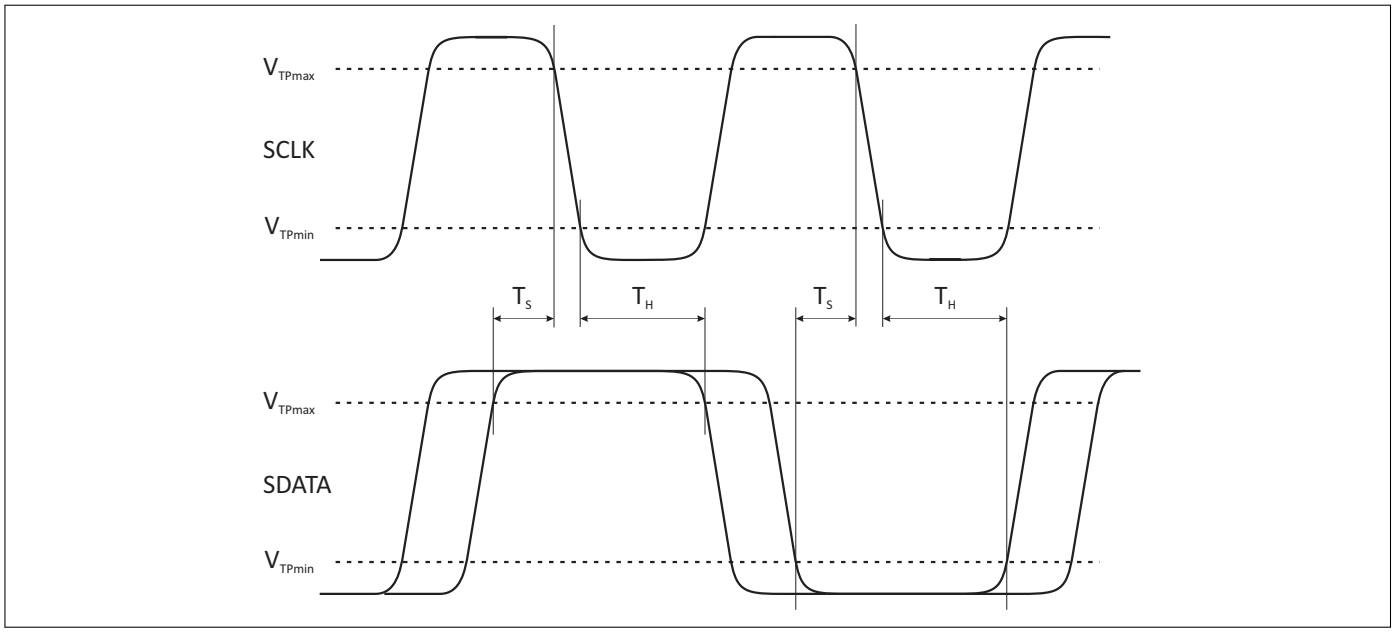


Figure 3: Bus active data receiver timing requirements

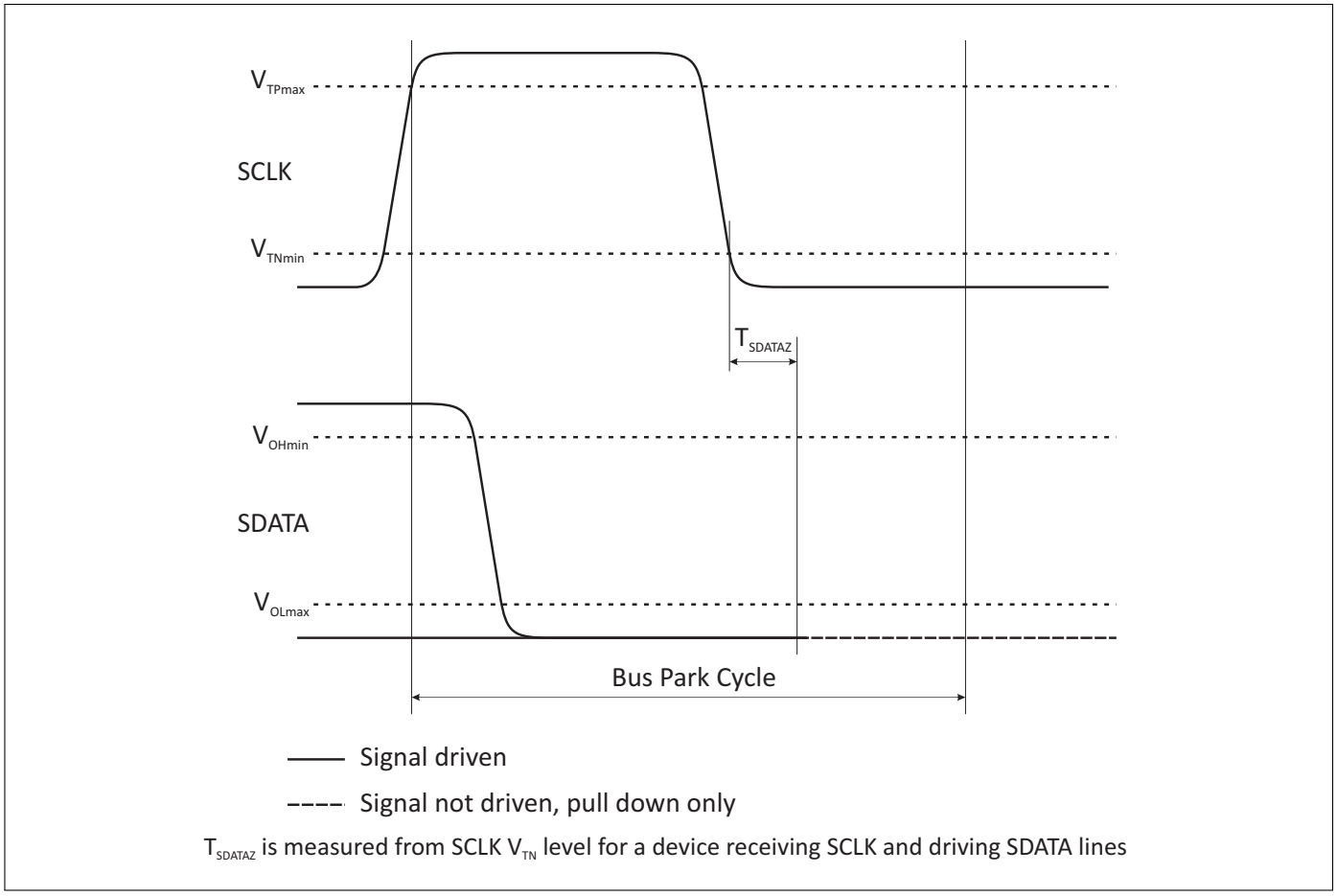


Figure 4: Bus park cycle timing

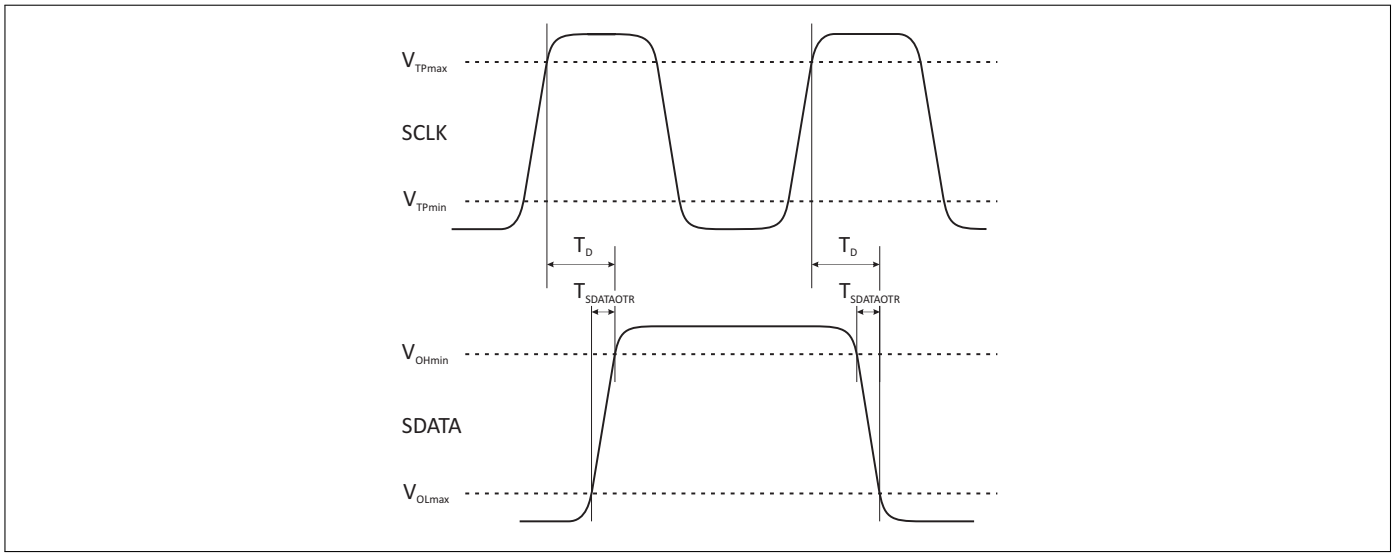


Figure 5: Bus active data transmission timing specification

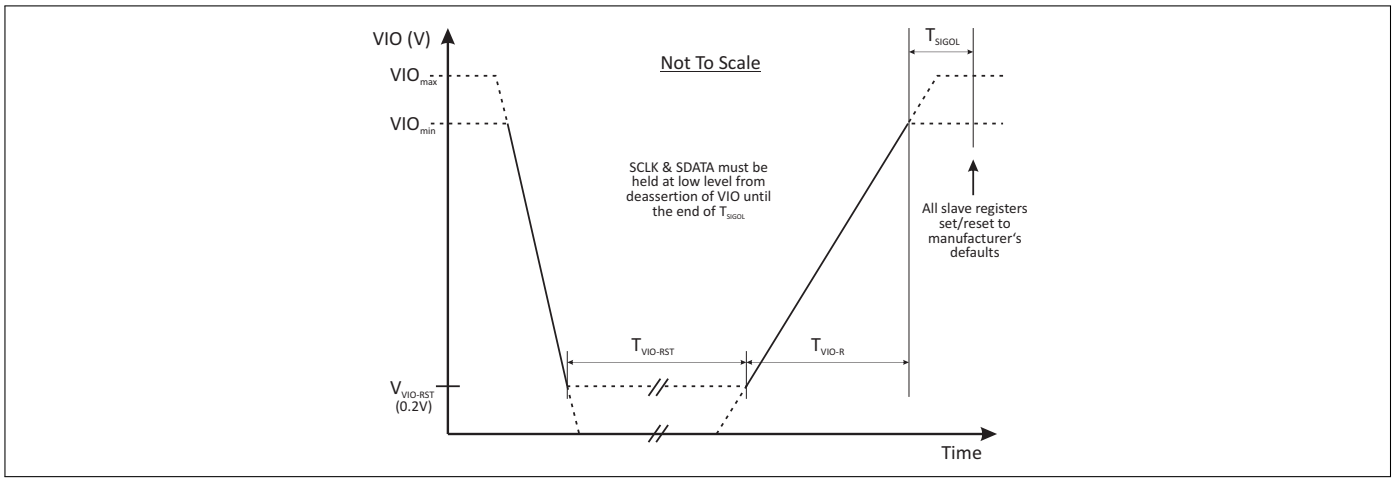


Figure 6: Requirements for VIO-initiated reset

Table 11: Register Mapping

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x0000	REGISTER_0	7:0	MODE_CTRL	Module control	00000000	No	Yes	R/W
0x001D	PRODUCT_ID	7:0	PRODUCT_ID	This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	11010011	No	No	R
0x001E	MANUFACTURER_ID	7:0	MANUFACTURER_ID [7:0]	This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value.	00011010	No	No	R

Continued on next page

Table 11: Register Mapping – Continued from previous page

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x001C	PM_TRIG	7:6	PWR_MODE	00: Normal operation 01: Default settings (STARTUP) 10: Low power (LOW POWER) 11: Reserved	10	Yes	No	R/W
		5	TRIGGER_MASK_2	If this bit is set, trigger 2 is disabled. When all triggers disabled, if writing to a register that is associated to trigger 2, the data goes directly to the destination register.	0	No	No	
		4	TRIGGER_MASK_1	If this bit is set, trigger 1 is disabled. When all triggers disabled, if writing to a register that is associated to trigger 1, the data goes directly to the destination register.	0	No	No	
		3	TRIGGER_MASK_0	If this bit is set, trigger 0 is disabled. When all triggers disabled, if writing to a register that is associated to trigger 0, the data goes directly to the destination register.	0	No	No	
		2	TRIGGER_2	A write of a one to this bit loads trigger 2's registers.	0	Yes	No	
		1	TRIGGER_1	A write of a one to this bit loads trigger 1's registers.	0	Yes	No	R/W
		0	TRIGGER_0	A write of a one to this bit loads trigger 0's registers.	0	Yes	No	
0x001F	MAN_USID	7:6	SPARE	These are read-only bits that are reserved and yield a value of 0b00 at readback.	00	No	No	R/W
		5:4	MANUFACTURER_ID [9:8]	These bits are read-only. However, during the programming of the USID, a write command sequence is performed on this register even though the write does not change its value.	01			
		3:0	USID	Programmable USID. Performing a write to this register using the described programming sequences will program the USID in devices supporting this feature. These bits store the USID of the device.	0011			
0x001A	RFFE_STATUS	7	SOFTWARE RESET	0: Normal operation 1: Software reset	0	No	No	R/W
		6	COMMAND_FRAME_ PARITY_ERR	Command sequence received with parity error - discard command.	0	No	No	R
		5	COMMAND_LENGTH_ERR	Command length error	0			
		4	ADDRESS_FRAME_ PARITY_ERR	Address frame parity error = 1	0			
		3	DATA_FRAME_ PARITY_ERR	Data frame with parity error	0			
		2	READ_UNUSED_REG	Read command to an invalid address	0			
		1	WRITE_UNUSED_REG	Write command to an invalid address	0			
		0	BID_GID_ERR	Read command with a BROADCAST_ID or GROUP_SID	0			
0x001B	GROUP_SID	7:4	RESERVED		0	No	No	R/W
		3:0	GROUP_SID	Group slave ID	0			

Table 12: Modes of Operation (Truth Table, Register_0)

		REGISTER_0 Bits							
State	**Mode**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	Isolation	x	x	x	0	0	0	0	0
2	RX1-AO	x	x	x	0	0	0	0	1
3	RX2-AO	x	x	x	0	0	0	1	0
4	RX3-AO	x	x	x	0	1	0	0	0
5	RX4-AO	x	x	x	0	0	1	0	0
6	RX5-AO	x	x	x	1	0	0	0	0
7	RX1&RX2-AO	x	x	x	0	0	0	1	1
8	RX2&RX3-AO	x	x	x	0	1	0	1	0
9	RX3&RX4-AO	x	x	x	0	1	1	0	0
10	RX4&RX5-AO	x	x	x	1	0	1	0	0
11	RX1&RX3-AO	x	x	x	0	1	0	0	1
12	RX2&RX4-AO	x	x	x	0	0	1	1	0
13	RX3&RX5-AO	x	x	x	1	1	0	0	0
14	RX1&RX4-AO	x	x	x	0	0	1	0	1
15	RX2&RX5-AO	x	x	x	1	0	0	1	0
16	RX1&RX5-AO	x	x	x	1	0	0	0	1

7 Application Information

Pin Configuration and Function

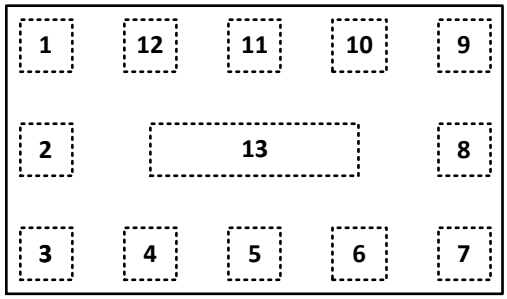


Figure 7: BGM15HA12 Pin Configuration (top view)

Table 13: Pin Definition and Function

Pin No.	Name	Function
1	SCLK	MIPI RFFE Clock
2	VIO	MIPI RFFE Power Supply
3	RX5	RF-Port RX No. 5
4	RX4	RF-Port RX No. 4
5	RX3	RF-Port RX No. 3
6	RX2	RF-Port RX No. 2
7	RX1	RF-Port RX No. 1
8	GND	Ground
9	GND	Ground
10	AO	RF-Output Port
11	VDD	Power Supply
12	SDATA	MIPI RFFE Data IO
13	GND	Ground

Application Board Configuration

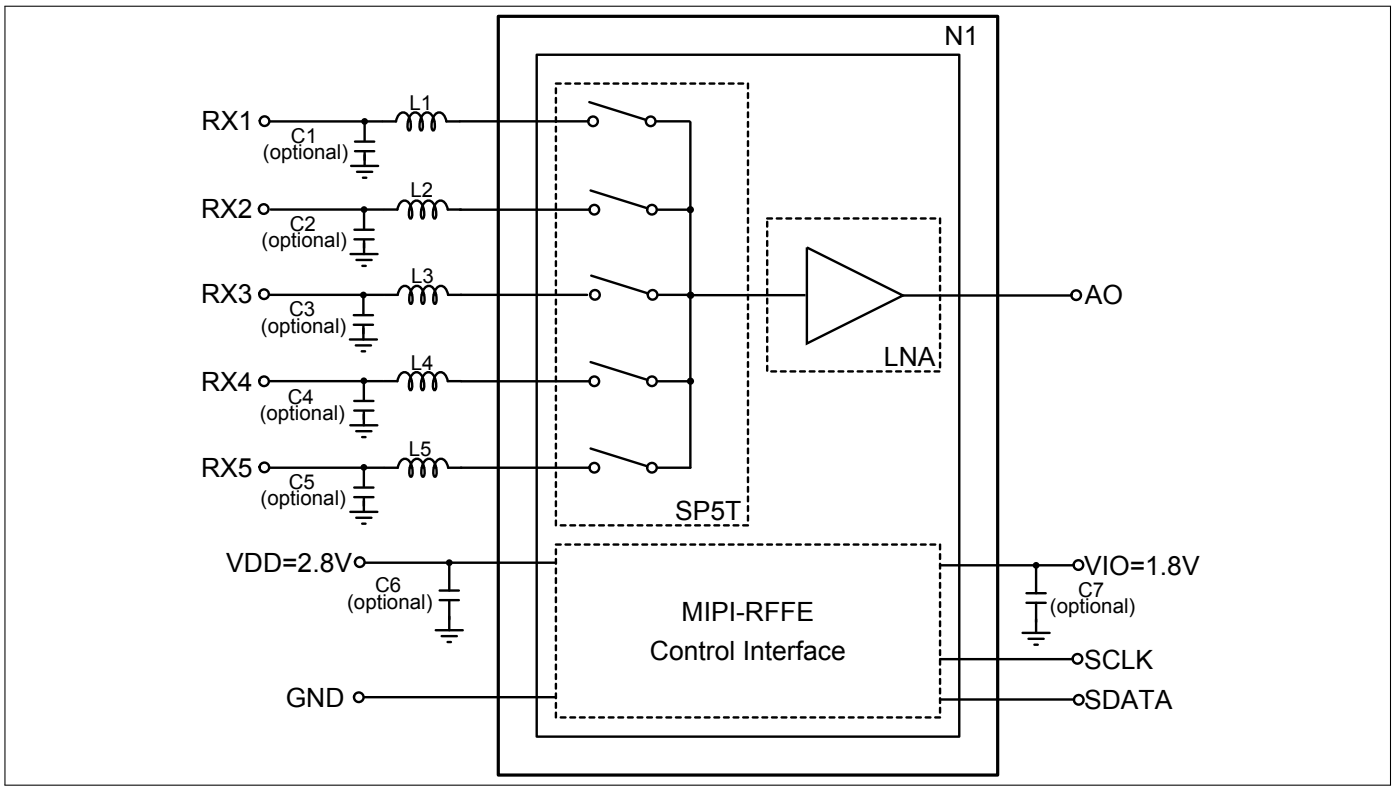


Figure 8: BGM15HA12 Application Schematic

Table 14: Bill of Materials Table

Name	Value	Package	Manufacturer	Function
C1 (optional)	tbd.	tbd.	Various	Input matching[2)]
C2 (optional)	tbd.	tbd.	Various	Input matching[2)]
C3 (optional)	1.3 pF	0402	Various	Input matching Band 40[2)]
C4 (optional)	1.0 pF	0402	Various	Input matching Band 38[2)]
C5 (optional)	1.1 pF	0402	Various	Input matching Band 7[2)]
C6 (optional)	1 nF	0402	Various	RF Bypass[1)]
C7 (optional)	1 nF	0402	Various	RF Bypass[1)]
L1	tbd.	tbd.	Various	Input matching[2)]
L2	tbd.	tbd.	Various	Input matching[2)]
L3	2.9 nH	0402	Various	Input matching Band 40 [2)]
L4	2.7 nH	0402	Various	Input matching Band 38[2)]
L5	2.7 nH	0402	Various	Input matching Band 7[2)]
N1	BGM15HA12	ATSLP-12-3	Infineon	LNA Multiplexer Module

[1)] RF bypass recommended to mitigate power supply noise.
[2)] The matching elements must be optimized with reference to the frequency band of interest. Each band can be arbiratily assigned to an RF port. The configuration shown in the table is only an example of the port assignment.

8 Package Information

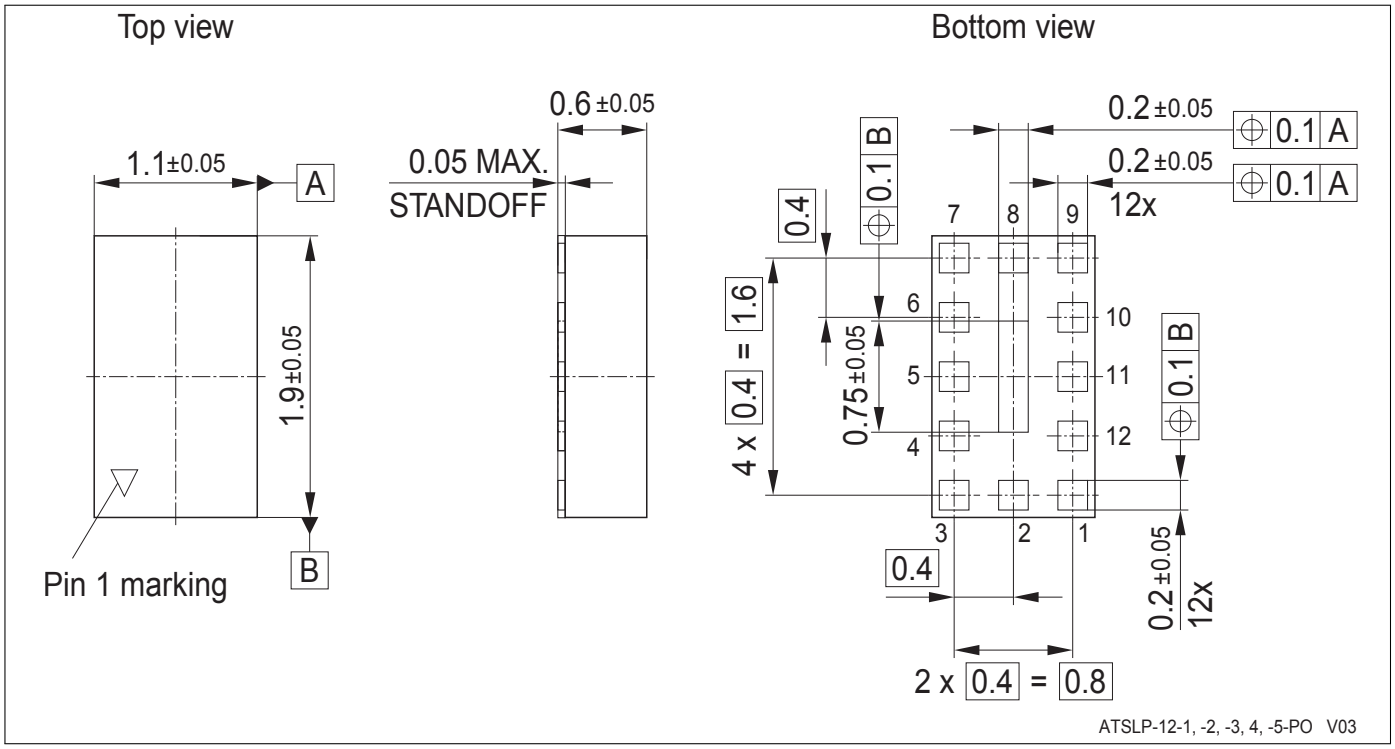


Figure 9: ATSLP-12-3 Package Outline (top, side and bottom views)

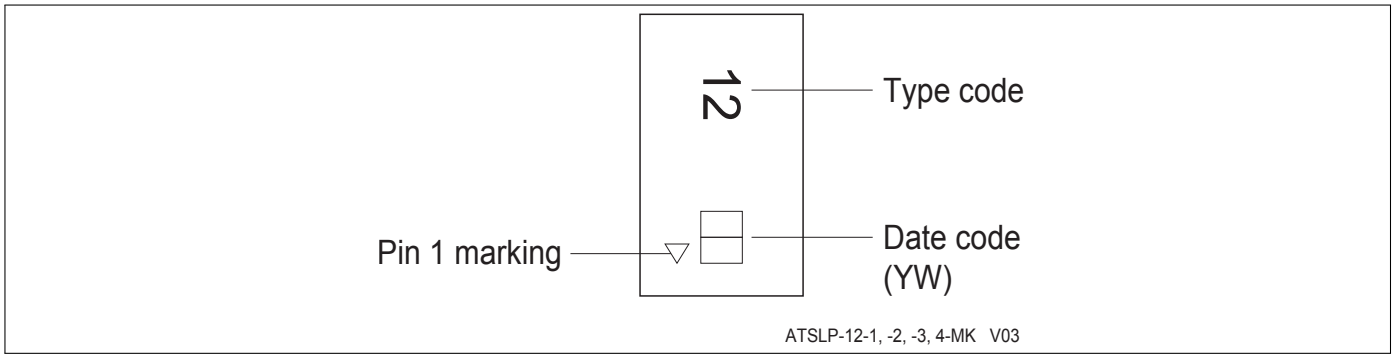


Figure 10: Marking Specification (top view)

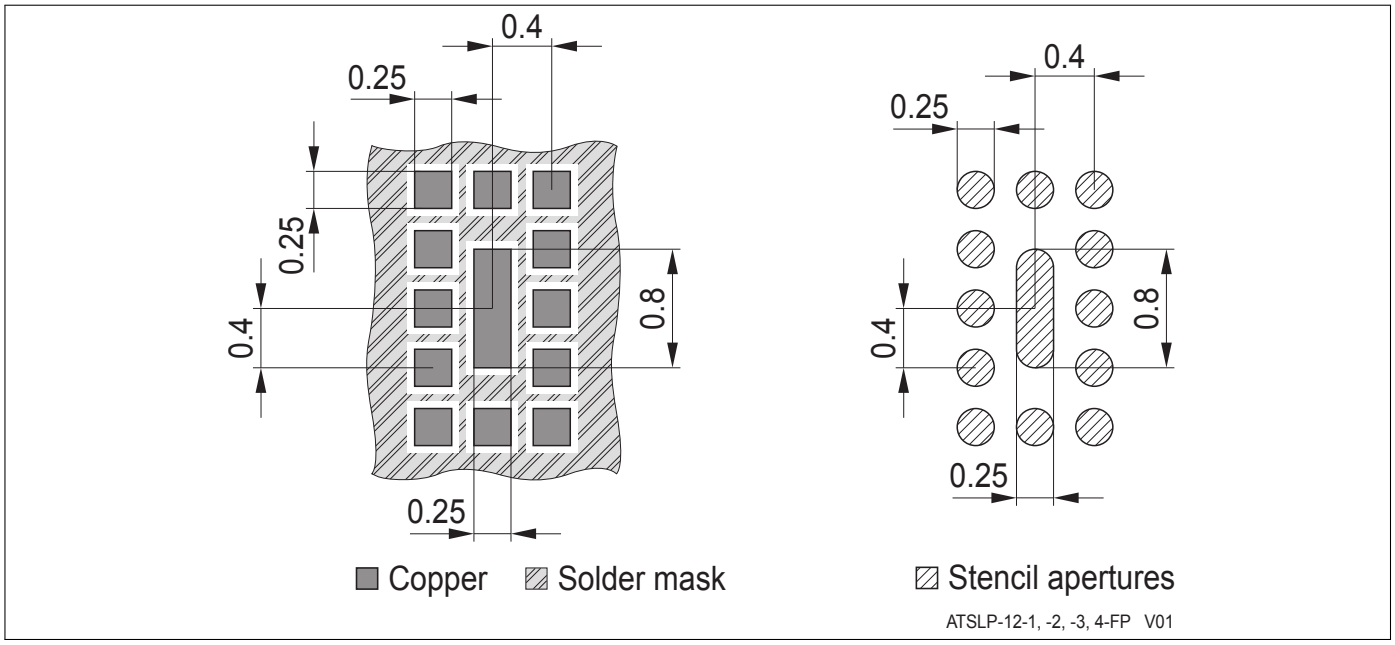


Figure 11: Footprint Recommendation

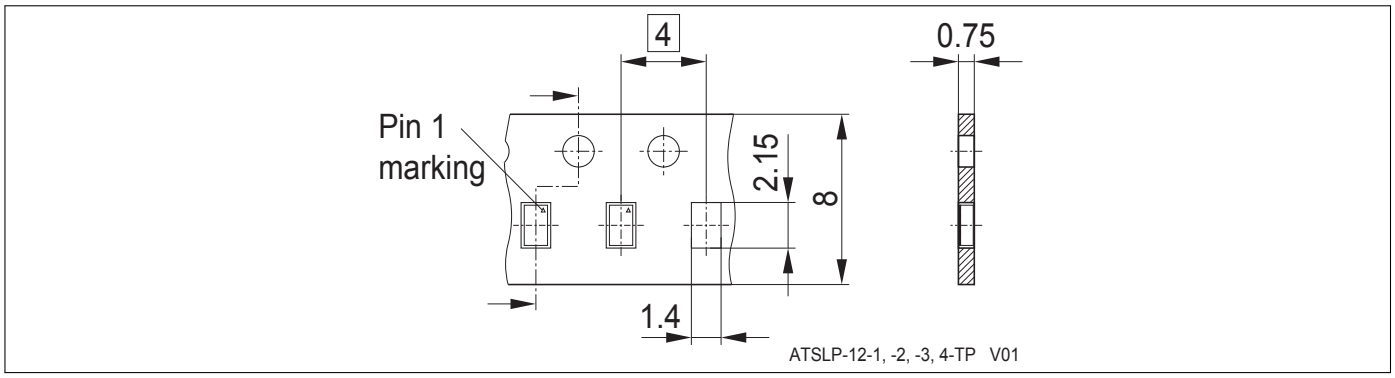


Figure 12: ATSLP-12-3 Carrier Tape

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