BGS1515MN20

RF SP5T + SP5T Antenna Diversity Switch

Data Sheet

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Power Management & Multimarket

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Revision History

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Page	**Subjects (major changes since last revision)**
08	RF Characteristics updated

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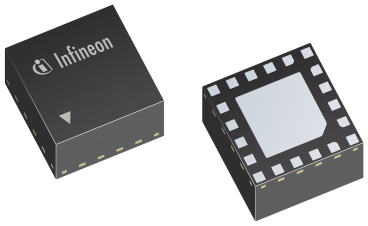
1 Features



- 10 high-linearity Rx paths with LTE and WCDMA power handling capability
- Low insertion loss
- Low harmonic generation
- High port-to-port isolation
- Suitable for Edge / CDMA2000 / LTE / WCDMA applications
- 0.1 to 2.7 GHz coverage
- No decoupling capacitors required if no DC applied on RF lines
- On-chip control logic including ESD protection
- Integrated MIPI RFFE interface operating in 1.1 to 1.95 V voltage range
- Software programmable MIPI RFFE USID
- Direct to battery supply
- Small form factor 2.3 mm x 2.3 mm
- No power supply blocking required
- High EMI robustness
- RoHS and WEEE compliant package

2 Product Description

The BGS1515MN20 is a Dual Pole Ten Throw (SP5T+SP5T) RF switch device optimized for wireless applications up to 2.7 GHz. This RF switch is a perfect solution for multimode handsets based on LTE and WCDMA. The switch device configuration is shown in Fig. 1.

The switch is controlled via a MIPI RFFE controller. The on-chip controller allows power-supply voltages from 1.1 to 1.95 V. The switch features direct-connect-to-battery functionality and DC-free RF ports. Unlike GaAs technology, external DC blocking capacitors at the RF ports are only required if DC voltage is applied externally.

Table 1: Ordering Information

Type	Package	Marking
BGS1515MN20	TSNP-20-1	55M2

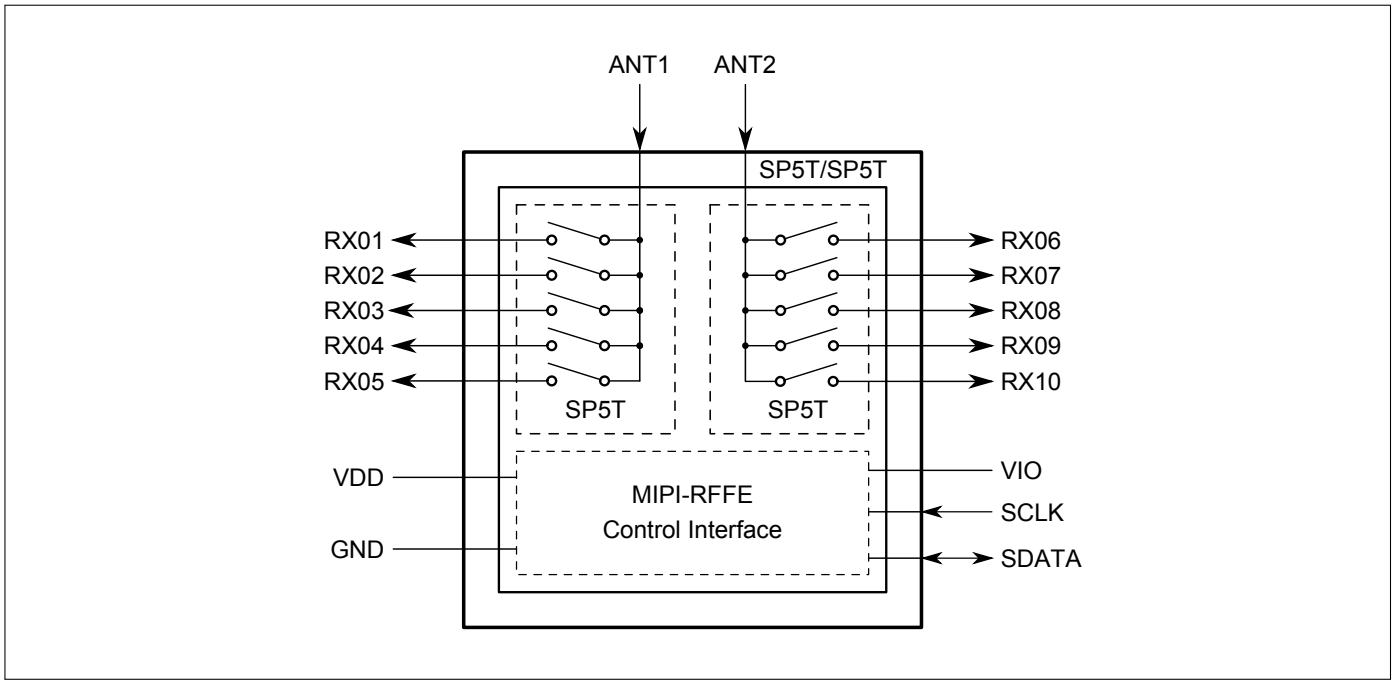


Figure 1: BGS1515MN20 Block Diagram

3 Maximum Ratings

Stresses above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Table 2: Maximum Ratings, Table I at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency range	f	0.1	–	–	GHz	[1]
Supply voltage	V_{DD}	-0.5	–	6.0	V	–
Storage temperature range	T_{STG}	-55	–	150	°C	–
Junction temperature	T_j	–	–	125	°C	–
ESD capability, CDM[2]	V_{ESD_CDM}	-1	–	+1	kV	All pins
ESD capability, HBM[3]	V_{ESD_HBM}	-1	–	+1	kV	Digital, digital versus RF
		-1	–	+1	kV	RF
ESD capability, system level[4]	V_{ESD_ANT}	-8	–	+8	kV	ANT versus system GND, with 27 nH shunt inductor

[1] There is also a DC connection between switched paths. The DC voltage at RF ports V_{RFDC} has to be 0V.
[2] Field-Induced Charged-Device Model JESD22-C101. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.
[3] Human Body Model ANSI/ESDA/JEDEC JS-001-2012 (R=1.5 kΩ, C=100 pF).
[4] IEC 61000-4-2 (R=330 Ω, C=150 pF), contact discharge.

Table 3: Maximum Ratings, Table II at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance junction - soldering point	R_{thJS}	–	54	–	K/W	–
Maximum DC-voltage on RF-ports and RF-ground	V_{RFDC}	0	–	0	V	No DC voltages allowed on RF-ports
RFFE supply voltage	V_{IO}	-0.5	–	3.6	V	–
RFFE control voltage levels	V_{SCLK}, V_{SDATA}	-0.7	–	V_{IO}+0.7 (max. 3.6)	V	–

4 Operation Ranges

Table 4: Operation Ranges

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	2.5	–	5.5	V	–
Supply current[2)]	I_{BAT}	–	80	200	µA	–
Supply current in standby mode[2)]	I_{BAT_SB}	–	0.5	1	µA	VIO=low or MIPI low-power mode
RFFE supply voltage	V_{IO}	1.1	1.8	1.95	V	–
RFFE input high voltage[1)]	V_{IH}	0.7*V_{IO}	–	V_{IO}	V	–
RFFE input low voltage[1)]	V_{IL}	0	–	0.3*V_{IO}	V	–
RFFE output high voltage[1)]	V_{OH}	0.8*V_{IO}	–	V_{IO}	V	–
RFFE output low voltage[1)]	V_{OL}	0	–	0.2*V_{IO}	V	–
RFFE control input capacitance	C_{Ctrl}	–	–	2	pF	–
RFFE supply current	I_{VIO}	–	15	–	µA	Idle State
Ambient temperature	T_A	-30	25	85	°C	–

[1)] SCLK and SDATA
[2)] T_A = –30 °C - 85 °C, V_{DD}= 2.5 - 5.5 V

Table 5: RF Input Power

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rx ports (50 Ω)	P_{RF_Rx}	–	–	27	dBm	–

5 RF Characteristics

Table 6: RF Characteristics at T_A = –30 °C–85 °C, P_{IN} = 0 dBm, Supply Voltage V_{DD}= 2.5 V–5.5 V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion Loss						
All Rx Ports	IL	–	0.25	0.40	dB	0.5–1.0 GHz
		–	0.35	0.55	dB	1.0–2.0 GHz
		–	0.45	0.65	dB	2.0–2.7 GHz
Return Loss						
All Rx Ports	RL	22	27	–	dB	0.5–1.0 GHz
		17	22	–	dB	1.0–2.0 GHz
		12	17	–	dB	2.0–2.7 GHz
Isolation						
All Rx Ports	ISO	27	40	–	dB	0.5–1.0 GHz
		21	35	–	dB	1.0–2.0 GHz
		19	30	–	dB	2.0–2.7 GHz
P0.1 dB Compression Point, Extrapolated						
All Rx Ports	$P_{0.1dB}$	34	–	–	dBm	
Intermodulation Distortion (UMTS Band 1, Band 5)[1)]						
2nd order intermodulation	IMD2 low	–	-105	-95	dBm	IMT, US Cell (see Tab. 8)
3rd order intermodulation	IMD3	–	-110	-100	dBm	IMT, US Cell (see Tab. 9)
2nd order intermodulation	IMD2 high	–	-110	-100	dBm	IMT, US Cell (see Tab. 8)
Harmonic Generation (UMTS Band 1, Band 5)						
H2	P_{Harm}	80	90	–	dBc	25 dBm, 50Ω, CW mode
H3	P_{Harm}	80	90	–	dBc	25 dBm, 50Ω, CW mode

[1)] On application board with shunt inductor according to application circuit shown in Fig. 3

Table 7: Switching Time at T_A = 25 °C, P_{IN} = 0 dBm, Supply Voltage V_{DD}= 2.5 V–5.5 V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Switching Time						
On/Off	$t_{on/off}$	–	1	2	µs	50 % last SCLK falling edge to 90 % ON, see Fig. 2
Power Up Settling Time	t_{PUP}	–	10	25	µs	After power down mode

Table 8: IMD2 Testcases

Band	CW tone 1 (MHz)	CW tone 1 (dBm)	CW tone 2 (MHz)	CW tone 2 (dBm)
IMT	1950	20	190 (IMD2 low)	-15
			4090 (IMD2 high)	
US Cell	835	20	45 (IMD2 low)	-15
			1715 (IMD2 high)	

Table 9: IMD3 Testcases

Band	CW tone 1 (MHz)	CW tone 1 (dBm)	CW tone 2 (MHz)	CW tone 2 (dBm)
IMT	1950	20	1760	-15
US Cell	835	20	790	-15

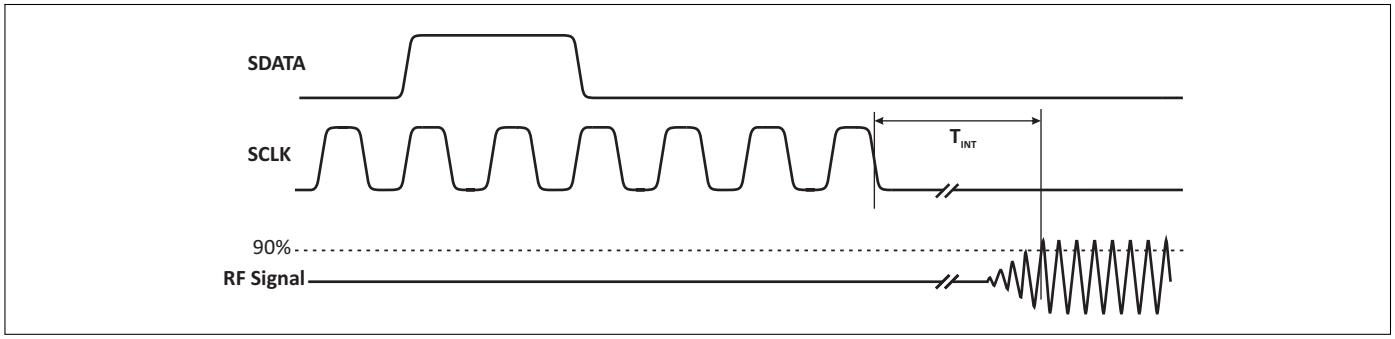


Figure 2: MIPI to RF Time

6 MIPI RFFE Specification

All sequences are implemented according to the 'MIPI Alliance Specification for RF Front-End Control Interface' document version 1.10 - 26. July 2011.

Table 10: MIPI Features

Feature	Supported	Comment
Register write command sequence	Yes	
Register read command sequence	Yes	
Extended register write command sequence	No	
Extented register read command sequence	No	
Register 0 write command sequence	Yes	
Trigger function	Yes	Trigger assignment to each control register is supported
Programmable USID	Yes	3 register command sequence and extended register command sequence
Status Register	Yes	Register for debugging
Reset	Yes	By VIO, Power Mode and RFFE_STATUS
Group SID	Yes	
USID_Sel pin	No	External pin for changing USID is not implemented
Full speed write	Yes	
Half speed read	Yes	
Full speed read	Yes	

Table 11: Startup Behavior

Feature	State	Comment
Power status	LOW POWER	The chip is in low power mode after startup
Trigger function	ENABLED	Trigger function is enabled after startup. Trigger function can be disabled via PM_TRIG register.

Table 12: Register Mapping, Table I

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x0000	REGISTER_0	7:0	MODE_CTRL	Switch control	00000000	No	Yes	R/W
0x001D	PRODUCT_ID	7:0	PRODUCT_ID	This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	10000110	No	No	R
0x001E	MANUFACTURER_ID	7:0	MANUFACTURER_ID [7:0]	This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value.	00011010	No	No	R

Table 13: Register Mapping, Table II

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x001C	PM_TRIG	7:6	PWR_MODE	00: Normal operation 01: Default settings (STARTUP) 10: Low power (LOW POWER) 11: Reserved	10	Yes	No	R/W
		5	TRIGGER_MASK_2	If this bit is set, trigger 2 is disabled. When all triggers disabled, if writing to a register that is associated to trigger 2, the data goes directly to the destination register.	0	No	No	
		4	TRIGGER_MASK_1	If this bit is set, trigger 1 is disabled. When all triggers disabled, if writing to a register that is associated to trigger 1, the data goes directly to the destination register.	0	No	No	
		3	TRIGGER_MASK_0	If this bit is set, trigger 0 is disabled. When all triggers disabled, if writing to a register that is associated to trigger 0, the data goes directly to the destination register.	0	No	No	
		2	TRIGGER_2	A write of a one to this bit loads trigger 2's registers.	0	Yes	No	
		1	TRIGGER_1	A write of a one to this bit loads trigger 1's registers.	0	Yes	No	
		0	TRIGGER_0	A write of a one to this bit loads trigger 0's registers.	0	Yes	No	
0x001F	MAN_USID	7:6	SPARE	These are read-only bits that are reserved and yield a value of 0b00 at readback.	00	No	No	R
		5:4	MANUFACTURER_ID [9:8]	These bits are read-only. However, during the programming of the USID, a write command sequence is performed on this register even though the write does not change its value.	01			
		3:0	USID	Programmable USID. Performing a write to this register using the described programming sequences will program the USID in devices supporting this feature. These bits store the USID of the device.	1010	No	No	R/W
0x001A	RFFE_STATUS	7	SOFTWARE RESET	0: Normal operation 1: Software reset	0	No	No	R/W
		6	COMMAND_FRAME_ PARITY_ERR	Command sequence received with parity error - discard command	0	No	No	
		5	COMMAND_LENGTH_ERR	Command length error	0			
		4	ADDRESS_FRAME_ PARITY_ERR	Address frame parity error	0			
		3	DATA_FRAME_ PARITY_ERR	Data frame with parity error	0			
		2	READ_UNUSED_REG	Read command to an invalid address	0			
		1	WRITE_UNUSED_REG	Write command to an invalid address	0			
		0	BID_GID_ERR	Read command with a BROADCAST_ID or GROUP_SID	0			
0x001B	GROUP_SID	7:4	RESERVED		0	No	No	R/W
		3:0	GROUP_SID	Group slave ID	0			

[1] Reset of all configurable registers to default values except for USID, GROUP_SID, or PM_TRIG

Table 14: Modes of Operation (Truth Table, Register_0)

		REGISTER_0 Bits							
State	**Mode**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	Isolation	x	x	x	x	x	0	0	0
2	ANT1-RX01	x	x	x	x	x	1	0	1
3	ANT1-RX02	x	x	x	x	x	1	0	0
4	ANT1-RX03	x	x	x	x	x	0	1	1
5	ANT1-RX04	x	x	x	x	x	0	1	0
6	ANT1-RX05	x	x	x	x	x	0	0	1

Table 15: Modes of Operation (Truth Table, Register_1)

		REGISTER_1 Bits							
State	**Mode**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
8	Isolation	x	x	x	x	0	0	0	0
8	ANT2-RX06	x	x	x	x	0	0	0	1
9	ANT2-RX07	x	x	x	x	0	0	1	0
10	ANT2-RX08	x	x	x	x	0	0	1	1
11	ANT2-RX09	x	x	x	x	0	1	0	0
12	ANT2-RX10	x	x	x	x	0	1	0	1

7 Pin Definition and Package Outline

Table 16: Pin Configuration

No	Name	Pin Type	Buffer Type	Function
0	GND	GND		RF ground; die pad
1	NC			Not connected
2	RX10	I/O		RX port 10
3	RX09	I/O		RX port 9
4	RX08	I/O		RX port 8
5	RX07	I/O		RX port 7
6	RX06	I/O		RX port 6
7	GND	GND		RF ground
8	ANT2	I/O		Antenna port 2
9	ANT1	I/O		Antenna port 1
10	GND	GND		RF ground
11	RX05	I/O		RX port 5
12	RX04	I/O		RX port 4
13	RX03	I/O		RX port 3
14	RX02	I/O		RX port 2
15	RX01	I/O		RX port 1
16	GND	GND		RF ground
17	VDD	PWR		V_{DD} supply
18	VIO	PWR		MIPI RFFE supply
19	SDATA	I/O		MIPI RFFE data
20	SCLK	I		MIPI RFFE clock

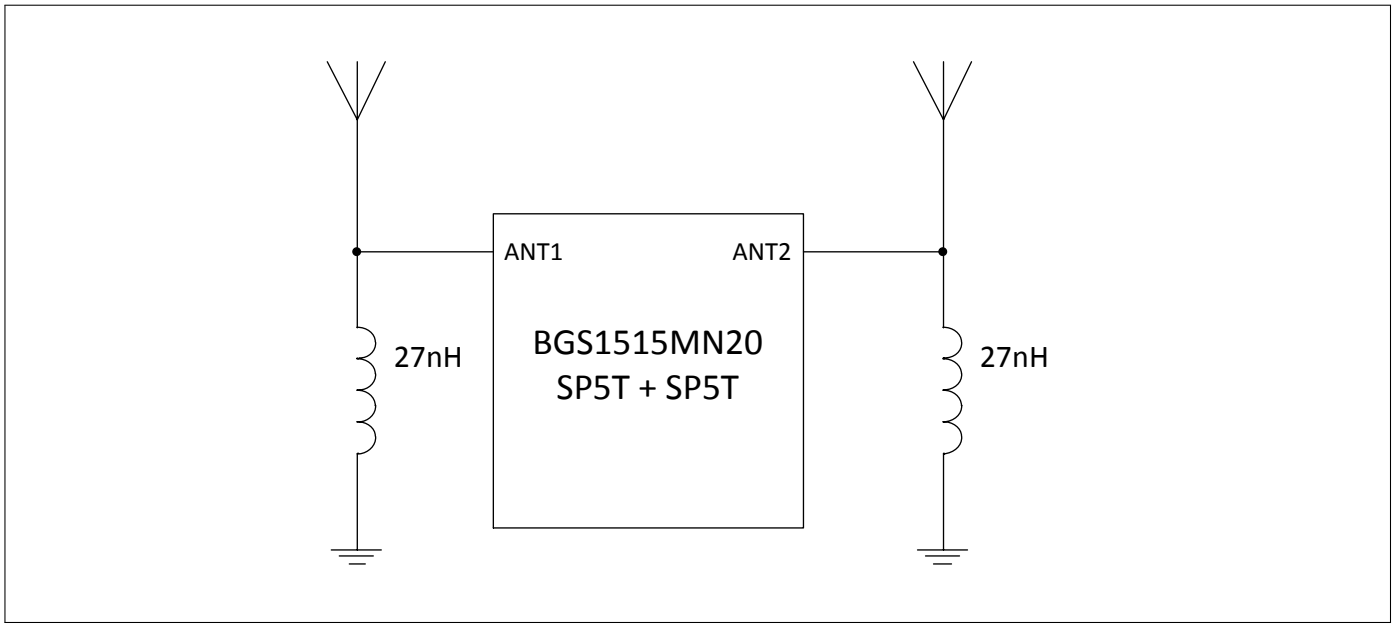


Figure 3: Application Circuit

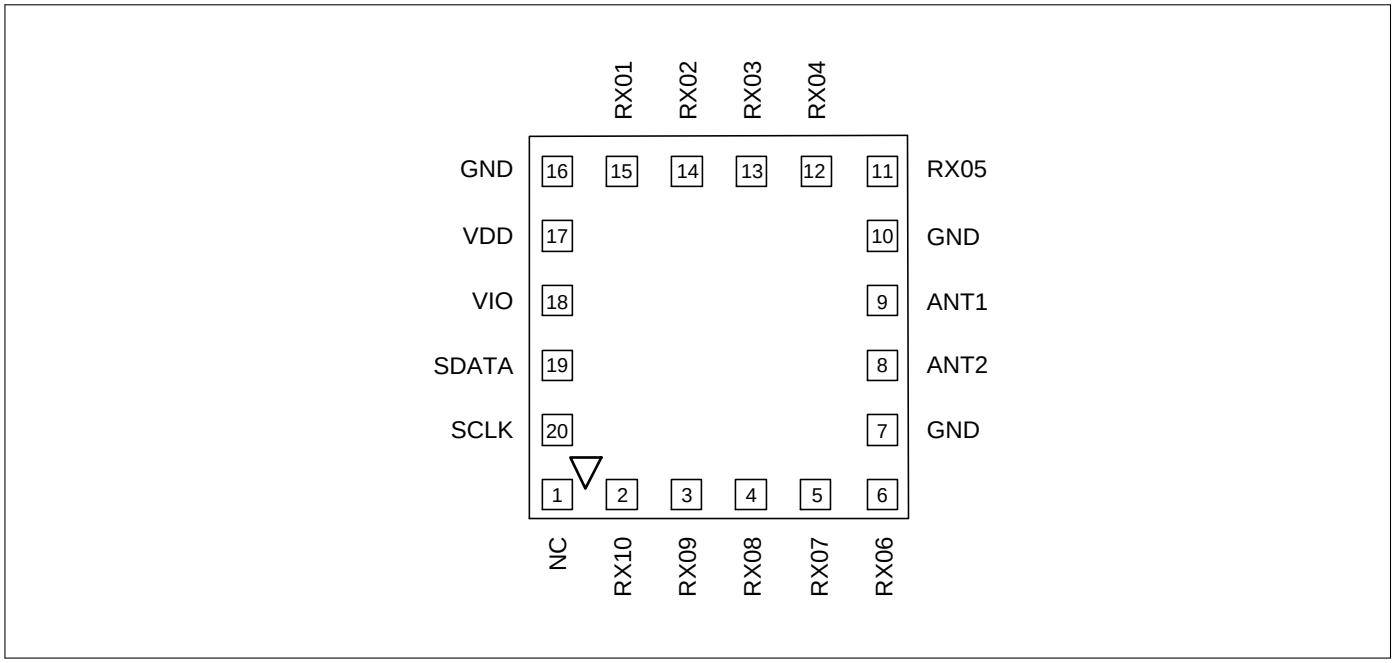


Figure 4: Pin Configuration (top view)

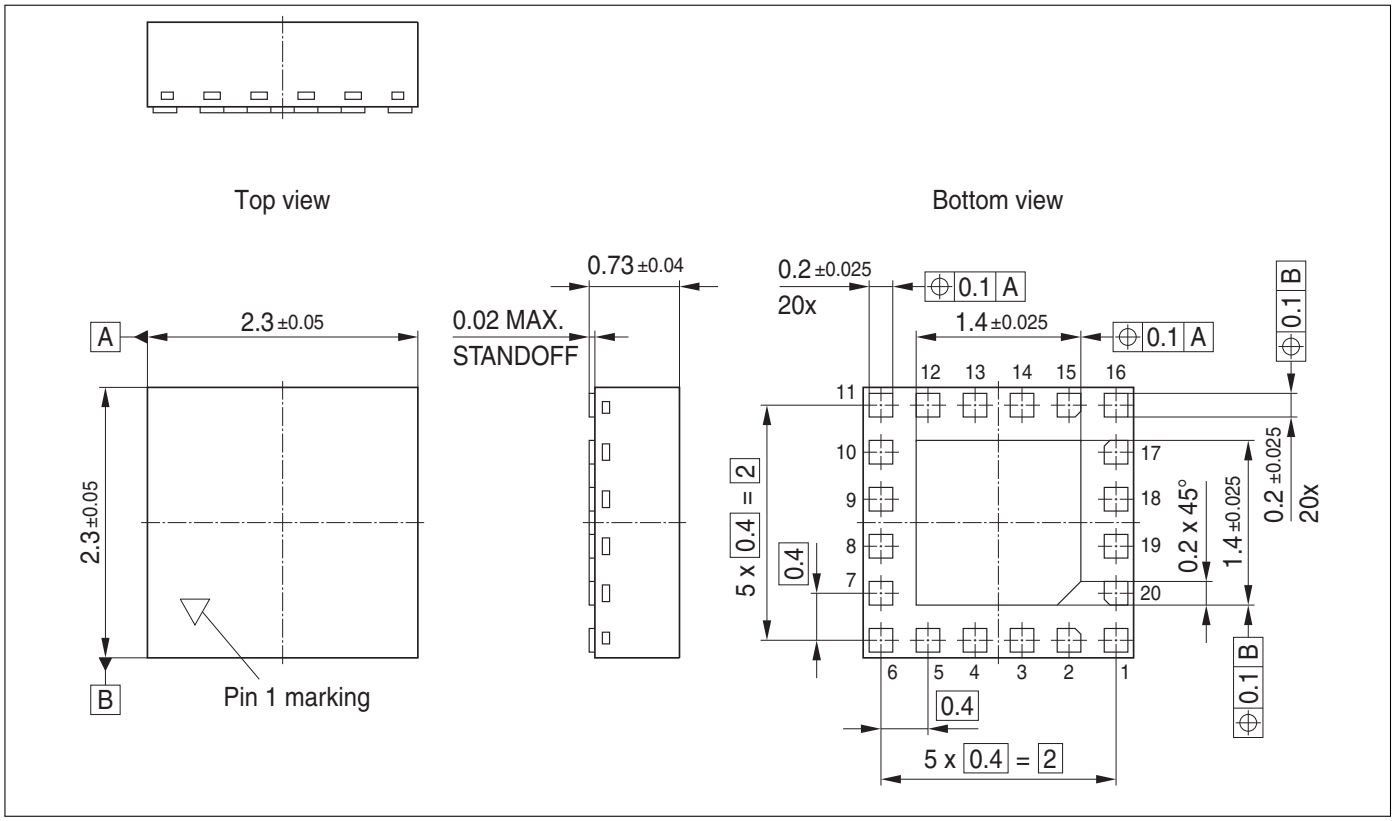


Figure 5: Package Outline (bottom and side view)

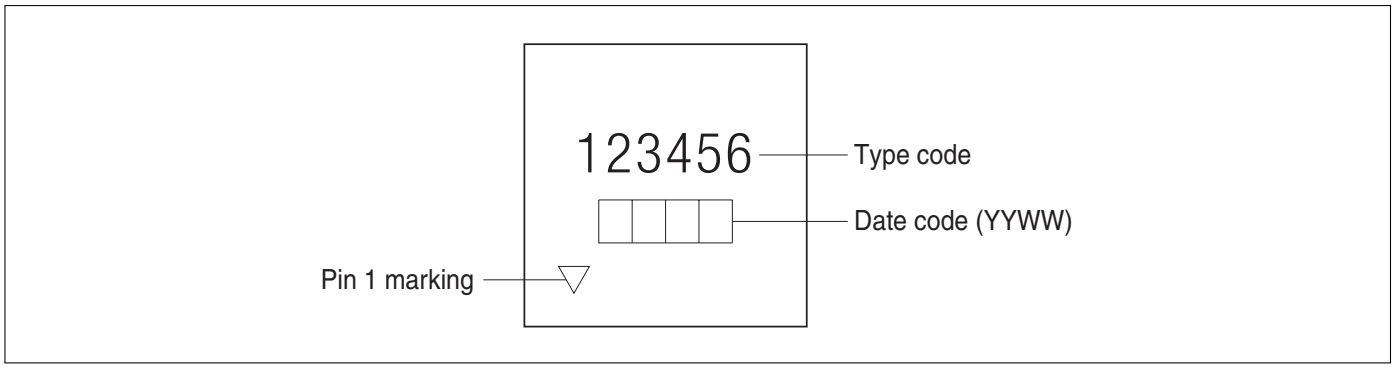


Figure 6: Marking Pattern

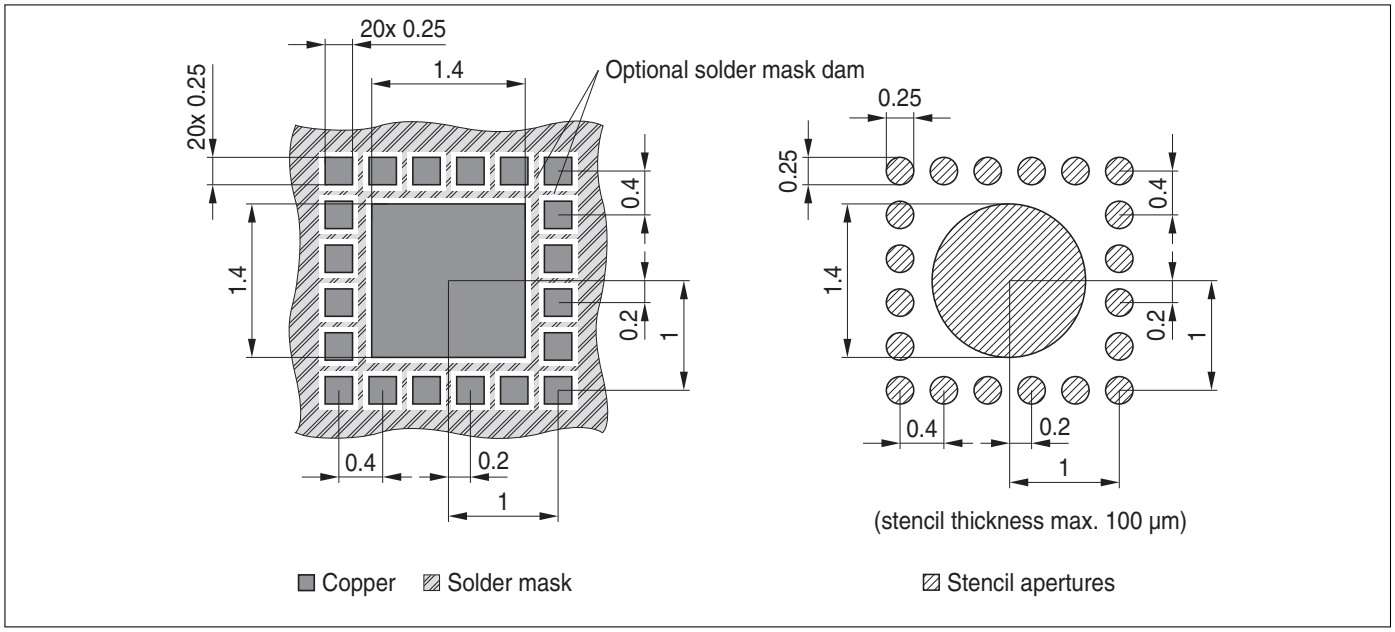


Figure 7: Land Pattern and Stencil Mask

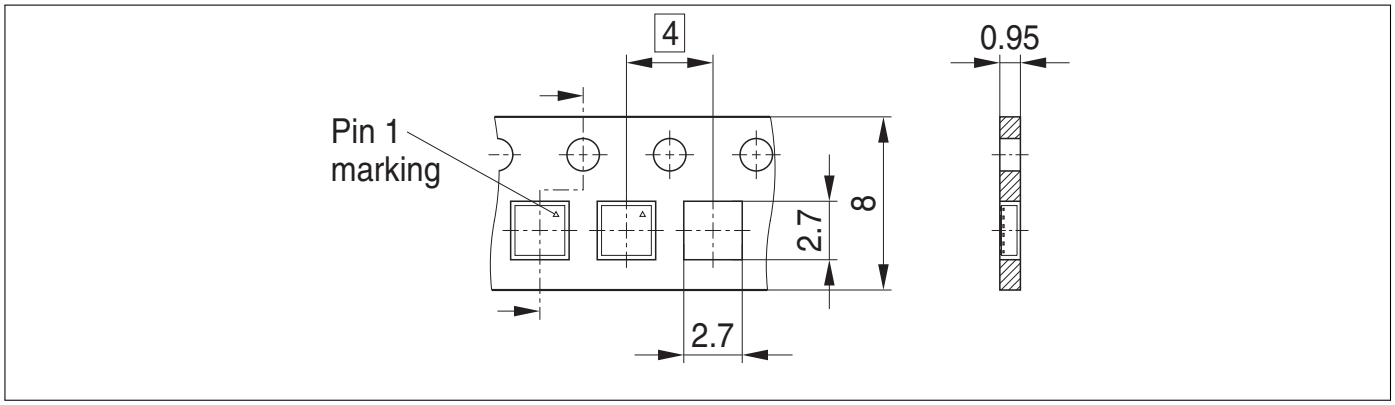


Figure 8: Tape Dimensions

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