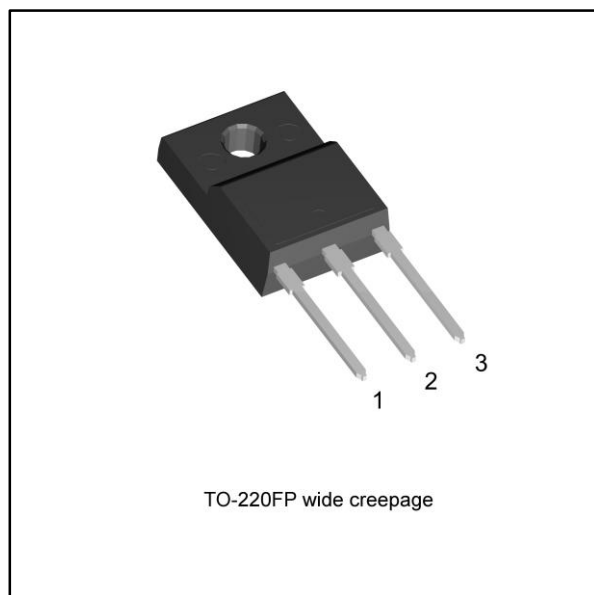
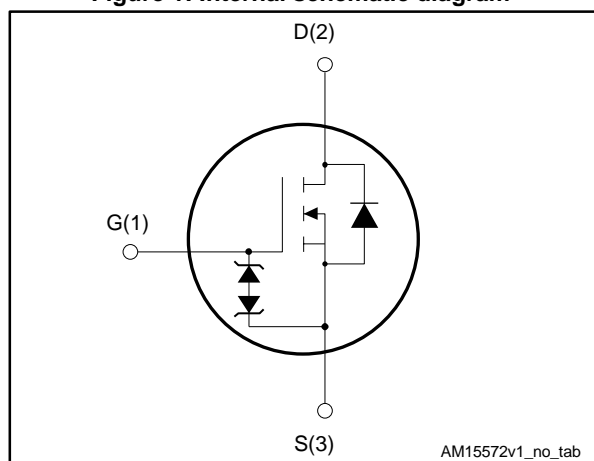


N-channel 600 V, 0.168 Ω typ., 18 A MDmesh™ M2 Power MOSFET in a TO-220FP wide creepage package

Datasheet - production data


Figure 1: Internal schematic diagram


Features

| Order code | V _{DS} @ T _{Jmax} | R _{DS(on)} max | I _D |
|-------------|-------------------------------------|-------------------------|----------------|
| STFH24N60M2 | 650 V | 0.19 Ω | 18 A |

- Extremely low gate charge
- Excellent output capacitance (C_{oss}) profile
- 100% avalanche tested
- Zener-protected
- Wide creepage distance of 4.25 mm between the pins

Applications

- Switching applications
- LLC converters, resonant converters

Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

The TO-220FP wide creepage package provides increased surface insulation for Power MOSFETs to prevent failure due to arcing, which can occur in polluted environments.

Table 1: Device summary

| Order code | Marking | Package | Packing |
|-------------|---------|------------------------|---------|
| STFH24N60M2 | 24N60M2 | TO-220FP wide creepage | Tube |

Contents

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1 Electrical ratings

Table 2: Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|--------------------------------|-----------------------------------------------------------------------------------------------------------------|-------------------|------|
| V _{GS} | Gate-source voltage | ± 25 | V |
| I _D | Drain current (continuous) at T _C = 25 °C | 18 ⁽¹⁾ | A |
| I _D | Drain current (continuous) at T _C = 100 °C | 12 ⁽¹⁾ | A |
| I _{DM} ⁽²⁾ | Drain current (pulsed) | 72 ⁽¹⁾ | A |
| P _{TOT} | Total dissipation at T _C = 25 °C | 30 | W |
| dv/dt ⁽³⁾ | Peak diode recovery voltage slope | 15 | V/ns |
| dv/dt ⁽⁴⁾ | MOSFET dv/dt ruggedness | 50 | V/ns |
| V _{ISO} | Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T _C = 25 °C) | 2500 | V |
| T _{stg} | Storage temperature range | - 55 to 150 | °C |
| T _j | Operating junction temperature range | | |

Notes:

⁽¹⁾Limited by maximum junction temperature.

⁽²⁾Pulse width limited by safe operating area.

⁽³⁾I_{SD} ≤ 18 A, di/dt ≤ 400 A/μs; V_{DSpeak} < V_{(BR)DSS}, V_{DD} = 400 V.

⁽⁴⁾V_{DS} ≤ 480 V.

Table 3: Thermal data

| Symbol | Parameter | Value | Unit |
|-----------------------|-----------------------------------------|-------|------|
| R _{thj-case} | Thermal resistance junction-case max | 4.2 | °C/W |
| R _{thj-amb} | Thermal resistance junction-ambient max | 62.5 | °C/W |

Table 4: Avalanche characteristics

| Symbol | Parameter | Value | Unit |
|-----------------|--------------------------------------------------------------------------------------------------------------------------|-------|------|
| I _{AR} | Avalanche current, repetitive or not repetitive (pulse width limited by T _{jmax}) | 3.5 | A |
| E _{AS} | Single pulse avalanche energy (starting T _j =25 °C, I _D = I _{AR} ; V _{DD} =50 V) | 180 | mJ |

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 5: On /off states

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|------------------------------------|--------------------------------------------------------------------------|------|-------|----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS} = 0, I_D = 1\text{ mA}$ | 600 | | | V |
| I_{DSS} | Zero gate voltage drain current | $V_{GS} = 0, V_{DS} = 600\text{ V}$ | | | 1 | μA |
| | | $V_{GS} = 0,$ $V_{DS} = 600\text{ V},$ $T_C = 125\text{ °C}^{(1)}$ | | | 100 | μA |
| I_{GSS} | Gate-body leakage current | $V_{DS} = 0, V_{GS} = \pm 25\text{ V}$ | | | ± 10 | μA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | 2 | 3 | 4 | V |
| $R_{DS(on)}$ | Static drain-source on- resistance | $V_{GS} = 10\text{ V}, I_D = 9\text{ A}$ | | 0.168 | 0.190 | Ω |

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------------------|-------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|----------|
| C_{iss} | Input capacitance | $V_{DS} = 100\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0\text{ V}$ | - | 1060 | - | pF |
| C_{oss} | Output capacitance | | - | 55 | - | pF |
| C_{rss} | Reverse transfer capacitance | | - | 2.2 | - | pF |
| $C_{oss\text{ eq.}}^{(1)}$ | Equivalent output capacitance | $V_{DS} = 0\text{ to }480\text{ V}, V_{GS} = 0\text{ V}$ | - | 258 | - | pF |
| R_G | Intrinsic gate resistance | $f = 1\text{ MHz}, I_D = 0\text{ A}$ | - | 7 | - | Ω |
| Q_g | Total gate charge | $V_{DD} = 480\text{ V}, I_D = 18\text{ A},$ $V_{GS} = 10\text{ V}$ (see Figure 15: "Test circuit for gate charge behavior") | - | 29 | - | nC |
| Q_{gs} | Gate-source charge | | - | 6 | - | nC |
| Q_{gd} | Gate-drain charge | | - | 12 | - | nC |

Notes:

⁽¹⁾ $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 7: Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 300\text{ V}$, $I_D = 9\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 14: "Test circuit for resistive load switching times" and Figure 19: "Switching time waveform") | - | 14 | - | ns |
| t_r | Rise time | | - | 9 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 60 | - | ns |
| t_f | Fall time | | - | 15 | - | ns |

Table 8: Source drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------------|-------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $I_{SD}^{(1)}$ | Source-drain current | | - | | 18 | A |
| $I_{SDM}^{(1)(2)}$ | Source-drain current (pulsed) | | - | | 72 | A |
| $V_{SD}^{(3)}$ | Forward on voltage | $I_{SD} = 18\text{ A}$, $V_{GS} = 0\text{ V}$ | - | | 1.6 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 18\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times") | - | 332 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 4 | | μC |
| I_{RRM} | Reverse recovery current | | - | 24 | | A |
| t_{rr} | Reverse recovery time | $I_{SD} = 18\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times") | - | 450 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 5.5 | | μC |
| I_{RRM} | Reverse recovery current | | - | 25 | | A |

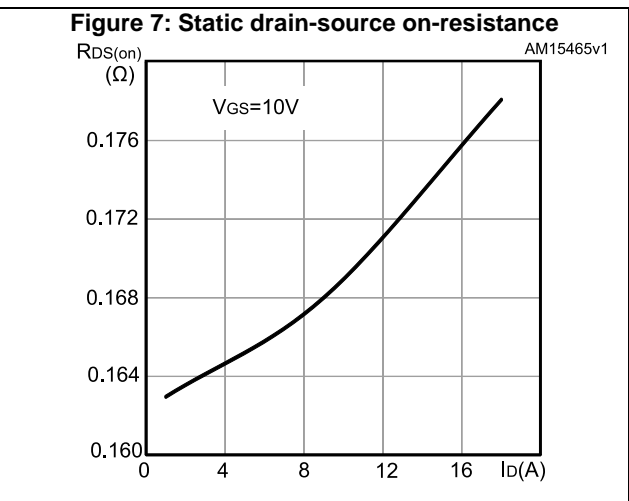
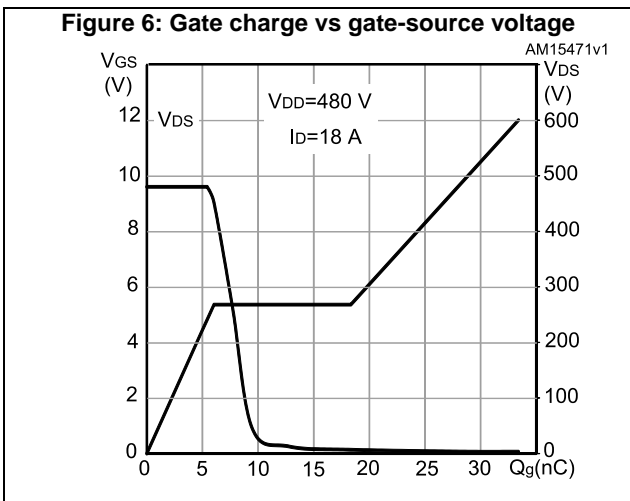
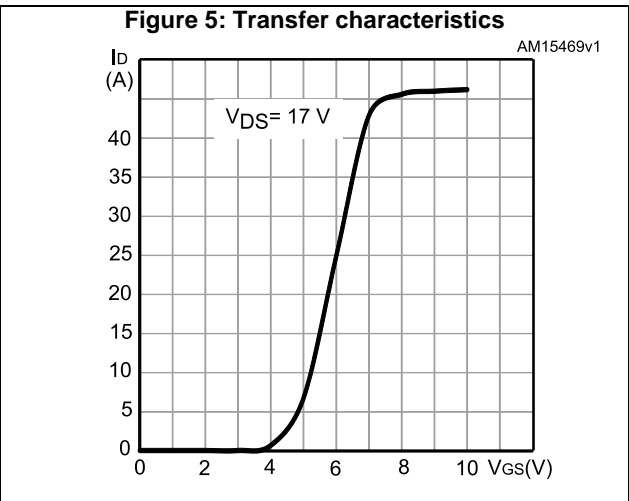
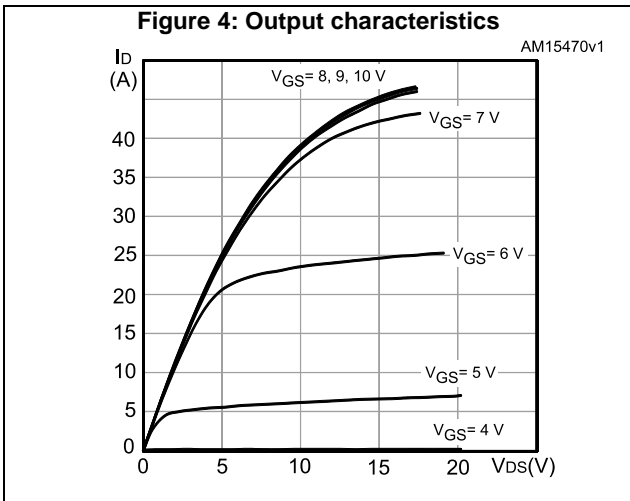
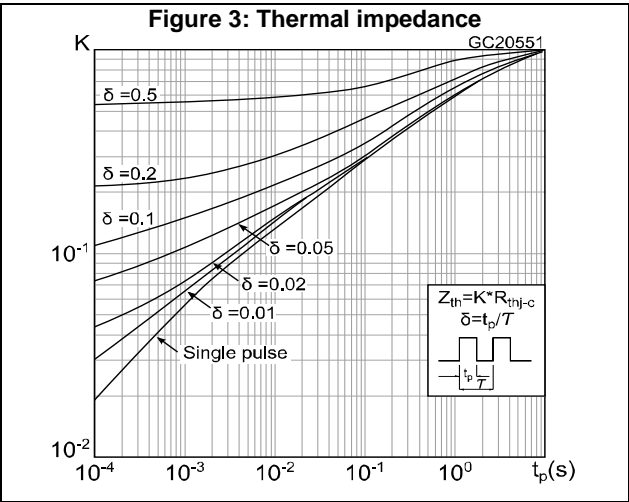
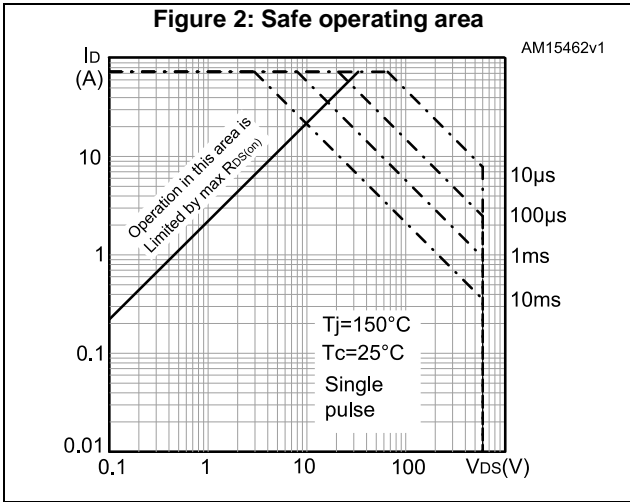
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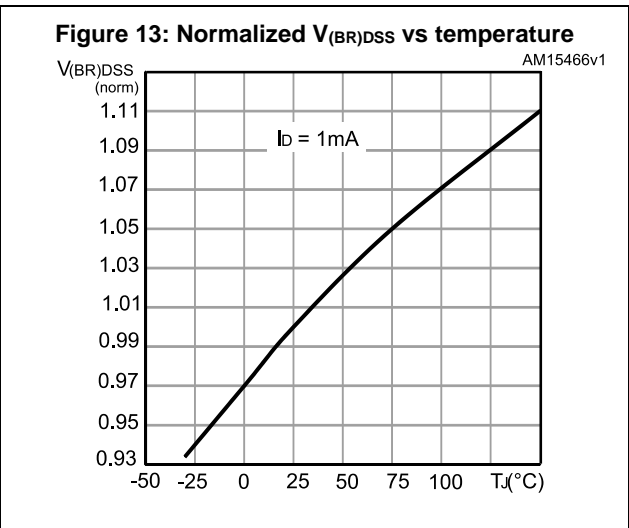
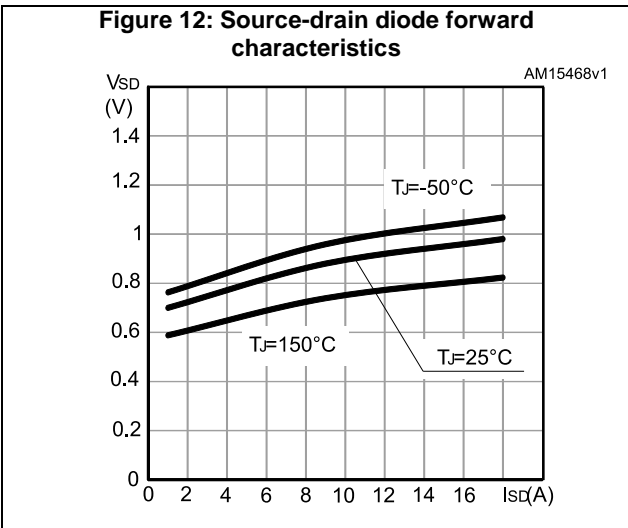
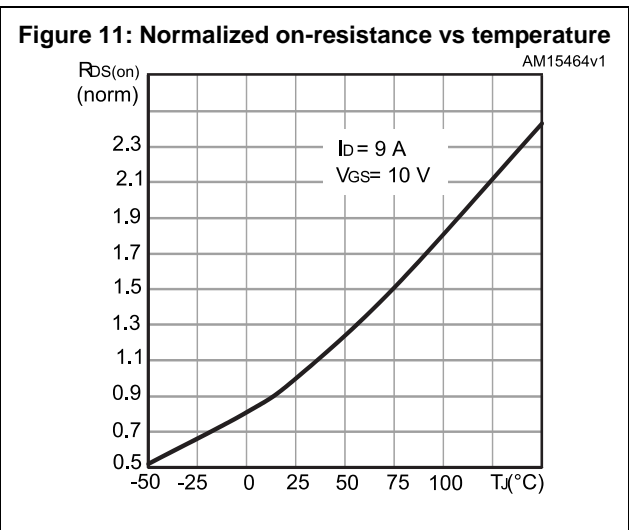
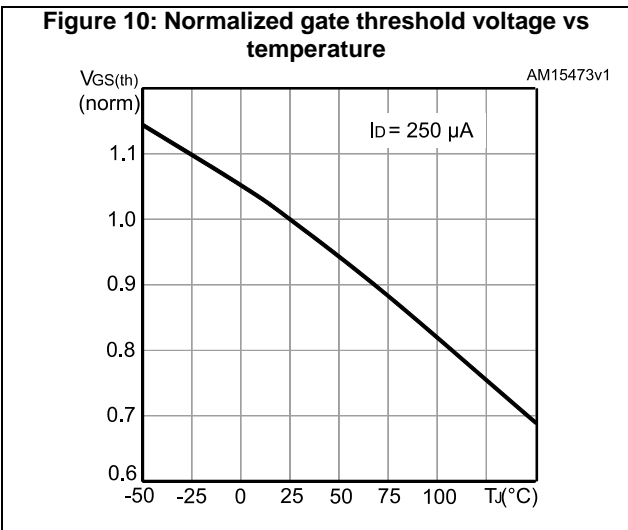
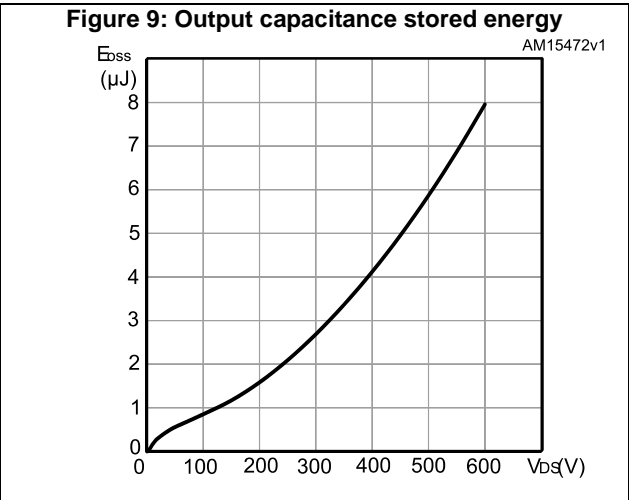
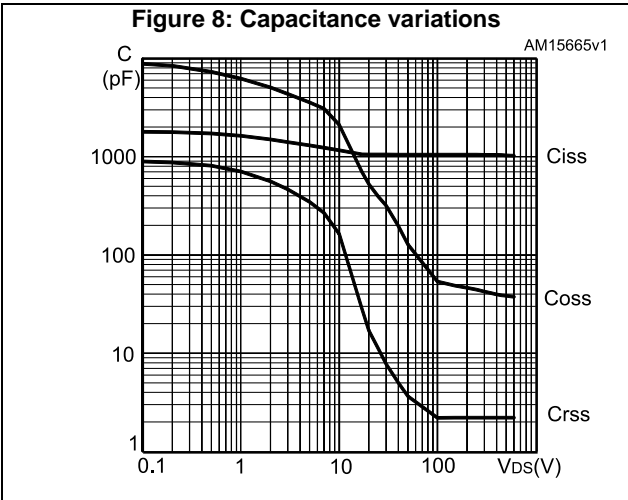
(1)The value is rated according to $R_{thj-case}$ and limited by package.

(2)Pulse width limited by safe operating area

(3)Pulsed: pulse duration = 300 μs , duty cycle 1.5%

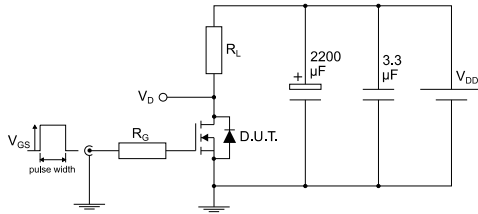
2.1 Electrical characteristics (curves)





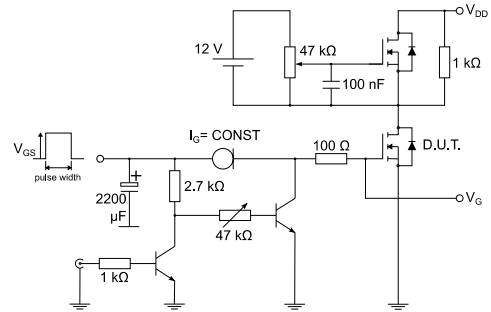
3 Test circuits

Figure 14: Test circuit for resistive load switching times



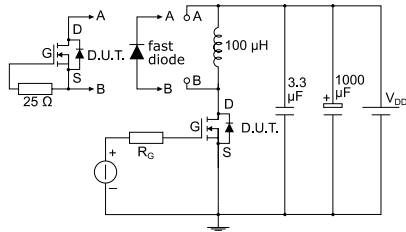
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Figure 15: Test circuit for gate charge behavior



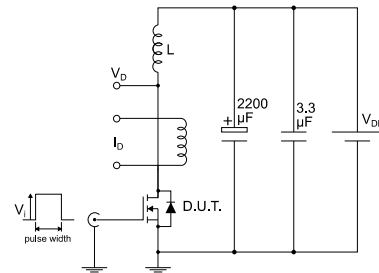
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Figure 16: Test circuit for inductive load switching and diode recovery times



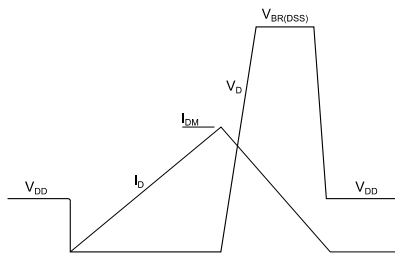
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Figure 17: Unclamped inductive load test circuit



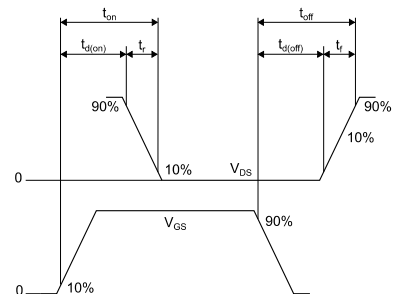
AM01471v1

Figure 18: Unclamped inductive waveform



AM01472v1

Figure 19: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-220FP wide creepage package information

Figure 20: TO-220FP wide creepage package outline

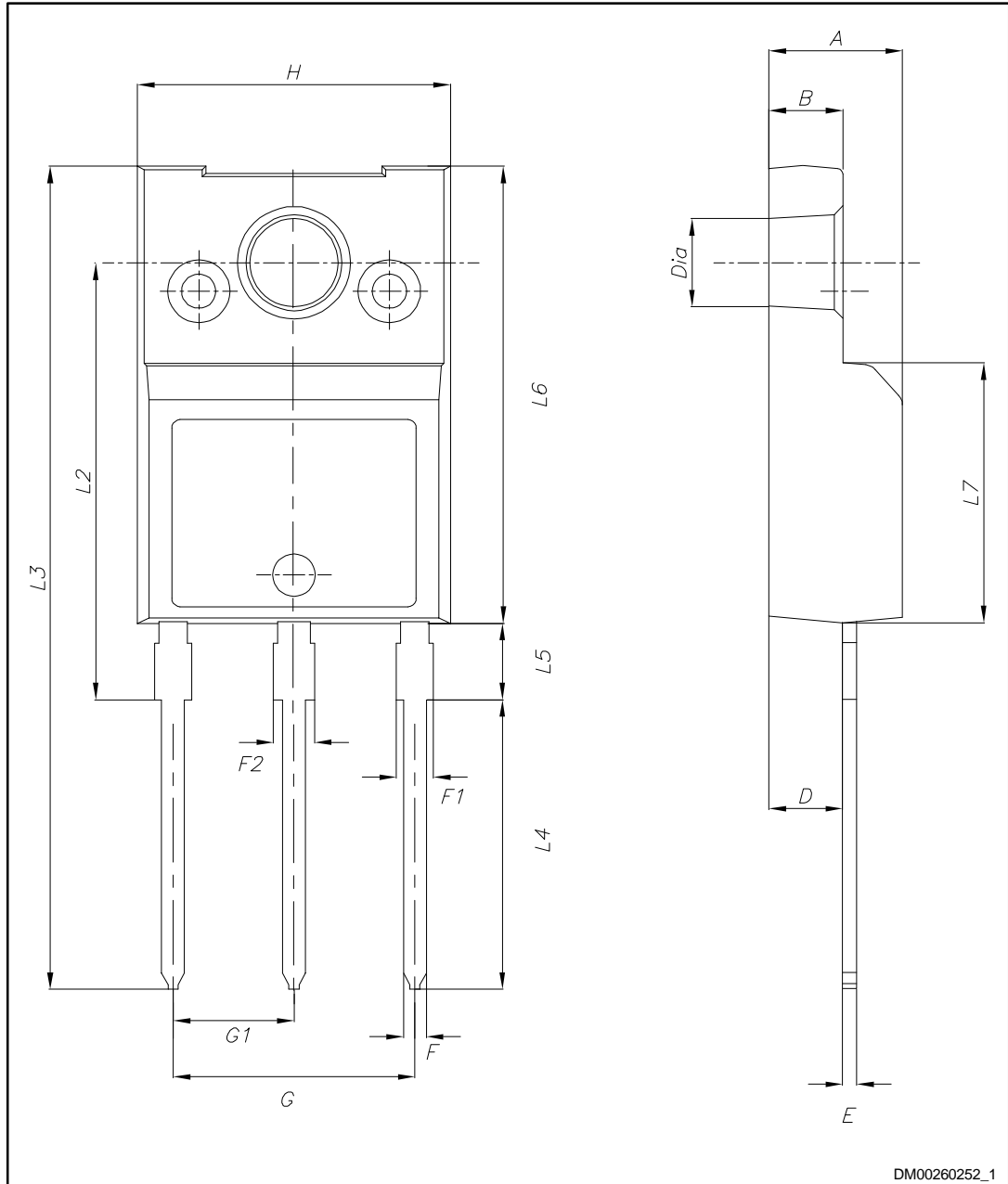


Table 9: TO-220FP wide creepage package mechanical data

| Dim. | mm | | |
|------|-------|-------|-------|
| | Min. | Typ. | Max. |
| A | 4.60 | 4.70 | 4.80 |
| B | 2.50 | 2.60 | 2.70 |
| D | 2.49 | 2.59 | 2.69 |
| E | 0.46 | | 0.59 |
| F | 0.76 | | 0.89 |
| F1 | 0.96 | | 1.25 |
| F2 | 1.11 | | 1.40 |
| G | 8.40 | 8.50 | 8.60 |
| G1 | 4.15 | 4.25 | 4.35 |
| H | 10.90 | 11.00 | 11.10 |
| L2 | 15.25 | 15.40 | 15.55 |
| L3 | 28.70 | 29.00 | 29.30 |
| L4 | 10.00 | 10.20 | 10.40 |
| L5 | 2.55 | 2.70 | 2.85 |
| L6 | 16.00 | 16.10 | 16.20 |
| L7 | 9.05 | 9.15 | 9.25 |
| Dia | 3.00 | 3.10 | 3.20 |

5 Revision history

Table 10: Document revision history

| Date | Revision | Changes |
|-------------|----------|-------------------------------------------------------------------------------------------|
| 07-Jun-2016 | 1 | First release. |
| 16-Jun-2016 | 2 | Document status promoted from preliminary data to production data. Minor text changes. |

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