Low-Cost, Integrated Analog Front-End for Weight-Scale and Body Composition Measurement

Check for Samples: AFE4300

FEATURES

- **Weight-Scale Front-End:**
  - **Supports up to Four Load Cell Inputs**
  - **On-Chip Load Cell 1.7-V Excitation Voltage for Ratiometric Measurement**
  - **68-nVrms Input-Referred Noise (0.1 Hz to 2 Hz)**
  - **Best-Fit Linearity: 0.01% of Full-Scale**
  - **Weight-Scale Measurement : 540 µA**
- **Body Composition Front-End:**
  - **Supports Up To Three Tetra-Polar Complex Impedance Measurements**
  - **6-Bit, 1-MSPS Sine-Wave Generation Digital-to-Analog Converter (DAC)**
  - **375-µArms, ±20% Excitation Source**
  - **Dynamic Range : 0 Ω to 2.8 kΩ**
  - **0.1-Ω Measurement RMS Noise in 2-Hz BW**
  - **Body Composition measurement : 970 µA**
- **Analog-to_Digital Converter (ADC):**
  - **16 Bits, 860 SPS**
  - **Supply current: 110 µA**

APPLICATIONS

- **Weight Scales with Body Composition Measurements**

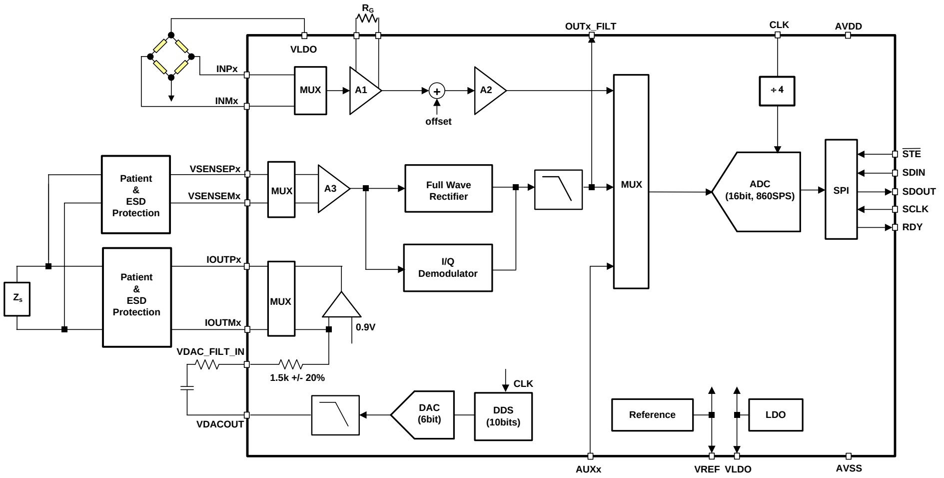
DESCRIPTION

The AFE4300 is a low-cost analog front-end incorporating two separate signal chains: one chain for weight-scale (WS) measurement and the other for body composition measurement (BCM) analysis. A 16-bit, 860-SPS analog-to-digital converter (ADC) is multiplexed between both chains. The weight measurement chain includes an instrumentation amplifier (INA) with the gain set by an external resistor, followed by a 6-bit digital-to-analog converter (DAC) for offset correction, and a circuit to drive the external bridge/load cell with a fixed 1.7 V for ratiometric measurements.

The AFE4300 can also measure body composition by applying a sinusoidal current into the body. The sinusoidal current is generated with an internal pattern generator and a 6-bit, 1-MSPS DAC. A voltage-to-current converter applies this sinusoidal current into the body, between two terminals. The voltage created across these two terminals as a result of the impedance of the body is measured back with a differential amplifier, rectified, and its amplitude is extracted and measured by the 16-bit ADC.

The AFE4300 operates from 2 V to 3.6 V, is specified from 0°C to +70°C, and is available in a TQFP-80 package.

FUNCTIONAL BLOCK DIAGRAM



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION(1)

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		AFE4300	UNIT
Voltage range	AVDD to AVSS	–0.3 to +4.1	V
	Any pin	–0.3 to AVDD + 0.3	V
Diode current at any device pin		±2	mA
Maximum operating junction temperature, T_J max		+105	°C
Storage temperature range, T_{stg}		–25 to +85	°C
Storage humidity		10% to 90%	Rh
Electrostatic discharge ratings	Humand body model (HBM)	2000	V
	Charged device model (CDM)	1000	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD	Supply voltage	2		3.6	V
AVSS	Supply voltage		0		V
f_{CLK}	External clock input frequency		1		MHz
T_A	Ambient temperature range	0		+70	°C

THERMAL INFORMATION

THERMAL METRIC(1)		AFE4300	UNITS
		PN (TQFP)	
		80 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	50.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	14.2	
θ_{JB}	Junction-to-board thermal resistance	25.3	
ψ_{JT}	Junction-to-top characterization parameter	0.5	
ψ_{JB}	Junction-to-board characterization parameter	24.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS: Front-End Amplification (Weight-Scale Signal Chain)

Over operating free-air temperature range, AVDD – AVSS = 3 V, G1 = 183, and G2 = 1, unless otherwise noted.

PARAMETER		TEST CONDITIONS	AFE4300 MIN	AFE4300 TYP	AFE4300 MAX	UNIT
BRIDGE SUPPLY						
$V_{(VLDO)}$	Output voltage (bridge supply voltage)			1.7		V
I_O	Output current	Current capability			20	mA
		Short-circuit protection		100		mA
t_{STBY}	Enable/disable time	With 470 nF cap on VLDO pin		1		ms
AMPLIFICATION CHAIN						
	Offset error	With offset correction DAC disabled		80		µV
	Offset drift vs temperature	With offset correction DAC diasbled		0.25		µV/°C
	Input bias current			±70		fA
	Input offset current			±140		fA
V_n	Noise voltage, equivalent input	G1 = 183, 0.01 Hz < f < 2 Hz		68		nVrms
I_n	Noise current, equivalent input	f = 10 Hz		100		$fA/\sqrt{Hz}$
z_{id}	Differential input impedance			100 || 4		GΩ || pF
z_{ic}	Common-mode input impedance			100 || 8		GΩ || pF
CMRR	Input common-mode rejection ratio	G1 = 183		95		dB
INL_{WS}	Gain nonlinearity	From input to digital output (including ADC)		0.01		% of FS(1)
	First-stage gain equation			$(1 + 2 \times 100k / R_G)$		V/V
t_{up}	Power-up time	From power up to valid reading		1		ms
R1	Internal feedback resistors		95	100	105	kΩ
Gain2	Second-stage gain settings			1, 2, 3, 4		
	Total gain error			±5%		
	Offset DAC number of bits			6		Bits
I_{DAC}	Full-scale offset DAC output current			±6.5		µA

(1) FS = full-scale.

ELECTRICAL CHARACTERISTICS: Body Composition Measurement Front-End

Over operating free-air temperature range, AVDD – AVSSS = 3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	AFE4300			UNIT
			MIN	TYP	MAX	
WAVEFORM GENERATOR						
	DAC resolution			6		Bits
	DAC full-scale voltage	Common mode voltage = 0.9 V		1		$V_{(PP)}$
	DAC sample rate			1		MSPS
BW_{LPF}	–3 dB bandwidth of the 2nd-order low-pass filter			150 ±30		kHz
R1	Internal current-setting resistor			1.5 ±20%		kΩ
DEMODULATION CHAIN						
	Input Impedance			50		kΩ
	Gain	From impedance to dc output of demodulator, IQ Mode & FWR mode		0.72		V/kΩ
	Gain error (without calibration)	FWR mode and I/Q mode		2.5		% of FS
	Offset error (without calibration)	FWR mode and I/Q mode		±5		mV
CMRR	Common-mode rejection ratio			75		dB
	Nonlinearity	0Ω to 1.25 kΩ range		0.15		% of FS
		0Ω to 2.50 kΩ range		3		% of FS
BW_{DEMOD}	Rectifier bandwidth	Internal resistor = 5 kΩ, external capacitor = 4.7 µF		3.5 ±20%		Hz
	Output noise at rectifier output	20-kHz waveform, noise integrated from 0.01 Hz to 2 Hz		15		µVrms

ELECTRICAL CHARACTERISTICS: Analog-to-Digital Converter

Over operating free-air temperature range, AVDD – AVSS = 3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	AFE4300			UNIT
			MIN	TYP	MAX	
ANALOG-TO-DIGITAL CONVERTER						
	ADC input voltage range	At the input of the ADC (after PGA)		2 × V_{REF}		V
V_{IN}	Full-scale input voltage	At the input of the PGA		V_{ADC} / Gain		V
V_{REF}	Reference voltage			1.7		V
$R_{ON(mux)}$	Input multiplexer on-resistance	0 V ≤ V_{AAUX} ≤ AVDD			6	kΩ
	AAUX input impedance			4		MΩ
f_{DR}	Output data rate		8		860	SPS
	Resolution		16			Bits
E_I	Integral linearity error	Best fit, DR = 8 SPS		1		LSB
E_O	Offset error	Differential inputs		±1		LSB
		Single-ended inputs		±3		LSB
E_G	Gain error			0.05%		
V_{BAT_MON}	Battery monitor output			AVDD / 3		V
I_{BAT_MON}	Battery monitor current consumption			1.5		µA
$I_{BAT\_MON\_ACC}$	Battery monitor accuracy			±2%		
POWER CONSUMPTION						
	Supply Current	Power-down current		0.25		µA
		Sleep-mode current		100		µA
		Weight-scale chain measurements		540		µA
		Body-composition measurements		970		µA
		Auxillary-channel measurements		110		µA

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, AVDD – AVSS = 3V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT/OUTPUT						
V_{IH}	High-level input voltage		0.75AVDD		AVDD	V
V_{IL}	Low-level input voltage		AVSS		0.25AVDD	V
V_{OH}	High-level output voltage	I_{OL} = 1 mA	0.8AVDD			V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA	GND		0.2AVDD	V
I_{IN}	Input current			±30		µA

SPI TIMING CHARACTERISTICS

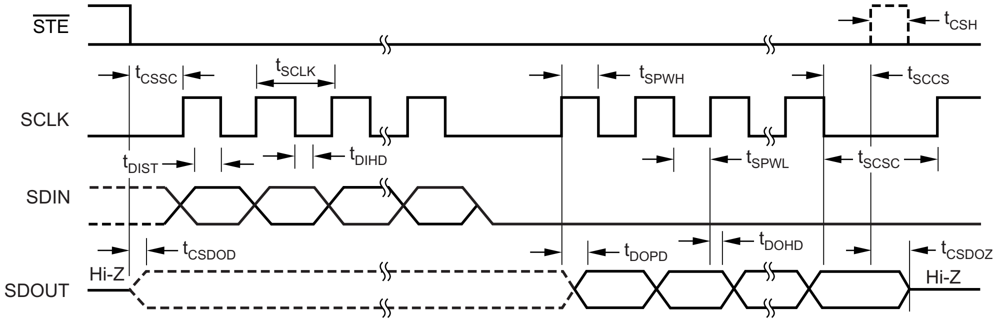


Figure 1. Serial Interface Timing

TIMING REQUIREMENTS: SERIAL INTERFACE TIMING

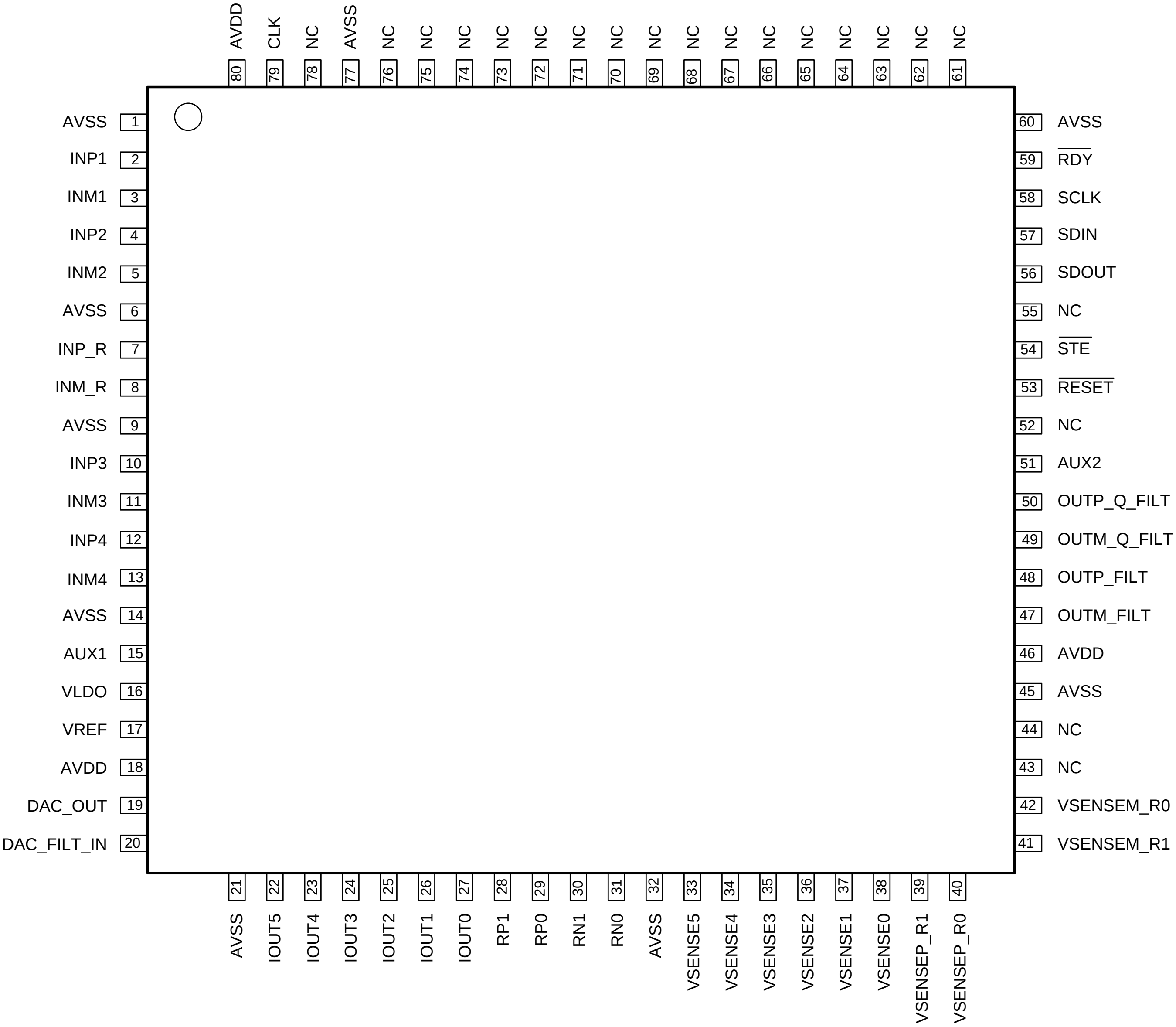
At T_A = 0°C to +70°C and VDD = 2 V to 3.6 V, unless otherwise noted.

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_{CSSC}	$\overline{\text{STE}}$ low to first SCLK setup time[1]	100		ns
t_{SCLK}	SCLK period	250		ns
t_{SPWH}	SCLK pulse width high	100		ns
t_{SPWL}	SCLK pulse width low	100		ns
t_{DIST}	Valid SDIN to SCLK falling edge setup time	50		ns
t_{DIHD}	Valid SDIN to SCLK falling edge hold time	50		ns
t_{DOPD}	SCLK rising edge to valid new SDOUT propagation delay[2]		50	ns
t_{DOHD}	SCLK rising edge to DOUT invalid hold time	0		ns
t_{CSDOD}	$\overline{\text{STE}}$ low to SDOUT driven propagation delay	100		ns
t_{CSDOZ}	$\overline{\text{STE}}$ high to SDOUT Hi-Z propagation delay	100		ns
t_{CSH}	$\overline{\text{STE}}$ high pulse	200		ns
t_{SCCS}	Final SCLK falling edge to $\overline{\text{STE}}$ high	100		ns

(1) $\overline{\text{STE}}$ can be tied low.
(2) DOUT load = 20 pF || 100 kΩ to DGND.

PIN CONFIGURATION

PN PACKAGE
TQFP-80
(TOP VIEW)



PIN ASSIGNMENTS

PIN		INPUT/ OUTPUT	DESCRIPTION
NAME	NUMBER		
AAUX1	15	I	Auxiliary input to the ADC
AAUX2	51	I	Auxiliary input to the ADC
AVDD	18, 46, 80		Supply (3.3 V)
AVSS	1, 6, 9, 14, 21, 32, 45, 60, 77	—	Ground
CLK	79	I	1-MHz clock
DAC_FILT_IN	20	I	Current generator input. Connect ac blocking capacitor between this pin and pin 19.
DACOUT	19	O	DAC output. Connect ac blocking capacitor between this pin and pin 20.

PIN ASSIGNMENTS (continued)

PIN		**INPUT/ OUTPUT**	**DESCRIPTION**
NAME	**NUMBER**		
INM1 to INM4	3, 5, 11, 13	I	Instrumentation amplifier differential inputs for each of the four weight-scale channels
INP1 to INP4	2, 4, 10, 12	I	
INM_R	8	—	Connection of gain setting resistor for the instrumentation amplifier
INP_R	7	—	
IOUT5 to IOUT0	22, 23, 24, 25, 26, 27	O	Current source output to electrodes
NC	43, 44, 52, 55, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 78	—	Do not connect
OUTM_I_FILT	47	—	I channel demodulator low pass filter, connect 10 µF between both pins
OUTP_I_FILT	48	—	
OUTM_Q_FILT	49	—	Q channel demodulator low pass filter, connect 10 µF between both pins
OUTP_Q_FILT	50	—	
$\overline{\text{RDY}}$	59	O	Data ready
RN1, RN0	30, 31	O	Current source output to calibration resistors
RP1, RP0	28, 29	O	
$\overline{\text{RST}}$	53	I	Reset. 0: reset, 1: normal operation.
$\overline{\text{STE}}$	54	I	SPI enable. 0: shift data in, 1: disable.
SCLK	58	I	Clock to latch input data (negative edge latch)
SDIN	57	I	Serial data input
SDOUT	56	O	Serial data output
VLDO	16	O	LDO output to supply the bridges (~1.7 V), Connect 470 nF to AVSS
VREF	17	O	Reference voltage (connect 470 nF to AVSS)
VSENSEN_R1, VSENSEN_R0	41, 42	I	Input to differential amplifier from calibration resistors
VSENSEP_R1, VSENSEP_R0	39, 40	I	
VSENSE5 to VSENSE0	33, 34, 35, 36, 37, 38	I	Input to differential amplifier from electrode

TYPICAL CHARACTERISTICS

All measurements at room temperature with AVDD = 3 V, unless otherwise specified.

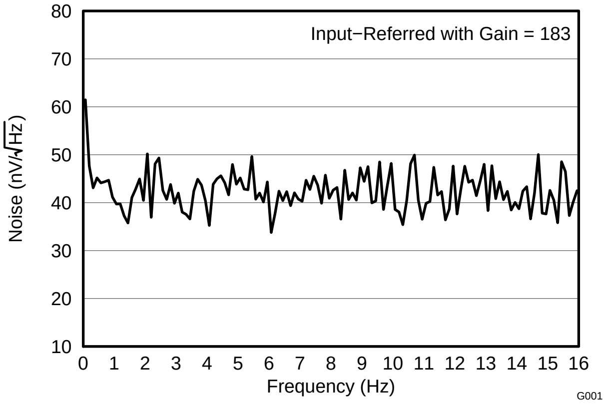


Figure 2. Weight-Scale Chain Noise vs Frequency

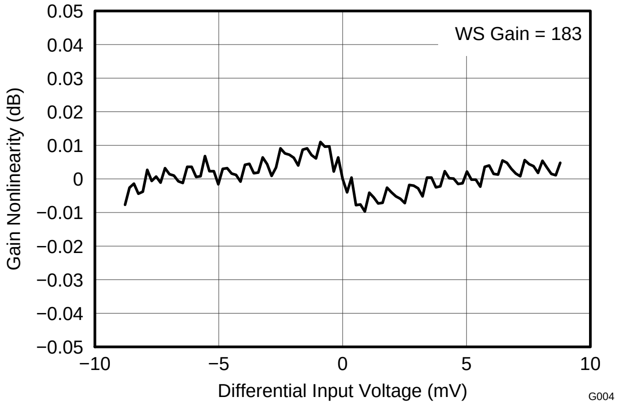


Figure 3. Weight-Scale Chain Nonlinearity

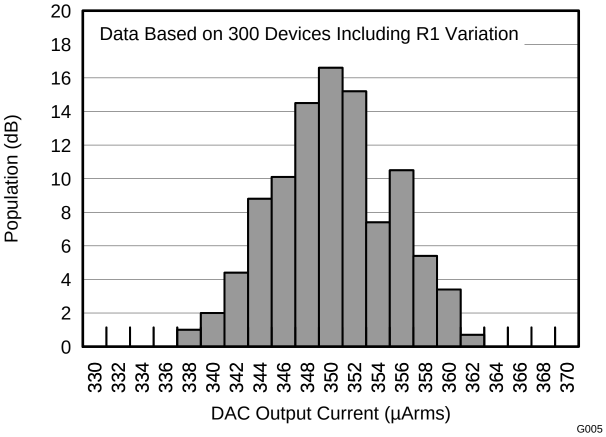


Figure 4. BCM DAC Output Current Distribution

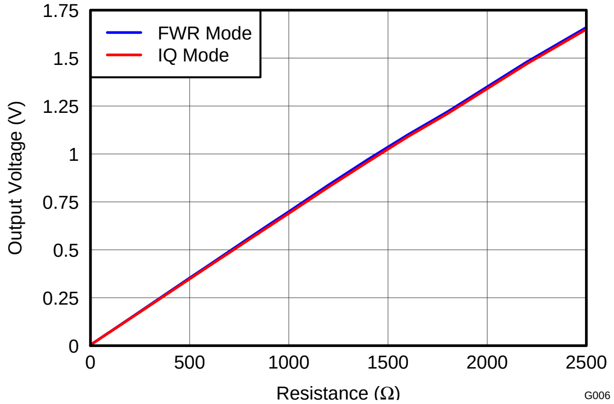


Figure 5. Body Impedance to Output Voltage Transfer Curve

OVERVIEW

The AFE4300 is a low-cost, integrated front-end designed for weight scales incorporating body-composition measurements. The AFE4300 integrates all the components typically used in a weight scale. It has two signal chains: one for weight scale measurements and the other for body composition measurements. Both signal chains share a 16-bit, delta-sigma converter that operates at a data rate of up to 860 SPS. This device also integrates a reference and a low-dropout regulator (LDO) that generates a 1.7-V supply that can be used as the excitation source for the load cells, thus simplifying ratiometric measurements. Both the signal chains use a single DAC. The DAC is used to generate the dc signal for load-cell offset cancellation in the weight-scale chain. The same DAC is also used to generate the sine-wave modulation signal for the body-composition signal chain. Therefore, only one of the two signal chains can be activated at a time (using the apprpriate register bits).

Two unique features of the AFE4300 are that it provides an option for connecting up to four separate load cells, and supports tetrapolar measurements with I/Q measurements.

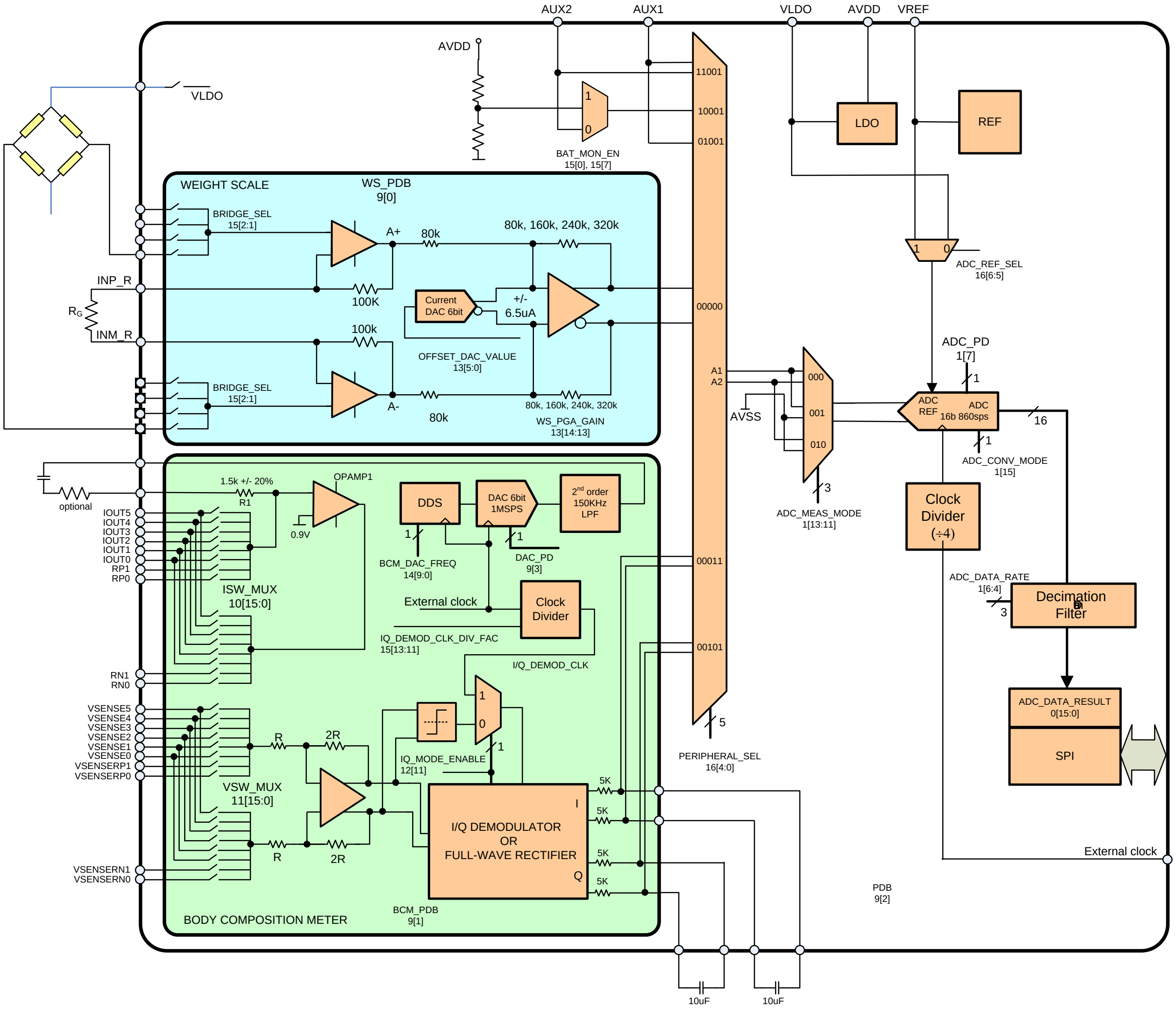


Figure 6. Block Diagram

THEORY OF OPERATION

This section describes the details of the AFE4300 internal functional elements. The analog blocks are reviewed first, followed by the digital interface. The theory behind the body-composition measurement using the full-wave rectification method and the I/Q demodulation method are also described. The analog front-end is divided in two signal chains: a weight-measurement chain and a body-composition measurement front-end chain; both use the same 16-bit ADC and 6-bit DAC.

Throughout this document:

- f_{CLK} denotes the frequency of the signal at the CLK pin.
- t_{CLK} denotes the period of the signal at the CLK pin.
- f_{DR} denotes the output data rate of the ADC.
- t_{DR} denotes the time period of the output data.
- f_{MOD} denotes the frequency at which the modulator samples the input.

WEIGHT-SCALE ANALOG FRONT-END

Figure 7 shows a top-level view of the front-end section devoted to weight-scale measurement. The weight-scale front-end has two stages of gain, with an offset correction DAC in the second gain stage. The first-stage gain is set by the external resistor and the second-stage gain is set by progamming the internal registers. For access and programming information, see the REGISTERS section.

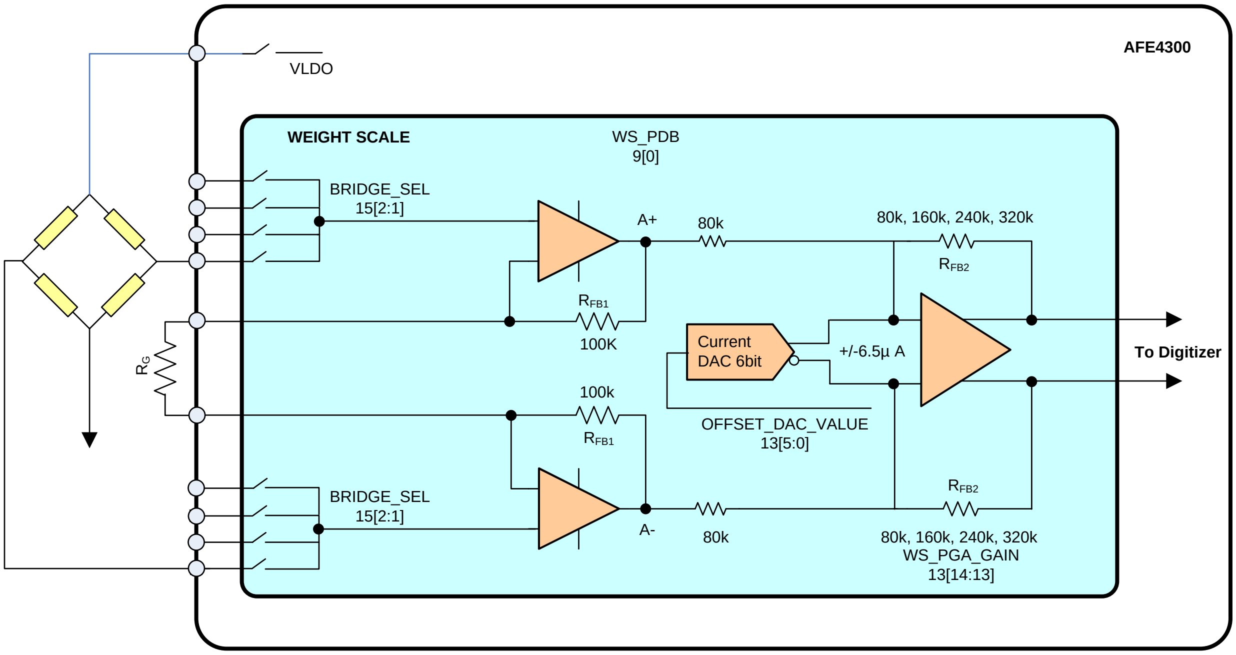


Figure 7. Weight-Scale Front-End

Though not shown in the diagram, an antialiasing network is required in front of the INA to filter out electromagnetic interference (EMI) signals or any other anticipated interference signals. A simple RC network should be sufficient, combined with of the attenuation provided by the on-chip decimation filter.

An internal reference source provides a constant voltage of 1.7 V at the VLDO output to drive the external bridge. The output of the bridge is connected to an INA (first stage). The first-stage gain (A_1) is set by the external resistor (R_G) and the 100-kΩ (±5%) internal feedback resistors (R_{FB1}) as shown in Equation 1:

$$A_1 = (1 + 2 \times 100k / R_G) \tag{1}$$

The second-stage gain (A_2) is controlled by feedback resistors R_{FB2}, which have four possible values: 80 kΩ, 160 kΩ, 240 kΩ, and 320 kΩ. Because the gain is R_F / 80 kΩ, the gain setting can be 1, 2, 3, or 4. See the REGISTERS section for details on setting the appropriate register bits.

Input Common mode Range

The usable input common mode range of the weight-scale front-end depends on various parameters, including the maximum differential input signal, supply voltage, and gain. The output of the first-stage amplifier must be within 250 mV of the power supply rails for linear operation. The allowed common-mode range is determined by Equation 2:

$$\text{AVDD} - 0.25 - \frac{\text{GAIN} \times V_{\text{MAX\_DIFF}}}{2} > \text{CM} > \text{AVSS} + 0.25 + \frac{\text{GAIN} \times V_{\text{MAX\_DIFF}}}{2}$$

Where:

- $V_{\text{MAX\_DIFF}}$ = maximum differential input signal at the input of the first gain stage,
- CM = Common-mode range. (2)

For example, If AVDD = 2 V, the first stage gain = 183, and $V_{\text{MAX\_DFF}}$ = 7.5 mV (dc + signal), then:

1.06 V > CM > 0.936 V

Input Differential Dynamic Range

The max differential (INP – INN) signal depends on the analog supply, reference used in the system. This range is shown in Equation 3:

$$\text{MAX(INP} - \text{INN)} < \frac{\text{VREF}}{\text{GAIN}}\text{; Full-Scale Range} = 2 \times \frac{\text{VREF}}{\text{GAIN}} \quad (3)$$

The gain in Equation 3 is the product of the gains of the INA and the second-stage gain. The full-scale input from the bridge signal typically consists of a differential dc offset from the load cell plus the actual weight signal. Having a high gain in the first stage helps minimize the effect of the noise addition from the subsequent stages. However, make sure to choose a gain that does not saturate the first stage with the full-scale signal. Also, the common-mode of the signal must fall within the range, as per Equation 2.

Offset Correction DAC

One way to increase the dynamic range of the signal chain is by calibrating the inherent offset of the load cell during the initial calibration cycle. The offset correction is implemented in the second stage with a 6-bit differential DAC, where each output is a mirror of the other and can source or sink up to 6.5 µA. The effect at the output of the second stage is an addition of up to ±6.5 µA × 2 × R_{FB2}. This is equivalent to a voltage at the input of the second stage (A+ / A–) of up to ±6.5 µA × 2 × 80 kΩ = ±1 V, when R_{FB2} = 80 kΩ. Notice that this has no effect in avoiding the first-stage saturation. Because the offset correction DAC is a 6-bit DAC, the offset compensation step is $2\text{ V}/2^6$ = 31.2 mV when referred to the input of the second stage.

Offset Correction Example

As an example, use a bridge powered from 1.7 V with 1.5 mV/V sensitivity and a potential offset between –4 mV and 4 mV. Worst case, the maximum signal is 4 mV of offset plus 1.7 × 1.5 mV/V = 2.55 mV of signal, for a total of 6.55 mV. The bridge common-mode voltage is ~0.85 V. The maximum excursion is 0.85 V – 0.25 V = 0.6 V (bottom rail) single-ended, on each output (A+ or A–). Therefore, ±1.2 V differentially at the output of the first stage prevents saturation. This result means that the first stage can have up to a gain of 1.2 V / 6.55 mV = 183.

Using this same example, the swing at the output of the first stage corresponding only to the potential offset range is 183 × ±4 mV = ±0.732 V. This swing can be completely removed at the output of the second stage by the offset correction (because it has a ±1-V range) except for a maximum error of 31.2 mV.

BODY COMPOSITION MEASUREMENT ANALOG FRONT-END

Body composition is traditionally obtained by measuring the impedance across several points on the body and matching the result in a table linking both the impedance measured and the body composition. This table is created by each manufacturer and is usually based on age group, sex, weight, and other parameters.

The body impedance that we want to measure, Z(f), is a function of the excitation frequency, and can be represented by polar or cartesian notations:

$$Z(f) = |Z(f)|.e^{j\theta(f)} = R(f) + jX(f)$$

where:

- $|Z| = \mathrm{sqrt}(R^2 + X^2)$
- $\theta = \mathrm{arctg}(X/R)$ (4)

The AFE4300 provides two options for body impedance measurement: ac rectification and I/Q demodulation. Both options work by injecting a sinusoidal current into the body and measuring the voltage across the body. The portion of the circuit injecting the current into the body is the same for each of those options. The difference, however, lies in how the measured voltage across the impedance is processed to obtain the final result.

AC Rectification

Figure 8 shows the portion of the AFE4300 devoted to body composition measurement in the RMS detector mode.

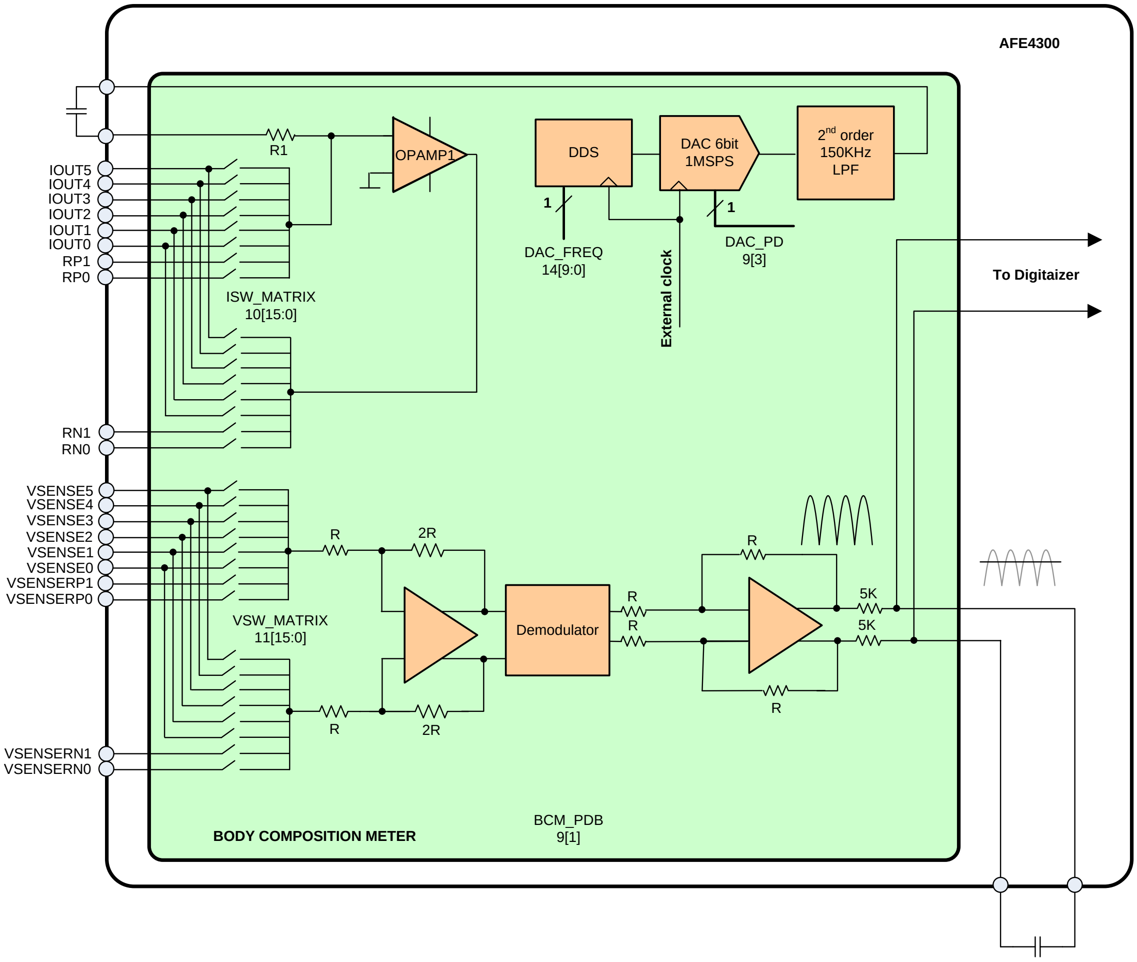


Figure 8. BCM in AC Rectifier Mode

The top portion of Figure 8 represents the current-injection circuit. A direct digital synthesizer (DDS) generates a sinusoidal digital pattern with a frequency obtained by dividing a 1-MHz clock with a 10-bit counter. The digital pattern drives a 6-bit, 1-MSPS DAC. The output of the DAC is filtered by a 150-kHz, second-order filter to remove the images, followed by a series external capacitor to block the dc current and avoid any dc current injection into the body. The output of the filter (after the dc blocking capacitor) drives a resistor setting the amplitude of the current to be injected in the body, as shown in Equation 5:

$$I(t) = VDAC / R1 = A \sin(w_0 t) \tag{5}$$

The tolerance of the resistor is ±20%; therefore, the resistor and the DAC amplitude are set so that the current injected is 375 µArms when all the elements are nominal. With a +20% error, the source is 450 µArms, and still below the 500 µArms limit.

Current flows into the body through an output analog multiplexer (mux) that allows the selection of up to six different contact points on the body. The same mux allows the connection of four external impedances for calibration. The current crosses the body impedance and a second mux selects the return path (contact) on the body, closing the loop to the output of the amplifier.

At the same time that the current is injected, a second set of multiplexers connects a differential amplifier across the same body impedance in order to measure the voltage drop created by the injected current, shown by Equation 6:

$$v(t) = A|Z|\sin(\omega_0 t + \theta)$$

where Z and θ are the module and phase of the impedance at ω_0, respectively. (6)

The output of the amplifier is routed to a pair of switches that implement the demodulation at the same frequency as the excitation current source in order to drive the control of those switches. This circuit performs a full-wave rectification of the differential amplifier output and a low-pass filter at its output, recovers the dc level, and finally routes it to the same 16-bit digitizer used in the weight-scale chain.

$$DC = \frac{2}{T}\int_{T/2} A\,|\,Z\,|\,\sin\left(\omega_0 t + \theta\right)dt = \frac{2A|Z|}{\pi} \tag{7}$$

Ultimately, the dc output is proportional to the module of the impedance. The proportionality factor can be obtained through calibration with the four external impedances. Although, with one single frequency or measurement, only the module of the impedance can be obtained; two different frequencies could be used to obtain both the real and the imaginary parts.

I/Q Demodulation

The AFE4300 includes a second circuit that with a single frequency measurement, obtains both the real and the imaginary portions, as shown in Figure 9. As explained previously, the portion of the circuit injecting the current into the body is the same for both configurations. Therefore, the circuit is the same in Figure 8 and Figure 9. The difference between them is that an I/Q demodulator is used in this second approach, as shown in Figure 9.

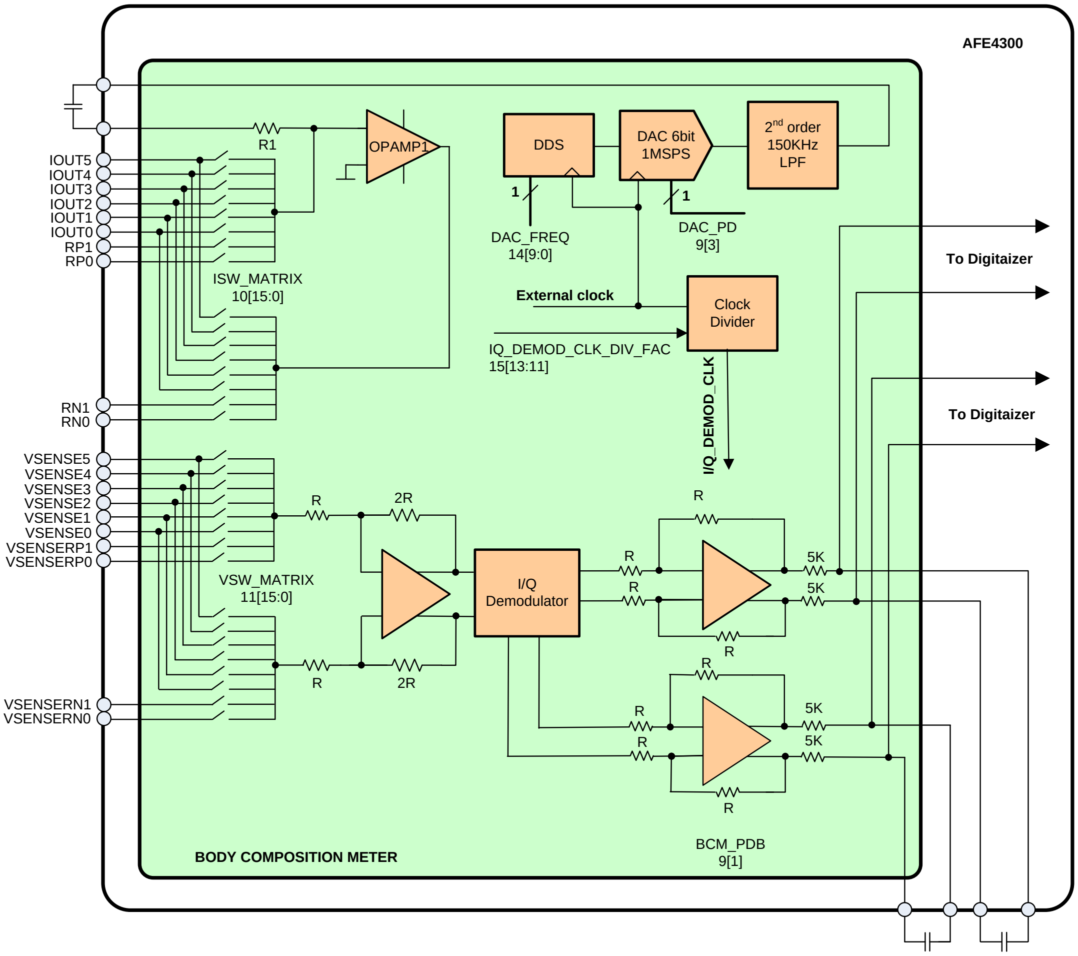


Figure 9. BCM in I/Q Demodulator Mode

As with the case of the RMS detector, a differential amplifier measures the voltage drop across the impedance, as shown in Equation 8:

$$v(t) = A|Z|\sin(\omega_0 t + \theta)$$

where:

- Z = the module of the impedance at ω_0
- θ = phase of the impedance at ω_0 (8)

The I/Q demodulator takes the v(t) signal and outputs two dc values. These two values are used to extract the impedance module and phase with a single frequency measurement. Figure 9 shows the block diagrm of the implementation. Using the I/Q demodulator helps reduce power consumption while yielding excellent performance. The local oscillator (LO) signals for the mixers are generated from the same clock driving the DDS/DAC and are of the same phase and frequency as the sinusoidal i(t) (see Equation 5). The LO signals directly control the switches on the in-phase (I) path, and after a delay of 90° degrees, control the switches on the quadrature (Q) path. This switching results in multiplying the v(t) signal by a square signal swinging from –1 to 1. Breaking down the LO signal into Fourier terms, we have Equation 9:

$$\mathrm{LO}_I(t) = \frac{4}{\pi}\left(\sin(\omega_0 t) + \frac{1}{3}\sin(3\omega_0 t) + \frac{1}{5}\sin(5\omega_0 t) + \ldots\right) \tag{9}$$

Therefore, the output voltage of the mixer is as shown in Equation 10:

$$I(t) = A|Z|\frac{4}{\pi}\left(\sin(\omega_0 t + \theta)\sin(\omega_0 t) + \frac{1}{3}\sin(\omega_0 t + \theta)\sin(3\omega_0 t) + \frac{1}{5}\sin(\omega_0 t + \theta)\sin(5\omega_0 t) + \ldots\right)$$

Where I(t) = in-phase output (not to be confused with i(t), the current injected in the impedance). (10)

Applying fundamental trigonometry gives Equation 11:

$$\sin a \ \sin b = -\frac{1}{2}\cos(a+b) + \frac{1}{2}\cos(a-b) \tag{11}$$

Each product of sinusoids can be broken up in an addition of two sinusoids. Equation 12 shows the first term:

$$\sin(\omega_0 t + \theta)\sin(\omega_0 t) = \frac{1}{2}\cos(\omega_0 t + \theta - \omega_0 t) - \frac{1}{2}\cos(\omega_0 t + \omega_0 t + \theta) = \frac{1}{2}\cos(\theta) - \frac{1}{2}\cos(2\omega_0 t + \theta) \tag{12}$$

Equation 13 shows the 2nd product:

$$\sin(\omega_0 t + \theta)\sin(3\omega_0 t) = \frac{1}{2}\cos(\omega_0 t + \theta - 3\omega_0 t) - \frac{1}{2}\cos(3\omega_0 t + \omega_0 t + \theta) = \frac{1}{2}\cos(-2\omega_0 t + \theta) - \frac{1}{2}\cos(4\omega_0 t + \theta) \tag{13}$$

And so on. Performing the same analysis on the Q side, the output voltage of the mixer is shown in Equation 14:

$$Q(t) = A|Z|\frac{4}{\pi}\left(\sin(\omega_0 t + \theta)\cos(\omega_0 t) + \frac{1}{3}\sin(\omega_0 t + \theta)\cos(3\omega_0 t) + \frac{1}{5}\sin(\omega_0 t + \theta)\cos(5\omega_0 t) + \ldots\right) \tag{14}$$

Agiain, applying fundamental trigonometry gives Equation 15:

$$\sin a \ \cos b = \frac{1}{2}\sin(a+b) + \frac{1}{2}\sin(a-b) \tag{15}$$

Each of the products can be broken up into sums. Starting with the first product, as shown in Equation 16:

$$\sin(\omega_0 t + \theta)\cos(\omega_0 t) = \frac{1}{2}\sin(2\omega_0 t + \theta) + \frac{1}{2}\sin(\theta) \tag{16}$$

And so on. Note that on I(t) as well as on Q(t), all the terms beyond the cutoff frequency of the low-pass filter at the output of the mixers (setup by the two 1-kΩ resistors and an external capacitor) are removed, leaving only the dc terms, giving Equation 17 for I_{DC} and Equation 18 for Q_{DC}:

$$I_{DC} = \frac{2A|Z|}{\pi}\cos(\theta) = K|Z|\cos(\theta) \tag{17}$$

$$Q_{DC} = \frac{2A|Z|}{\pi}\sin(\theta) = K|Z|\sin(\theta) \tag{18}$$

In reality, the LO amplitude is not known (likely, not ±1) and affects the value of K in Equation 17 and Equation 18. Solving these two equations gives Equation 19:

$$\theta = \arctan\frac{Q_{DC}}{I_{DC}}$$

$$Z = \frac{1}{K}\sqrt{{I_{DC}}^2 + {Q_{DC}}^2} \tag{19}$$

In order to account for all the nonidealities in the system, the AFE4300 also offers four extra terminals on the driving side (two to drive, and two for the currents to return) and four extra terminals on the receive/differential-amplifier side. As with RMS mode, these spare terminals allow for connection of up to four external calibration impedances, and they also compute *K*.

DIGITIZER

The digitizer block includes an analog mux and a 16-bit sigma-delta ADC.

Multiplexer

There are two levels of analog mux. The first level selects from among the outputs of the weight scale, the body composition function, two auxiliary inputs, and the battery monitor. A second mux is used to obtain the measurement of the outputs coming from the first mux, either differentially or with respect to ground (single-ended). Note that when measuring single-ended inputs, the negative range of the output codes are not used. For battery or AVDD monitoring, an internal 1/3 resistor divider is included that enables the measurement using only one reference setting for any battery voltage, thus simplifying the monitoring routine.

Analog-to-Digital Converter

The 16-bit, delta-sigma, ADC operates at a modulator frequency of 250 kHz with an f_{CLK} of 1 MHz. The full-scale voltage of the ADC is set by the voltage at its reference (V_{REF}). The reference can be either the LDO output (1.7 V) for the weight-scale front-end or the internally-generated reference signal (1.7 V) for the BCM front-end.

The decimation filter at the output of the modulator is a single-order sinc filter. The decimation rate can be programmed to provide data rates from 8 SPS to 860 SPS with an f_{CLK} of 1 MHz. Refer to the ADC_CONTROL_REGISTER1 register in the REGISTERS section for details on programming the data rates. Figure 10 shows the frequency response of the digital filter for a data rate of 8 SPS. Note that the modulator has pass band around integer multiples of the modulator sampling frequency of 250 kSPS. Set the corner frequency of the antialiasing network before the INA so that there is adequate attenuation at the first multiple of the modulator frequency.

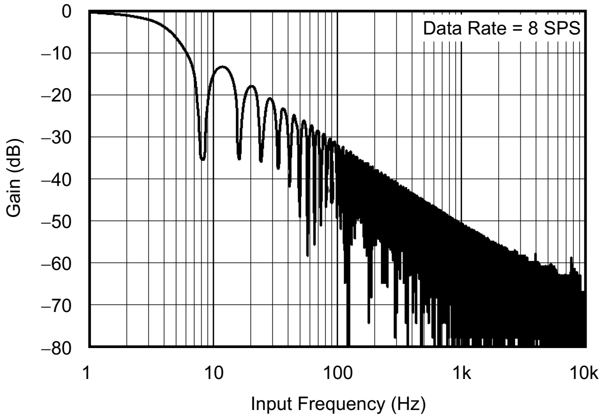


Figure 10. Frequency Response

The output format of the ADC is twos complement binary. Table 1 describes the output code versus the input signal, where full-scale (FS) is equal to the V_{REF} value.

Table 1. Input Signal Versus Ideal Output Code

INPUT SIGNAL, V_{IN} (AIN_P – AIN_N)	IDEAL OUTPUT CODE
$\geq$ FS $(2^{15} – 1)/2^{15}$	7FFFh
$+FS/2^{15}$	0001h
0	0
$–FS/2^{15}$	FFFFh
$\leq$ –FS	8000h

Operating Modes

The digitizer of the AFE4300 operates in one of two modes: continuous-conversion or single-shot. In Continuous-Conversion mode, the AFE4300 continuously performs conversions. Once a conversion has been completed, the AFE4300 places the result in the Conversion register and immediately begins another conversion. In Single-Shot mode, the AFE4300 waits until the ADC_PD bit of ADC_CONTROL_REGISTER1 is set high. Once asserted, the bit is set to '0', indicating that a conversion is currently in progress. Once conversion data are ready, the ADC_PD bit reasserts, and the device powers down. Writing a '1' to the ADC_PD bit during a conversion has no effect.

RESET AND POWER-UP

After power up, the device needs to be reset to get all the internal registers to their default state. Resetting the device is done by applying a zero pulse in the RST line for more than 20 ns after the power is stable for 5 ms. After 30 ns, the first access can be initiated (first falling edge of STE). As part of the reset process, the AFE4300 sets all of the register bits to the respective default settings. Some of the register bits must be written after reset and power up for proper operation. Refer to the REGISTERS section for more details. By default, the AFE4300 enters into a power-down state at start-up. The device interface and digital are active, but no conversion occurs until the ADC_PD bit is written to. The initial power-down state of the AFE4300 is intended to relieve systems with tight power-supply requirements from encountering a surge during power-up.

DUTY CYCLING FOR LOW POWER

For many applications, improved performance at low data rates may not be required. For these applications, the AFE4300 supports duty cycling that can yield significant power savings by periodically requesting high data-rate readings at an effectively lower data rate. For example, an AFE4300 in power-down mode with a data rate set to 860 SPS could be operated by a microcontroller that instructs a single-shot conversion every 125 ms (8 SPS). Because a conversion at 860 SPS only requires approximately 1.2 ms, the AFE4300 automatically enters power-down mode for the remaining 123.8 ms. In this configuration, the digitizer consumes about 1/100th the power of the digitizer when operated in Continuous-Conversion mode. The rate of duty cycling is completely arbitrary and is defined by the master controller.

SERIAL INTERFACE

The SPI™-compatible serial interface consists of either four signals (STE, SCLK, SDIN, and SDOUT) or three signals (in which case, STE can be tied low). The interface is used to read conversion data, read from and write to registers, and control AFE4300 operation. The data packet (between falling and rising edge of STE) is 24 bits long and is serially shifted into SDIN with the MSB first. The first eight bits (MSB) represent the address of the register being accessed and last 16 bits (LSB) represent the data to be stored or read from that address. For the eight bits address, the lower five bits [20:16] are the real address bits. Bit 21 is the read and write bit.

- '0' in bit 21 defines a write operation of the 16 data bits [15:0] into the register defined by the address bits [20:16].
- '1' in bit 21 triggers a read operation of the register defined by the address bits [20:16]. The data are output into SDOUT with every rising edge of SCLK, starting at the ninth rising edge. At the same time, data in SDIN are shifted inside the 16 data bits of that given register. Note that everytime a register is read, it must be rewritten except while reading the data output register.

SPI Enable (STE)

The STE pin selects the AFE4300 for SPI communication. This feature is useful when multiple devices share the serial bus. STE must remain low for the duration of the serial communication. When STE is taken high, the serial interface is reset, and SCLK is ignored.

Serial Clock (SCLK)

The SCLK pin features a Schmitt-triggered input and is used to clock data on the DIN and RDY pins into and out of the AFE4300. Even though the input has hysteresis, it is recommended to keep SCLK as clean as possible to prevent glitches from accidentally shifting the data. When the serial interface is idle, hold SCLK low.

Data Input (SDIN)

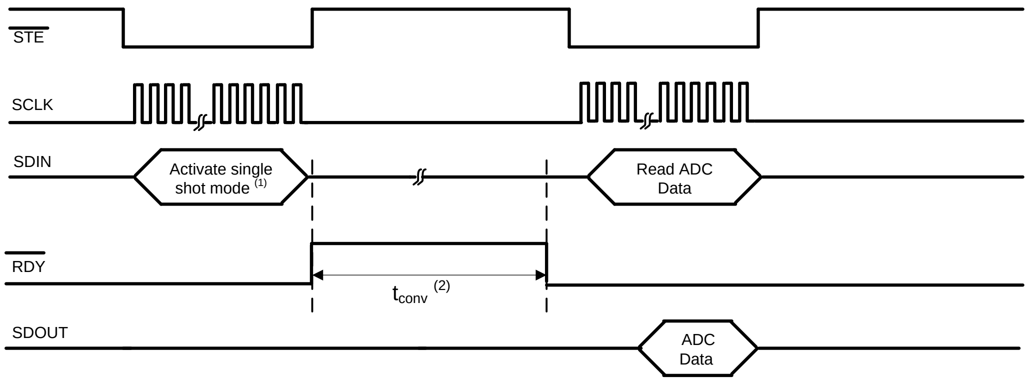
The data input pin (SDIN) is used along with SCLK to send data to the AFE4300 (opcode commands and register data). The device latches data on SDIN on the falling edge of SCLK. The AFE4300 never drives the SDIN pin. Note that everytime a register is read, it must be rewritten, except while reading the data output register.

Data Output (SDOUT)

The data output and data ready pin ($\overline{\text{RDY}}$) are used with SCLK to read conversion and register data from the AFE4300. In Read Data Continuous mode, $\overline{\text{RDY}}$ goes low when conversion data are ready, and goes high 8 µs before the data ready signal. Data on $\overline{\text{RDY}}$ are shifted out on the rising edge of SCLK. If the AFE4300 does not share the serial bus with another device, $\overline{\text{STE}}$ may be tied low. Note that every time a register is read, it must be rewritten, except while reading the data output register.

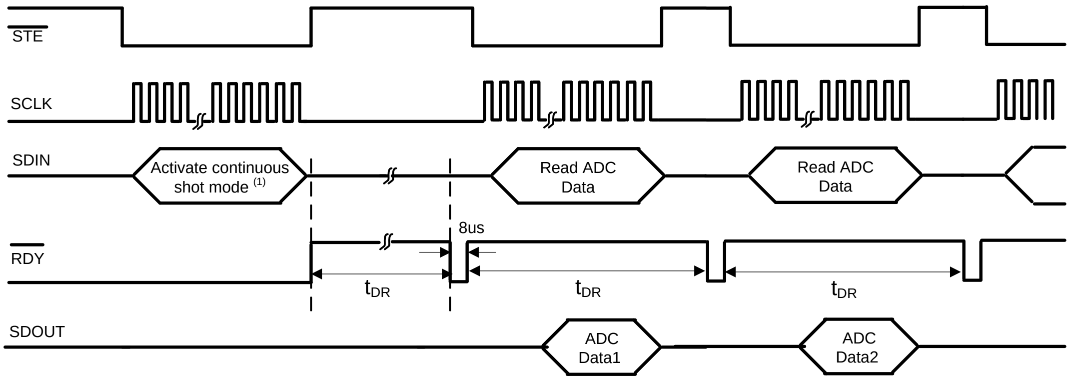
Data Ready ($\overline{\text{RDY}}$)

$\overline{\text{RDY}}$ acts as a conversion ready pin in both Continous-Conversion mode and Single-Shot mode. When in Continuous-Conversion mode, the AFE4300 provides a brief (~8 µs) pulse on the $\overline{\text{RDY}}$ pin at the end of each conversion. In Single-Shot mode, the $\overline{\text{RDY}}$ pin asserts low at the end of a conversion. Figure 11 and Figure 12 show the timing diagram for these two modes.



Note 1 : Write ADC_CONTROL_REGISTER[7] = 1, ADC_CONTROL_REGISTER1[15] = 1,
Note 2 : t_{CONV} = Time to internally set ADC_CONTROL_REGISTER[15] to logic ‘0’, ADC power up, single conversion, ADC power down, ADC_CONTROL_REGISTER1[15] internally set to logic ‘1’

Figure 11. Timing for Single-Shot Mode



Note 1 : Write ADC_CONTROL_REGISTER[7] = 0

Figure 12. Timing for Continuous Mode

REGISTERS

Register Map

Table 2 describes the registers of the AFE4300.

Table 2. Register Map

REGISTER NAME	CONTROL	ADDRESS	DESCRIPTION	DEFAULT
DEVICE CONTROLS				
DEVICE_CONTROL1	(See Description)	0x09[14:13]	Write '11' after power up and/or reset	00b
	DAC_PD	0x09[3]	Enable DAC for WS, BC measurements	0b
	PDB	0x09[2]	Chip power down	0b
	BCM_PDB	0x09[1]	Body composition measurement front-end power down	0b
	WS_PDB	0x09[0]	Weight-scale front-end power down	0b
DEVICE_CONTROL2	BAT_MON_EN1	0x0F[7]	Enables battery monitoring along with bit[0]	0b
	BAT_MON_EN2	0x0F[0]	Enables battery monitoring along with bit[7]	0b
ADC CONTROLS				
ADC_DATA_RESULT	(See Description)	0x00[15:0]	ADC data result, read only register	
ADC_CONTROL_REGISTER1	ADC_CONV_MODE	0x01[15]	Continuous-Conversion or Single-Shot mode	0b
	ADC_MEAS_MODE	0x01[13:11]	Single-Ended or Differential mode	000b
	ADC_PD	0x01[7]	ADC power down	1b
	ADC_DATA_RATE	0x01[6:4]	ADC data-rate control bits	100b
ADC_CONTROL_REGISTER2	ADC_REF_SEL	0x10[6:5]	Reference selection bits	00b
	PERIPHERAL_SEL	0x10[4:0]	Peripheral selection bits	00000b
WEIGHT-SCALE MODES				
DEVICE_CONTROL2	BRIDGE_SEL	0x0F[2:1]	Selects one of the four bridge inputs	00b
WEIGHT_SCALE_CONTROL	WS_PGA_GAIN	0x0D[14:13]	PGA gain of weight-scale front-end	00b
	OFFSET_DAC_VALUE	0x0D[5:0]	Offset DAC setting for weight-scale front-end	000000b
BCM CONTROLS				
ISW_MUX	ISW_MUXP	0x0A[15:8]	Control for switches IOUTP and RP	0x00
	ISW_MUXM	0x0A[7:0]	Control for switches IOUTN and RN	0x00
VSENSE_MUX	VSENSE_MUXP	0x0B[15:8]	Control for switches VSENSEP and VSENSEP_R	0x00
	VSENSE_MUXM	0x0B[7:0]	Control for switches VSENSEN and VSENSN_R	0x00
BCM_DAC_FREQ	DAC_FREQ	0x0E[9:0]	Sets the frequency of BCM excitation current source	0x00
IQ_MODE_ENABLE	IQ_MODE_ENABLE	0x0C[11]	Enable IQ demodulator	0b
DEVICE_CONTROL2	IQ_DEMOD_CLK_DIV_FAC	0x0F[13:11]	IQ Demodulator clock frequency	000b
MISCELLANEOUS REGISTERS				
MISC_REGISTER1	(See Description)	0x02[15:0]	Write 0x0000 after power up and/or reset	0x8000
MISC_REGISTER2	(See Description)	0x03[15:0]	Write 0xFFFF after power up and/or reset	0x7FFF
MISC_REGISTER3	(See Description)	0x1A[15:0]	Write 0x0030 after power up and/or reset	0x0000

ADC_DATA_RESULT (Address 0x00, Default 0x0000)

This register stores the most recent conversion data in twos complement format with the MSB in bit 15 and the LSB in bit 0.

ADC_CONTROL_REGISTER1 (Address 0x01, Default 0x01C3)

This register is used in conjunction with ADC_PD (bit 7). Refer to the description of the ADC_PD bit for more details.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADC_CONV_MODE	1	ADC_MEAS_MODE			0	0	1	ADC_PD	ADC_DATA _RATE			0	0	0	0

Bit 15 **ADC_CONV_MODE:** ADC conversion mode/ADC single-shot conversion start.

This bit determines the operational status of the device. This bit can only be written when in the ADC power-down mode. When read, this bit gives the status report of the conversion.

For a write status:
0 : No effect (default)
1 : Single-shot conversion mode

For a read status:
0 : Device currently performing a conversion
1 : Device not currently performing a conversion

Bit 14 **Always write ‘1’.**

Bits[13:11] **ADC_MEAS_MODE:** ADC measurement mode selection.

These bits set the ADC measurements to be either single-ended or differential.

ADC_MEAS_MODE	ADC AINP, AINM
000 (default)	A1, A2 = differential (default)
001	A1, AVSS = single-ended
010	A2, AVSS = single-ended

Bits[10:8] Always write '001'

Bit 7 **ADC_PD:** ADC Powerdown

This bit powers down the ADC_PGA and the ADC. By default, the ADC is powered down (ADC_PDN = '1').
For continuous convesion mode, this bit must to set to '0'.
For single-shot mode, this bit must be set to ‘1’ along with bit 15. During single-shot conversion mode, the device automatically powers up the ADC, triggers one ADC conversion, and then powers down the ADC.

ADC_CONV_MODE (Bit 15)	ADC_PDN (Bit 7)	MODE
X	**0**	**Continuous conversion**
0	**1 (default)**	**ADC PD**
1	**1 (default)**	**Single-shot**

Bits[6:4] **ADC_DATA_RATE:** Conversion rate select bits.

These bits select one of eight different ADC conversion rates. The data rates shown assume a master clock of 1 MHz.

000: 8 SPS
001: 16 SPS
010: 32 SPS
011: 64 SPS
100: 128 SPS (default)
101: 250 SPS
110: 475 SPS
111: 860 SPS

Bits[3:0] **Always write '0000'.** At power up, these bits are set as '0011'.

MISC_REGISTER1 (Address 0x02, Default 0x8000)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 15	**Always write ‘0’.** At power up, this bit is set as '1'.
Bits[14:0]	**Not used, always write ‘0’.** At power up, these bits are set as '0'.

MISC_REGISTER2 (Address 0x03, Default 0x7FFF)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit 15	**Always write ‘1’.** At power up, this bit is set as '0'.
Bits[14:0]	**Always write ‘1’.** At power up, these bits are set as '1'.

DEVICE_CONTROL1 (Address 0x09, Default 0x0000)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	0	0	0	0	0	0	0	0	DAC_PD	PDB	BCM_PDB	WS_PDB

Bits[15]	**Not used. Always write '0'.**
Bits[14:13]	**Not used. Always write '1'.**
Bits[12:4]	**Not used. Always write '0'.**
Bit 3	**DAC_PDB:** Power down DAC. This bit powers down the weight-scale front-end offset correction DAC and the BCM front-end current source DAC. 0: Power up DAC (default) 1: Power down DAC
Bit 2	**PDB**: Power down device. This bit in conjunction with the other power-down bits determines the power state of the device. 0: Power down (default) 1: Power up of front-end
Bit 1	**BCM_PDB:** Body composition measurement front-end power-down bit. 0: Power down body compositionmeasurement front-end (default) 1: Power up body composition measurement front-end. Power down the weight scale when powering up the BCM.
Bit 0	**WS_PDB:** Weight-scale front-end power-down bit. 0: Power down weight-scale front-end (default) 1: Power up weight-scale front-end. Power down BCM when powering up the weight scale.

Table 3 shows the available power-down modes.

Table 3. Power-Down Modes

DAC_PDB (Bit3)	PDB (Bit 2)	BCM_PDB (Bit 1)	WS_PDB (Bit 0)	ADC_PD (Bit 7, ADC Control Register)	MODE
X	0	0	0	1	Full device power down
1	1	0	0	1	Sleep mode
0	1	1	0	0	Weight-scale power down, body composition measurement
0	1	0	1	0	Body composition measurement power down, weight-scale measurement
0	1	0	0	0	Weight-scale and body composition measurement power down (aux/battery measurement)

ISW_MUX (Address 0x0A, Default 0x0000)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IOUTP5	IOUTP4	IOUTP3	IOUTP2	IOUTP1	IOUTP0	RP1	RP0	IOUTN5	IOUTN4	IOUTN3	IOUTN2	IOUTN1	IOUTN0	RN1	RN0

Bits[15:10] **IOUTP[5:0]**

These bits close the switches routing IOUTPx to the negative input of OPAMP1.

0: Switch is open (default)
1: Switch is closed

Bits[9:8] **RP[1:0]**

These bits close the switches routing the calibration signal to the negative input of OPAMP1.

0: Switch is open (default)
1: Switch is closed

Bits[7:2] **IOUTN[5:0]**

These bits close the switches routing IOUTNx to the output of OPAMP1.

0: Switch is open (default)
1: Switch is closed

Bits[1:0] **RN[1:0]**

These bits close the switches routing the calibration signal to the output of OPAMP1.

0: Switch is open (default)
1: Switch is closed

VSENSE_MUX (Address 0x0B, Default 0x0000)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VSENSEP5	VSENSEP4	VSENSEP3	VSENSEP2	VSENSEP1	VSENSEP0	VSENSEP_R1	VSENSEP_R0	VSENSEN5	VSENSEN4	VSENSEN3	VSENSEN2	VSENSEN1	VSENSEN0	VSENSEM_R1	VSENSEM_R0

Bits[15:10] **VSENSEPx[5:0]**

These bits close the switches routing VSENSEPx to the positive input of the receive amplifier.

0: Switch is open (default)
1: Switch is closed

Bits[9:8] **VSENSEP_Rx[1:0]**

These bits close the switches routing the calibration signal to the positive input of the receive amplifier.

0: Switch is open (default)
1: Switch is closed

Bits[7:2] **VSENSENx[5:0]**

These bits close the switches routing VSENSENx to the negative input of the receive amplifier.

0: Switch is open (default)
1: Switch is closed

Bits[1:0] **VSENSEM_Rx[1:0]**

These bits close the switches routing the calibration signal to the negative input of the receive amplifier.

0: Switch is open (default)
1: Switch is closed

IQ_MODE_ENABLE (Address 0x0C, Default 0x0000)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	IQ_ MODE_ ENABLE	0	0	0	0	0	0	0	0	0	0	0

Bits[15:12]	**Not used. Always write '0'.**
Bit 11	**IQ_MODE_ENABLE:** Enable the I/Q demodulator. This bit sets the impedece measurement mode to either full-wave rectifier mode or I/Q demodulator mode. For I/Q Demodulator mode, the DAC_FREQ bits of the BCM_DAC_FREQ register and the IQ_DEMOD_CLK_DIV_FAC bits of the DEVICE_CONTROL2 register must be set appropriately. Refer to the respective register section for more details. 0: Full-Wave Rectifier mode (default) 1: I/Q Demodulator mode
Bits[10:0]	**Not used. Always write '0'.**

WEIGHT_SCALE_CONTROL (Address 0x0D, Default 0x0000)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	WS_PGA_GAIN		0	0	0	0	0	0	0	OFFSET_DAC_VALUE					

Bit 15	**Not used. Always write '0'.**
Bits[14:13]	**WS_PGA_GAIN:** Sets the second-stage gain of the weight-scale front-end. 00: Gain = 1 (default) 01: Gain = 2 10: Gain = 3 11: Gain = 4
Bits[12:6]	**Not used. Always write '0'.**
Bit[5:0]	**OFFSET_DAC_VALUE:** Offset correction DAC setting. These bits set the value for the DAC used to correct the input offset of the weight-scale front-end. The correction is made at the second stage. The offset correction at the output of the first stage is given by OFFSET_DAC_VALUE × 31.2 mV. Note that OFFSET_DAC_VALUE is a number from –32 to 31, in twos complement; default is '000000'.

BCM_DAC_FREQ (Address 0x0E, Default 0x0000)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	DAC8	DAC7	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0

Bits[15:9]	**Not used. Always write '0'.**
Bits[8:0]	**DAC[8:0]:** Sets the frequency of the BCM excitation current source. The DAC output frequency is given by DAC[9:0] × f_{CLK} / 1024, where f_{CLK} is the frequency of the device input clock (pin 79). All combinations of the DAC frequency can be used for the full-wave rectifier mode. However, only certain combinations of the DAC frequency can be used for the IQ demodulator mode. Refer to the description of the DEVICE_CONTROL2 register for more details. For example, with f_{CLK} = 1 MHz: DAC = 0x00FF → 255 kHz DAC = 0x0001 → 1 kHz

DEVICE_CONTROL2 (Address 0x0F, Default 0x0000)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	IQ_DEMOD_CLK_DIV_FAC			0	0	0	BAT_ MON_ EN1	0	0	0	0	BRIDGE_SEL		BAT_ MON_ EN0

Bits[15:14] **Not used. Always write '0'.**

Bits[13:11] **IQ_DEMOD_CLK_DIV_FAC:** I/Q demodulator clock frequency.

The clock for the IQ demodulator (IQ_DEMOD_CLK signal) is internally generated from the device input clock (f_{CLK}) by a divider controlled by this register. Note that the IQ_DEMOD_CLK should be four times the BCM_DAC_FREQ so that it can generate the phases for the mixers (that is, IQ_DEMOD_CLK = f_{CLK} / (IQ_DEMOD_CLK_DIV_FAC) = BCM_DAC_FREQ × 4)

000: Divide by 1 (default)
001: Divide by 2
010: Divide by 4
011: Divide by 8
100: Divide by 16
Others: Divide by 32

Bit 7 **BAT_MON_EN1:** This bit (along with BAT_MON_EN0, bit 0) enables battery monitoring.

When disabled, the battery monitoring block is powered down to save power. See the description of BAT_MON_EN0, bit 0.

Bits[6:3] **Not used. Always write '0'.**

Bits[2:1] **BRIDGE_SEL:** Selects one of the four input pairs to be routed to the weight-scale front-end.

00: Bridge 1 (INP1, INM1) connected to the weight-scale front-end (default)
01: Bridge 2 (INP2, INM2) connected to the weight-scale front-end
10: Bridge 3 (INP3, INM3) connected to the weight-scale front-end
11: Bridge 4 (INP4, INM4) connected to the weight-scale front-end.

Bit 0 **BAT_MON_EN0:** This bit along with BAT_MON_EN1 (Bit[7]) enables battery monitoring.

00: Monitor disabled (default)
11: Monitor enabled (AVDD / 3)

NOTE: The PERIPHERAL_SEL bits of the ADC_CONTROL_REGISTER2 must be set to '10001' in order to route the battey monitor output to the ADC.

ADC_CONTROL_REGISTER2 (Address 0x10, Default 0x0000)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	ADC_REF_SEL		PERIPHERAL_SEL				

Bits[15:7] **Not used. Always write '0'.**

Bits[6:5] **ADC_REF_SEL[1:0]:** Selects the reference for the ADC.

00: ADCREF connected to VLDO. Used for ratiometric weight-scale measurement (default).
01, 10: Do not use
11: ADCREF connected to VREF (internal voltage reference generator). Used for impedance measurement.

Bits[4:0] **PERIPHERAL_SEL[4:0]:** Selects the signals that are connected to the ADC.

00000: Output of the weight-scale front-end (default)
00011: Output of the body composition measurement front-end (OUTP_FILT/OUTM_FILT)
00101: Output of the body composition measurement front-end (OUTP_Q_FILT/OUTM_Q_FILT)
01001: AUX1 signal for single-ended measurement. Also set bit[13:11] of the ADC_CONTROL_REGISTER1 to '001'.
10001: AUX2 signal for single-ended measurement. Also set bit[13:11] of the ADC_CONTROL_REGISTER1 to '010'.
11001: AUX2 and AUX1 signal for differential measurement (AUX2-AUX1). Also set bit[13:11] of the ADC_CONTROL_REGISTER1 to 000.

NOTE: All other bit combinations are invalid.

MISC_REGISTER3 (Address 0x1A, Default 0x0000)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

Bits[15:6]	**Not used. Always write '0'.**
Bits[5:4]	**Always write '1'.**
Bits[3:0]	**Not used. Always write '0'.**

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from the page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
AFE4300PN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	AFE4300	Samples
AFE4300PNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	AFE4300	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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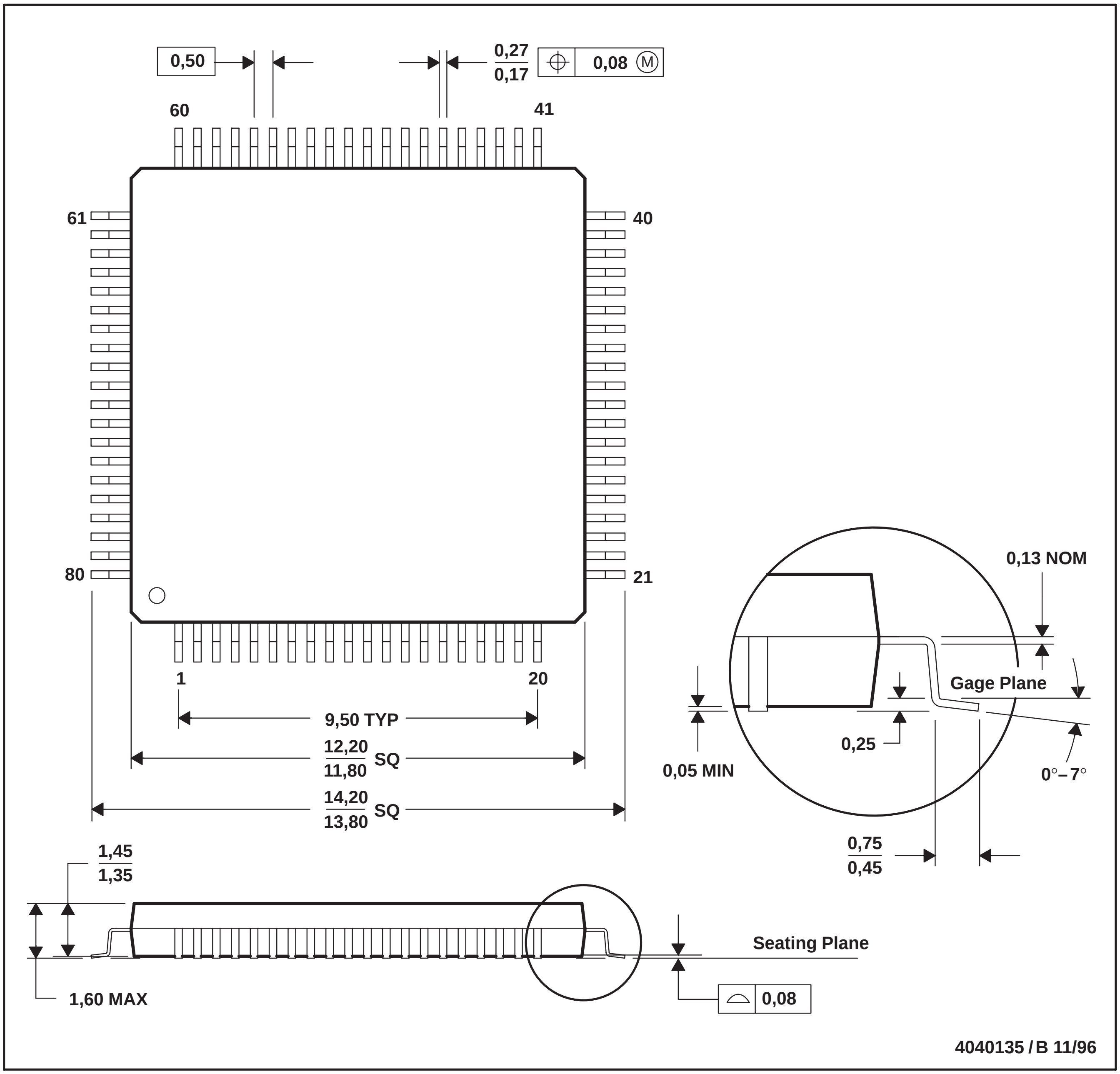
PN (S-PQFP-G80) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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