SRC4192-Q1 192-kHz Stereo Asynchronous Sample-Rate Converters

1 Features

- Automatic Sensing of the Input-to-Output Sampling Ratio
- Wide Input-to-Output Sampling Range: 16:1 to 1:16
- Supports Input and Output Sampling Rates Up to 212 kHz
- Dynamic Range: 144 dB (–60-dbFS Input, BW = 20 Hz to f_S/2, A-Weighted)
- THD+N: –140 dB (0-dbFS Input, BW = 20 Hz to f_S/2)
- Attenuates Sampling and Reference Clock Jitter
- High-Performance, Linear-Phase Digital Filtering with Stop Band Attenuation Greater than 140 dB
- Flexible Audio Serial Ports:
  - Master or Slave-Mode Operation
  - Supports I^2S, Left-Justified, Right-Justified, and TDM Data Formats
  - Supports 16-Bit, 18-Bit, 20-Bit, or 24-Bit Audio Data
  - TDM Mode Allows Daisy-Chaining of up to Eight Devices
- Low Group Delay Option for Interpolation Filter
- Power Down Mode
- Operates From a Single 3.3-V Power Supply
- Small 28-Pin SSOP Package
- Pin Compatible with the AD1896

2 Applications

- Digital Audio Workstations
- Audio Distribution and Broadcast Systems
- High-End A/V Receivers

3 Description

The SRC4192-Q1 device is an asynchronous, sample-rate converter designed for professional and broadcast audio applications. The SRC4192-Q1 device combines a wide input-to-output sampling ratio with outstanding dynamic range and ultra-low distortion. Input and output serial ports support standard audio formats, as well as a Time Division Multiplexed (TDM) mode. Flexible audio interfaces allow the SRC4192-Q1 device to connect to a wide range of audio data converters, digital audio receivers and transmitters, and digital signal processors.

The SRC4192-Q1 device is a standalone, pin-programmed device, with control pins for mode, data format, mute, bypass, and low group-delay functions.

The SRC4192-Q1 device can operate from a single 3.3-V power supply. A separate digital I/O supply (V_{IO}) operates over the 1.65-V to 3.6-V supply range, allowing greater flexibility when interfacing to current and future generation signal processors and logic devices. The device is available in a 28-pin SSOP package.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SRC4192-Q1	SSOP (28)	5.30 mm × 10.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic

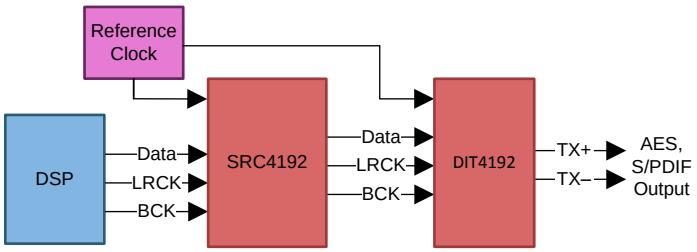


Table of Contents

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

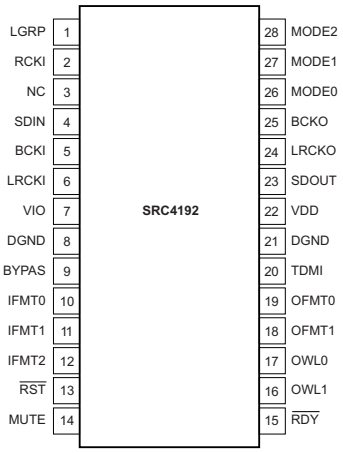
Changes from Revision Preview (October 2015) to Revision A	Page
• Added Rest of documentation for Q1 device release.	1

6 Device Comparison Table

Part Number	SNR (dB A-Weighted)	Channel Count	Control Interface	Other Features
SRC4184	128	4	SW (SPI)	
SRC4190	128	2	HW (Hardware)	Q1 Version Available
SRC4192	144	2	HW	Q1 Version Available
SRC4193	144	2	SW (SPI) (Software - SPI)	
SRC4194	144	4	SW (SPI)	
SRC4382	128	2	SW (SPI) / HW	Integrated S/PDIF Transceiver
SRC4392	144	2	SW (SPI) / HW	Integrated S/PDIF Transceiver

7 Pin Configuration and Functions

DB Package
28-Pin SSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BCKI	5	I	Input port bit clock I/O
BCKO	25	O	Output port bit clock I/O
BYPAS	9	I	ASRC bypass control input (Active High)
DGND	8	–	Digital ground
	21		
IFMT0	10	I	Input port data format control input
IFMT1	11	I	Input port data format control input
IFMT2	12	I	Input port data format control input
LGRP	1	I	Low group delay control input (active high)
LRCKI	6	I	Input port left/right word clock I/O
LRCKO	24	O	Output port left/right word clock I/O
MODE0	26	I	Serial port mode control input
MODE1	27	I	Serial port mode control input
MODE2	28	I	Serial port mode control input
MUTE	14	I	Output mute control input (active high)
NC	3	–	No connection
OFMT0	19	I	Output port data format control input
OFMT1	18	I	Output port data format control input
OWL0	17	I	Output port data word length control input
OWL1	16	I	Output port data word length control input
RCKI	2	I	Reference Clock Input
$\overline{RDY}$	15	O	ASRC Ready Status Output (Active Low)
$\overline{RST}$	13	I	Reset Input (Active Low)
SDIN	4	I	Audio Serial Data Input
SDOUT	23	O	Audio Serial Data Output
TDMI	20	I	TDM Data Input (Connect to DGND when not in use)
V_{DD}	22	I	Digital Core Supply, 3.3 V
V_{IO}	7	I	Digital I/O Supply, 1.65 V to V_{DD}

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply Voltage	V_{DD}	–0.3	4	V
	V_{IO}	–0.3	4	
Digital Input Voltage		–0.3	4	
Operating Temperature		–40	125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage	V_{DD}	3	3.3	3.6	V
	V_{IO} 1.8 V	1.65	1.8	1.95	
	V_{IO} 3.3 V	3	3.3	3.6	
Operating temperature		–40		125	°C

8.4 Thermal Information

THERMAL METRIC (1)		SRC4192-Q1 DB (SSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	78.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	38.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

All parameters specified with T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE (1)						
	Resolution			24		Bits
f_{SIN}	Input sampling frequency		4		212	kHz
f_{SOUT}	Output sampling frequency		4		212	kHz

(1) Dynamic performance measured with an Audio Precision System Two Cascade or Cascade Plus.

Electrical Characteristics (continued)

All parameters specified with T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input: output sampling ratio	Upsampling				1:16	
	Downsampling				16:1	
Dynamic range	44.1 kHz; 48 kHz	BW = 20 Hz to f_{SOUT}/2, –60-dBFS Input f_{IN} = 1 kHz, Unweighted (add 3 dB to spec for A-weighted result)		140		dB
	48 kHz; 44.1 kHz			140		
	48 kHz; 96 kHz			140		
	44.1 kHz; 192 kHz			138		
	96 kHz; 48 kHz			141		
	192 kHz; 12 kHz			141		
	192 kHz; 32 kHz			141		
	192 kHz; 48 kHz			141		
	32 kHz; 48 kHz			140		
	12 kHz; 192 kHz			138		
Total harmonic distortion + noise	44.1 kHz; 48 kHz	BW = 20 Hz to f_{SOUT}/2, 0-dBFS Input f_{IN} = 1 kHz, Unweighted		–140		dB
	48 kHz; 44.1 kHz			–140		
	48 kHz; 96 kHz			–140		
	44.1 kHz; 192 kHz			–137		
	96 kHz; 48 kHz			–140		
	192 kHz; 12 kHz			–140		
	192 kHz; 32 kHz			–141		
	192 kHz; 48 kHz			–141		
	32 kHz; 48 kHz			–140		
	12 kHz; 192 kHz			–137		
Interchannel gain mismatch				0		dB
Interchannel phase deviation				0		°
Mute attenuation		24-Bit Word Length, A-weighted		–144		dB
DIGITAL INTERPOLATION FILTER CHARACTERISTICS						
Passband					0.4535 × f_{SIN}	Hz
Passband ripple					±0.007	dB
Transition band			0.4535 × f_{SIN}		0.5465 × f_{SIN}	Hz
Stop band			0.5465 × f_{SIN}			Hz
Stop band attenuation			–144			dB
Normal group delay (LGRP = 0)		Decimation Filter On (DFLT = 0)		102.53125 / f_{SIN}		s
		Decimation Filter Off (DFLT = 1)		102 / f_{SIN}		

Electrical Characteristics (continued)

All parameters specified with T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Low group delay (LGRP = 1)	Decimation Filter On (DFLT = 0)		70.53125 / f_{SIN}		s
		Decimation Filter Off (DFLT = 1)		70 / f_{SIN}		
DIGITAL DECIMATION FILTER CHARACTERISTICS						
	Passband				0.4535 × f_{SOUT}	Hz
	Passband ripple				±0.008	dB
	Transition band		0.4535 × f_{SOUT}		0.5465 × f_{SOUT}	Hz
	Stop band		0.5465 × f_{SOUT}			Hz
	Stop band attenuation		–143			dB
	Group delay – decimation filter			36.46875 / f_{SOUT}		s
DIGITAL I/O CHARACTERISTICS						
V_{IH}	High-level input voltage		0.7 × V_{IO}		V_{IO}	V
V_{IL}	Low-level input voltage		0		0.3 × V_{IO}	V
I_{IH}	High-level input current (for pins other than IFMT0, IFMT1, IFMT2, OFMT0, OFMT1, OWL0)			0.5	10	µA
I_{IH}	High-level input current for IFMT0, IFMT1, IFMT2, OFMT0, OFMT1, OWL0 (SRC4192 specific)			0.5	25	µA
I_{IL}	Low-level input current			0.5	10	µA
V_{OH}	High-level output voltage	I_O = –4 mA	0.8 × V_{IO}		V_{IO}	V
V_{OL}	Low-level output voltage	I_O = +4 mA	0		0.2 × V_{IO}	V
C_{IN}	Input Capacitance			3		pF
POWER SUPPLIES						
	Operating voltage, V_{DD}		3	3.3	3.6	V
	Operating voltage, V_{IO}		1.65	3.3	3.6	V
	Supply current, I_{DD}, power down	V_{DD} = 3.3 V, V_{IO} = 3.3 V, $\overline{RST}$ = 0, No Clocks			100	µA
	Supply current, I_{DD}, dynamic	V_{DD} = 3.3 V, V_{IO} = 3.3 V, f_{SIN} = f_{SOUT} = 192 kHz		66		mA
	Supply current, I_{IO}, power down	V_{DD} = 3.3 V, V_{IO} = 3.3 V, $\overline{RST}$ = 0, No Clocks			100	µA
	Supply current, I_{IO}, dynamic	V_{DD} = 3.3 V, V_{IO} = 3.3 V, f_{SIN} = f_{SOUT} = 192 kHz		2		mA
	Total power dissipation, P_D, power down	V_{DD} = 3.3 V, V_{IO} = 3.3 V, $\overline{RST}$ = 0, No Clocks			660	µW
	Total power dissipation, P_D, dynamic	V_{DD} = 3.3 V, V_{IO} = 3.3 V, f_{SIN} = f_{SOUT} = 192 kHz		225		mW

8.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE CLOCK TIMING						
	RCKI frequency	f_{SMIN} = min (f_{SIN}, f_{SOUT}), f_{SMAX} = max (f_{SIN}, f_{SOUT})	128 × f_{SMIN}		50	MHz
t_{RCKIP}	RCKI period		20		1 / (128 × f_{SMIN})	ns

Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RCKIH}	RCKI pulsewidth high		0.4 × t_{RCKIP}			ns
t_{RCKIL}	RCKI pulsewidth low		0.4 × t_{RCKIP}			ns
RESET TIMING						
t_{RSTL}	$\overline{RST}$ pulse width low		500			ns
INPUT SERIAL PORT TIMING						
t_{LRIS}	LRCKI to BCKI setup time		10			ns
t_{SIH}	BCKI pulsewidth high		10			ns
t_{SIL}	BCKI pulsewidth low		10			ns
t_{LDIS}	SDIN data setup time		10			ns
t_{LDIH}	SDIN data hold time		10			ns
OUTPUT SERIAL PORT TIMING						
t_{DOPD}	SDOUT data delay time				10	ns
t_{DOH}	SDOUT data hold time		2			ns
t_{SOH}	BCKO pulsewidth high		10			ns
t_{SOL}	BCKO pulsewidth low		5			ns
TDM MODE TIMING						
t_{LROS}	LRCKO setup time		10			ns
t_{LROH}	LRCKO hold time		10			ns
t_{TDMS}	TDMI data setup time		10			ns
t_{TDMH}	TDMI data hold time		10			ns
SPI TIMING						
	CCLK frequency				25	MHz
t_{CDS}	CDATA setup time		12			ns
t_{CDH}	CDATA hold time		8			ns
t_{CSCR}	$\overline{CS}$ falling to CCLK rising		15			ns
t_{CFCS}	CCLK falling to $\overline{CS}$ rising		12			ns

8.7 Typical Characteristics

At T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V, unless otherwise noted.

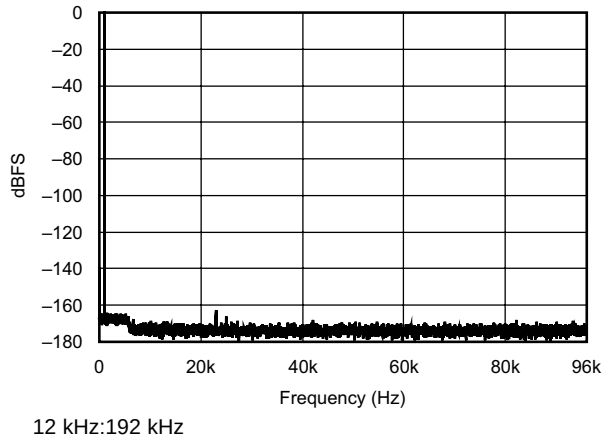


Figure 1. FFT With 1-kHz Input Tone at 0 dBFS

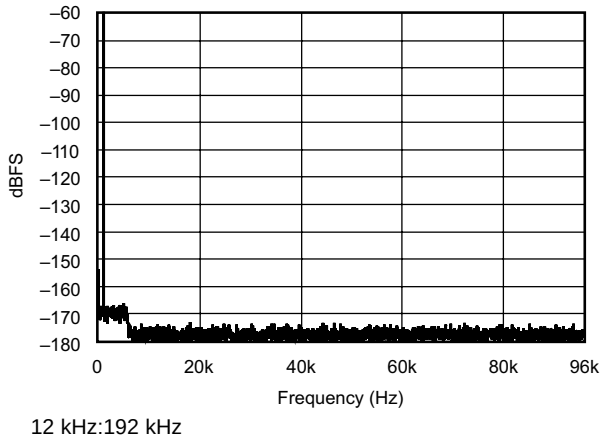
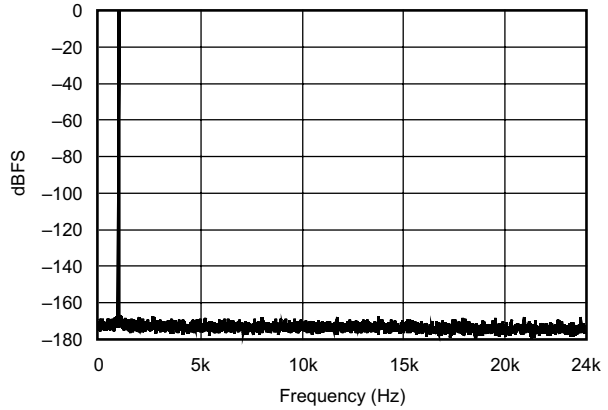


Figure 2. FFT With 1-kHz Input Tone at –60 dBFS

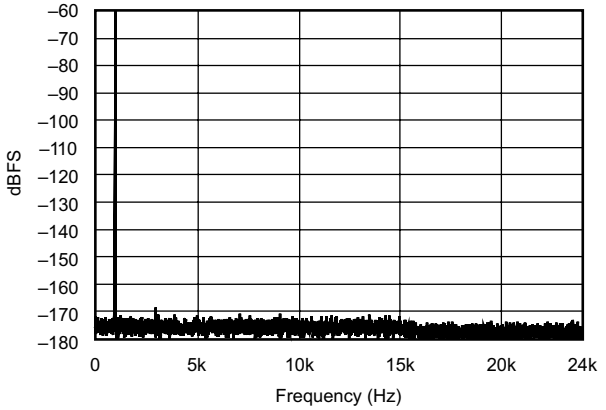
Typical Characteristics (continued)

At T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V, unless otherwise noted.



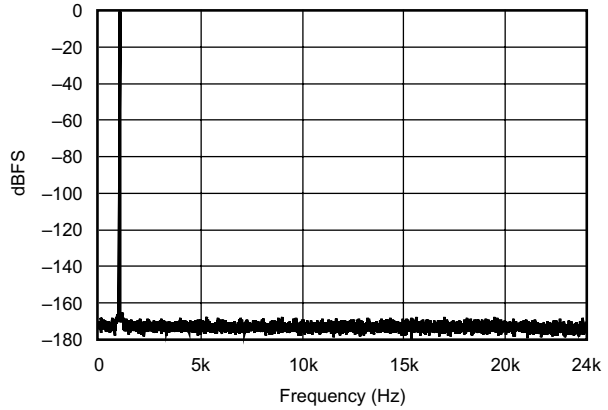
32 kHz:48 kHz

Figure 3. FFT With 1-kHz Input Tone at 0 dBFS



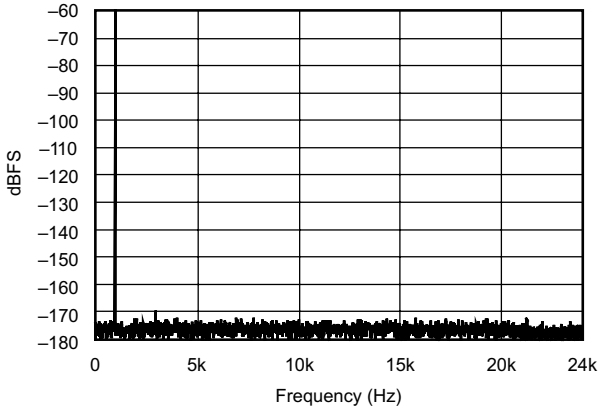
32 kHz:48 kHz

Figure 4. FFT With 1-kHz Input Tone at –60 dBFS



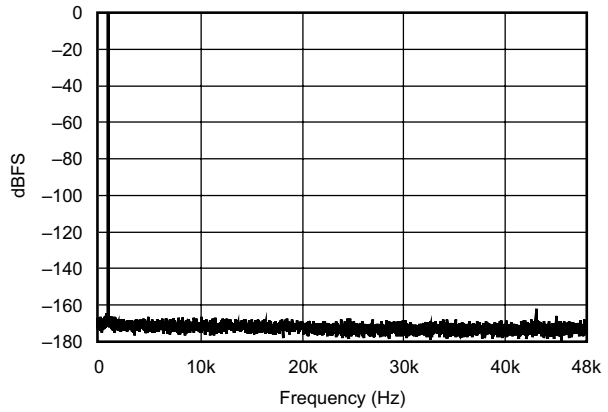
44.1 kHz:48 kHz

Figure 5. FFT With 1-kHz Input Tone at 0 dBFS



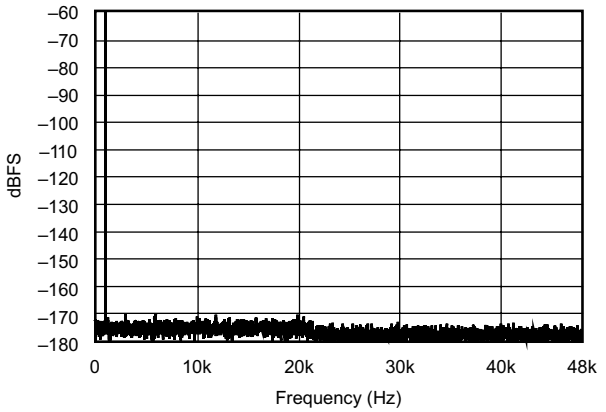
44.1 kHz:48 kHz

Figure 6. FFT With 1-kHz Input Tone at –60 dBFS



44.1 kHz:96 kHz

Figure 7. FFT With 1-kHz Input Tone at 0 dBFS

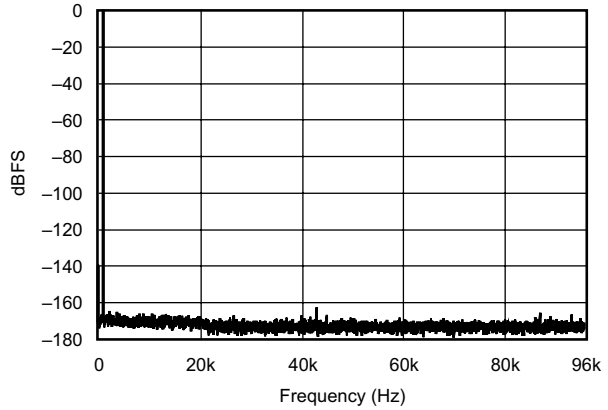


44.1 kHz:96 kHz

Figure 8. FFT With 1-kHz Input Tone at –60 dBFS

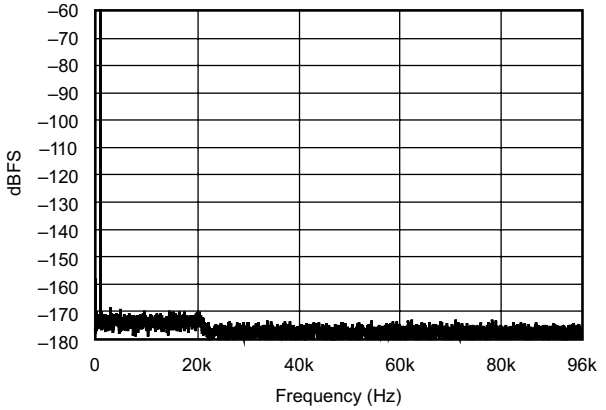
Typical Characteristics (continued)

At T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V, unless otherwise noted.



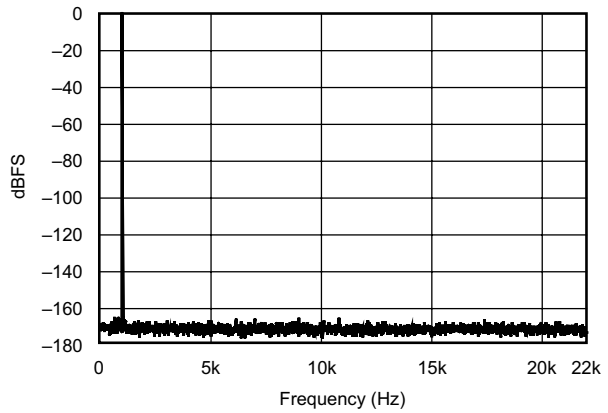
44.1 kHz:192 kHz

Figure 9. FFT With 1-kHz Input Tone at 0 dBFS



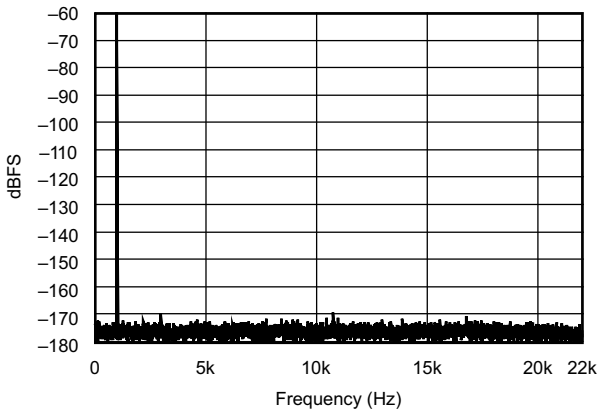
44.1 kHz:192 kHz

Figure 10. FFT With 1-kHz Input Tone at –60 dBFS



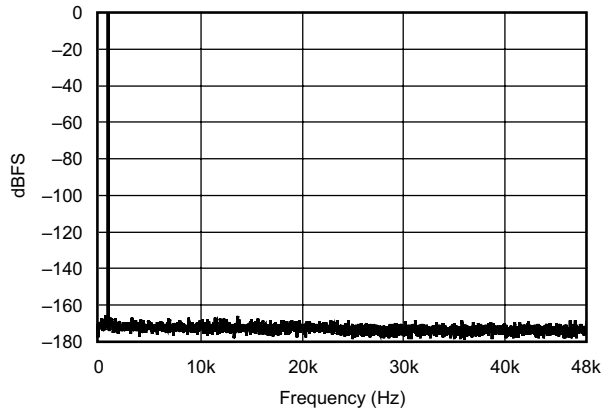
48 kHz:44.1 kHz

Figure 11. FFT With 1-kHz Input Tone at 0 dBFS



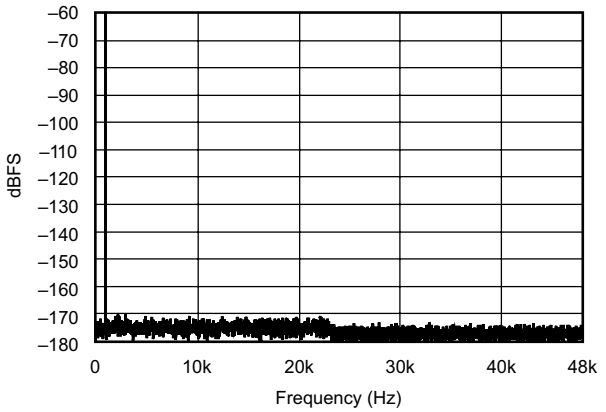
48 kHz:44.1 kHz

Figure 12. FFT With 1-kHz Input Tone at –60 dBFS



48 kHz:96 kHz

Figure 13. FFT With 1-kHz Input Tone at 0 dBFS

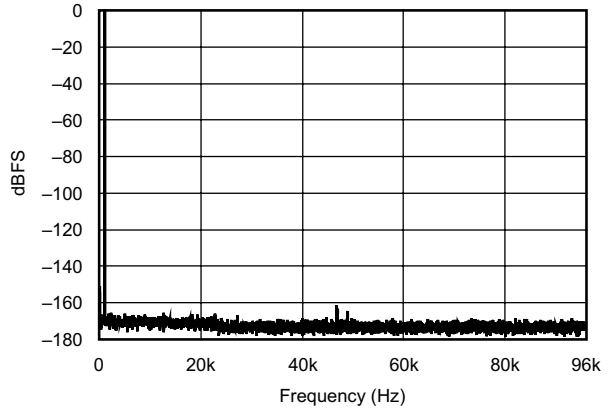


48 kHz:96 kHz

Figure 14. FFT With 1-kHz Input Tone at –60 dBFS

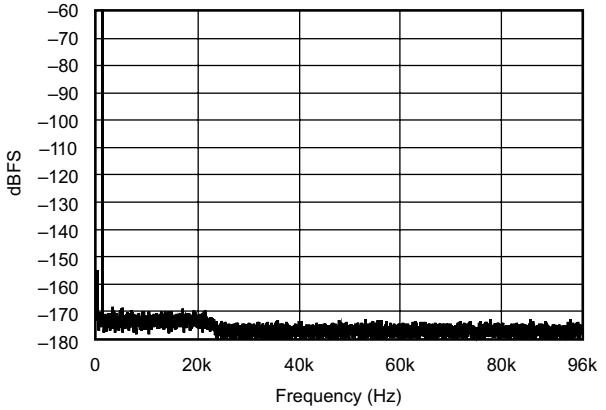
Typical Characteristics (continued)

At T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V, unless otherwise noted.



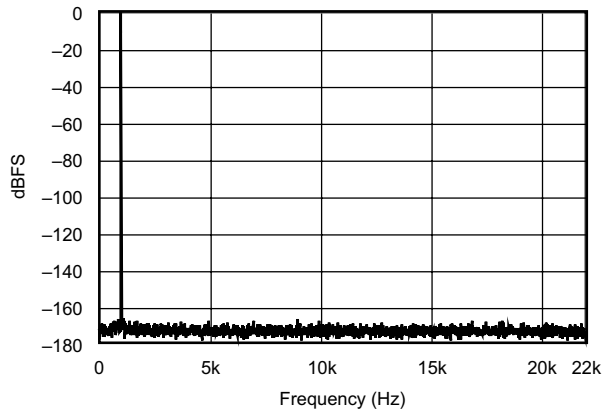
48 kHz:192 kHz

Figure 15. FFT With 1-kHz Input Tone at 0 dBFS



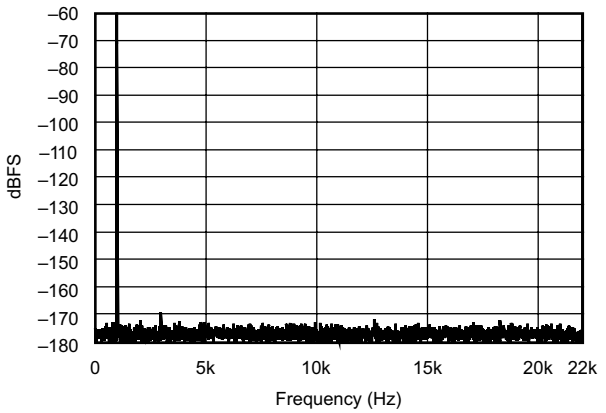
48 kHz:192 kHz

Figure 16. FFT With 1-kHz Input Tone at –60 dBFS



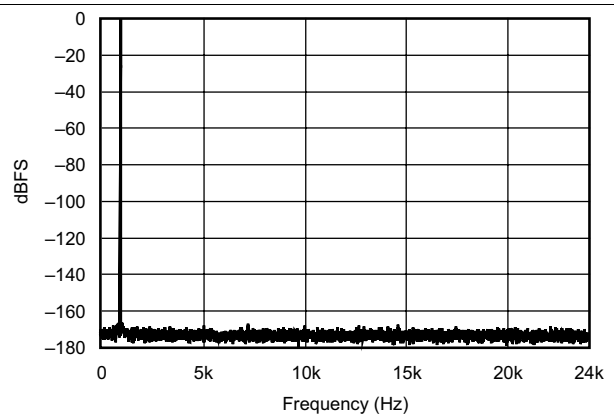
96 kHz:44.1 kHz

Figure 17. FFT With 1-kHz Input Tone at 0 dBFS



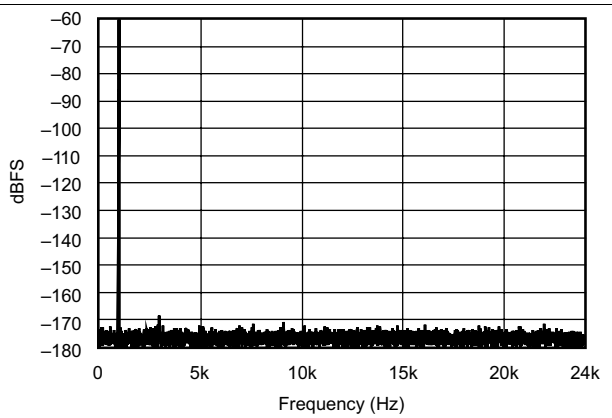
96 kHz:44.1 kHz

Figure 18. FFT With 1-kHz Input Tone at –60 dBFS



96 kHz:48 kHz

Figure 19. FFT With 1-kHz Input Tone at 0 dBFS

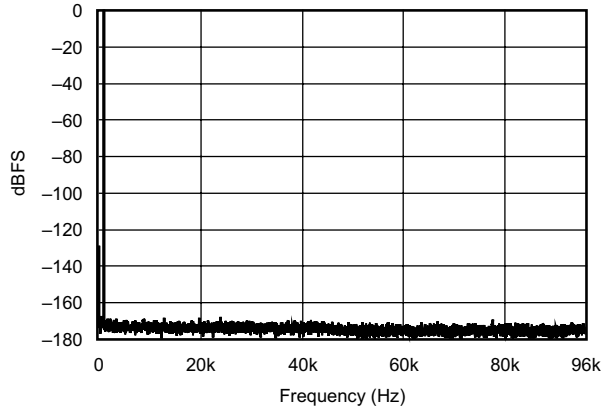


96 kHz:48 kHz

Figure 20. FFT With 1-kHz Input Tone at –60 dBFS

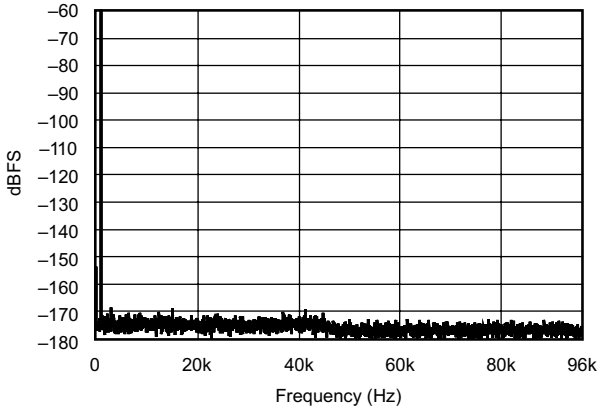
Typical Characteristics (continued)

At T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V, unless otherwise noted.



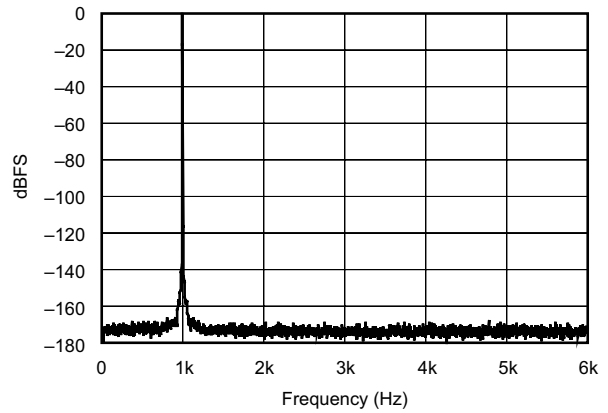
96 kHz:192 kHz

Figure 21. FFT With 1-kHz Input Tone at 0 dBFS



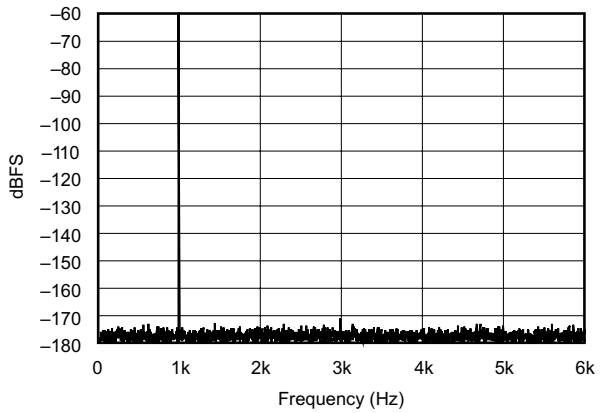
96 kHz:192 kHz

Figure 22. FFT With 1-kHz Input Tone at –60 dBFS



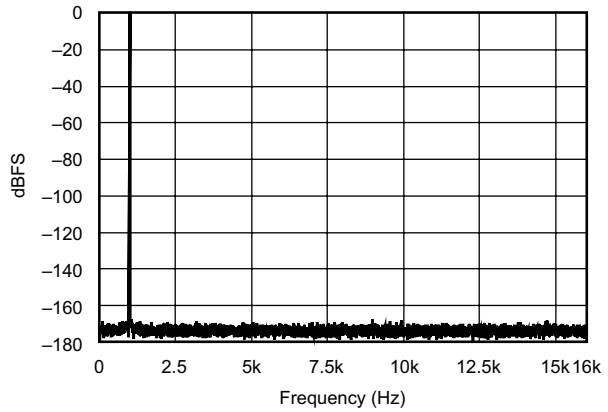
192 kHz:12 kHz

Figure 23. FFT With 1-kHz Input Tone at 0 dBFS



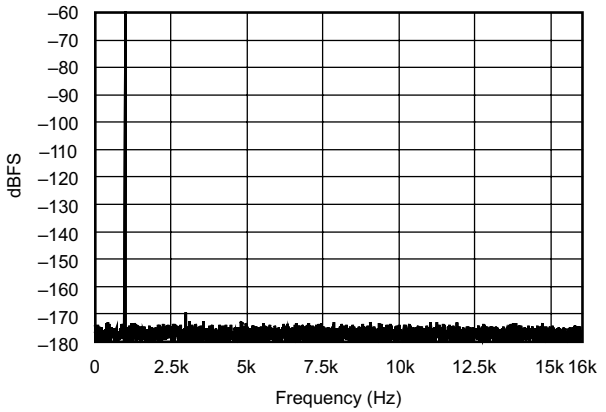
192 kHz:12 kHz

Figure 24. FFT With 1-kHz Input Tone at –60 dBFS



192 kHz:32 kHz

Figure 25. FFT With 1-kHz Input Tone at 0 dBFS

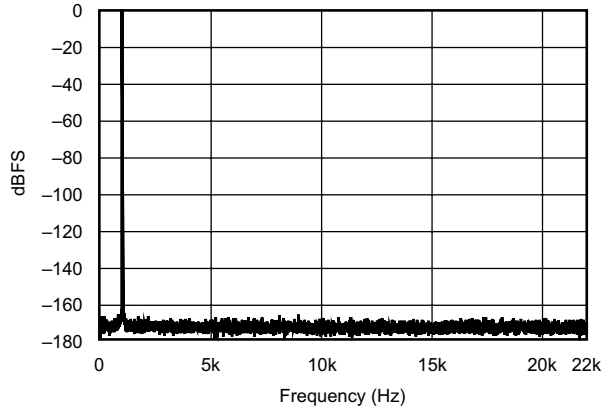


192 kHz:32 kHz

Figure 26. FFT With 1-kHz Input Tone at –60 dBFS

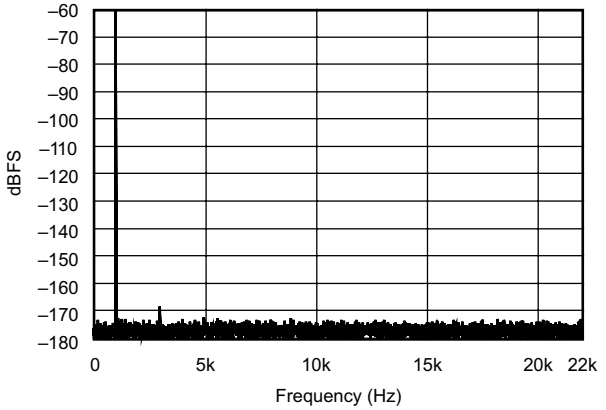
Typical Characteristics (continued)

At T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V, unless otherwise noted.



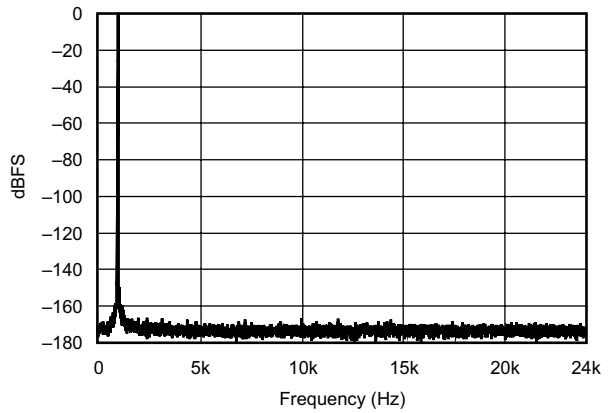
192 kHz:44.1 kHz

Figure 27. FFT With 1-kHz Input Tone at 0 dBFS



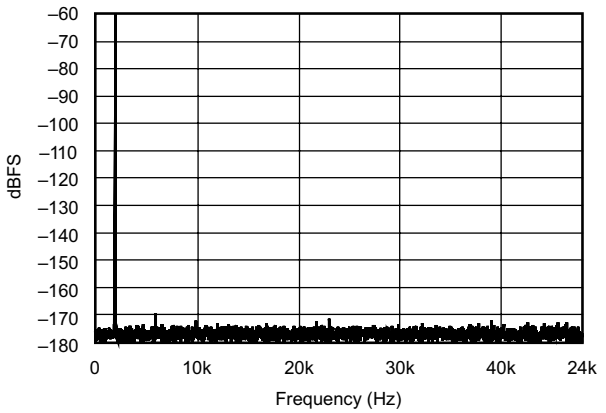
192 kHz:44.1 kHz

Figure 28. FFT With 1-kHz Input Tone at –60 dBFS



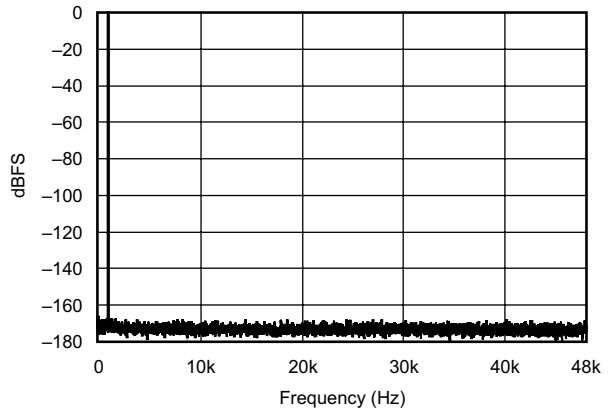
192 kHz:48 kHz

Figure 29. FFT With 1-kHz Input Tone at 0 dBFS



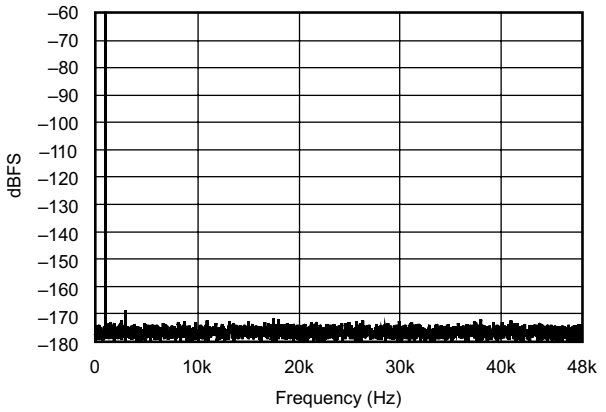
192 kHz:48 kHz

Figure 30. FFT With 1-kHz Input Tone at –60 dBFS



192 kHz:96 kHz

Figure 31. FFT With 1-kHz Input Tone at 0 dBFS

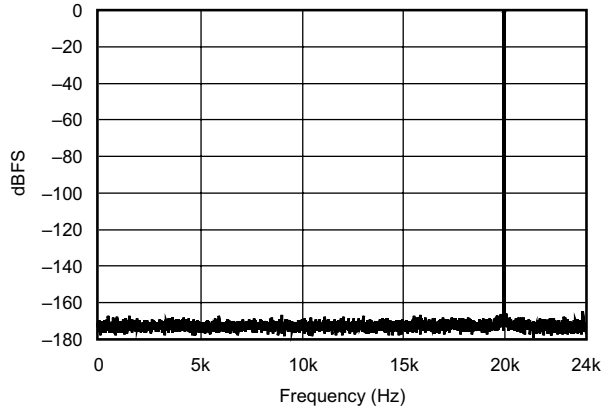


192 kHz:96 kHz

Figure 32. FFT With 1-kHz Input Tone at –60 dBFS

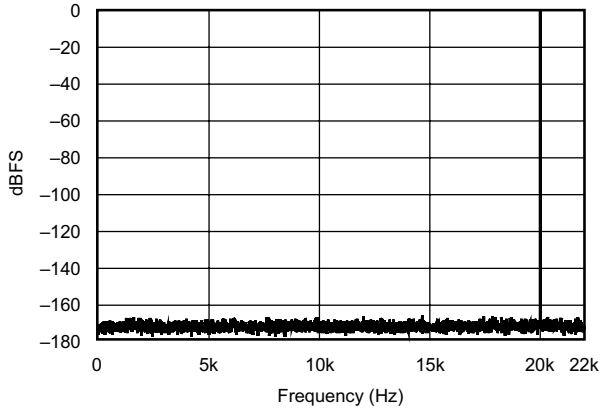
Typical Characteristics (continued)

At T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V, unless otherwise noted.



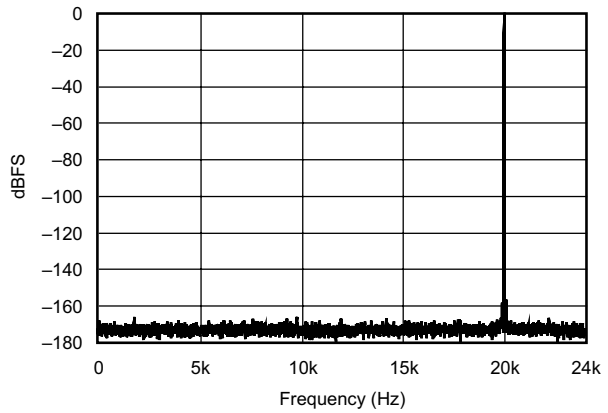
44.1 kHz:48 kHz

Figure 33. FFT With 20-kHz Input Tone at 0 dBFS



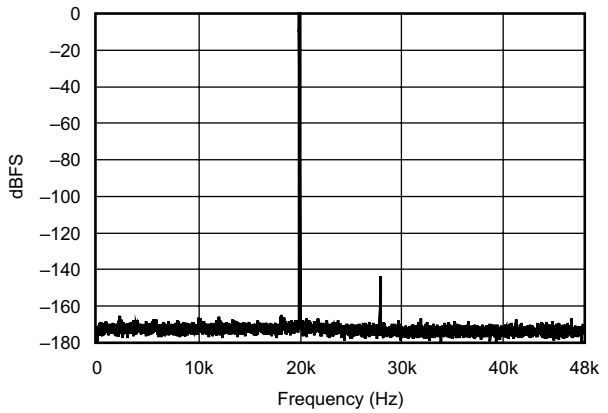
48 kHz:44.1 kHz

Figure 34. FFT With 20-kHz Input Tone at 0 dBFS



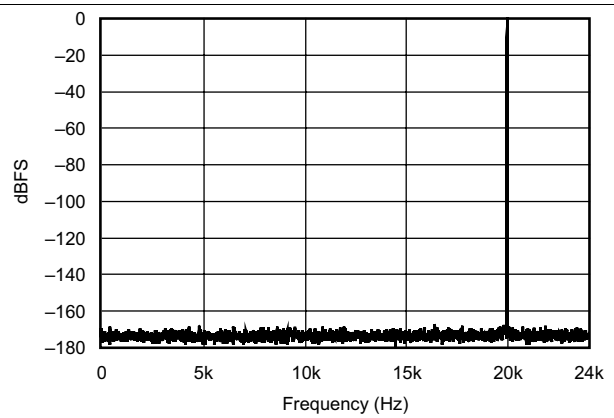
48 kHz:48 kHz

Figure 35. FFT With 20-kHz Input Tone at 0 dBFS



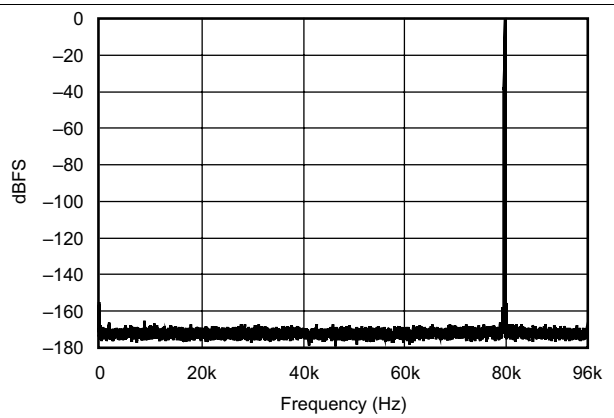
48 kHz:96 kHz

Figure 36. FFT With 20-kHz Input Tone at 0 dBFS



96 kHz:48 kHz

Figure 37. FFT With 20-kHz Input Tone at 0 dBFS

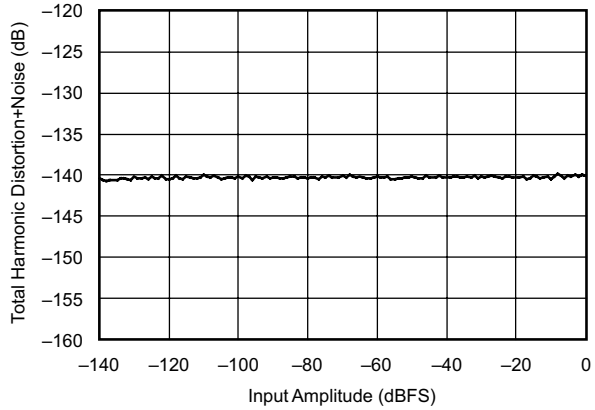


192 kHz:192 kHz

Figure 38. FFT With 80-kHz Input Tone at 0 dBFS

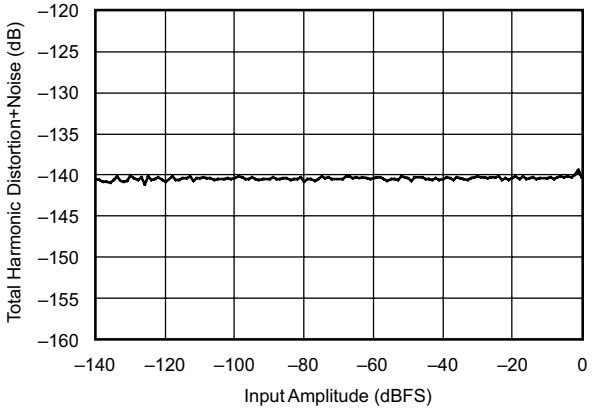
Typical Characteristics (continued)

At T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V, unless otherwise noted.



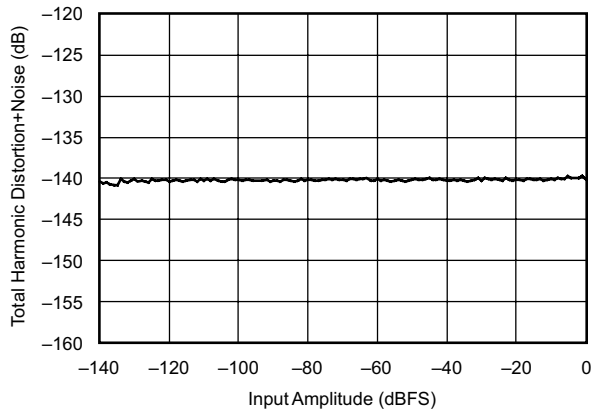
44.1 kHz:48 kHz

Figure 39. THD+N vs Input Amplitude f_{IN} = 1 kHz



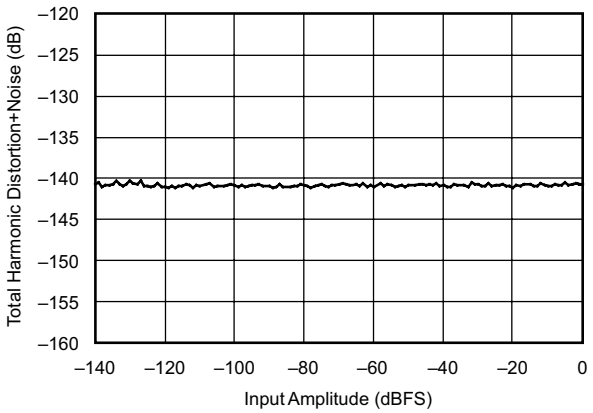
48 kHz:44.1 kHz

Figure 40. THD+N vs Input Amplitude f_{IN} = 1 kHz



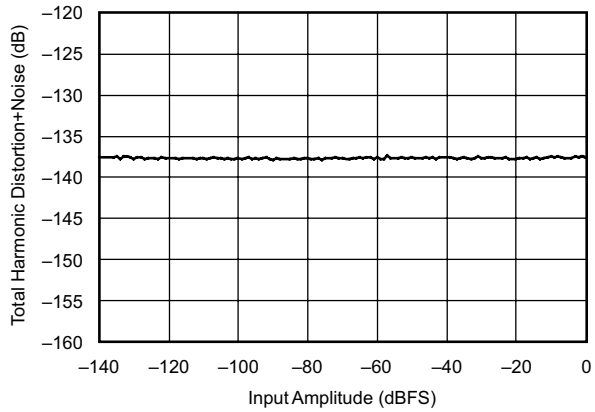
48 kHz:96 kHz

Figure 41. THD+N vs Input Amplitude f_{IN} = 1 kHz



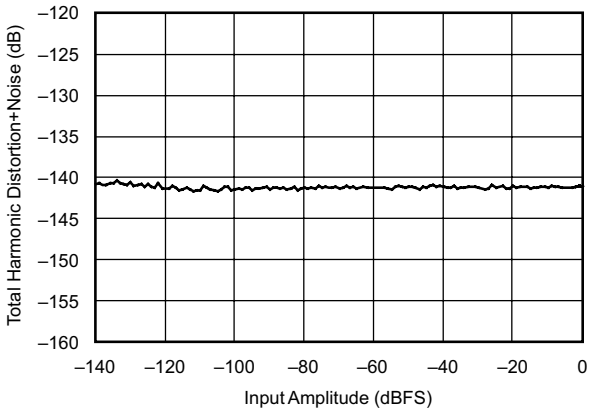
96 kHz:48 kHz

Figure 42. THD+N vs Input Amplitude f_{IN} = 1 kHz



44.1 kHz:192 kHz

Figure 43. THD+N vs Input Amplitude f_{IN} = 1 kHz

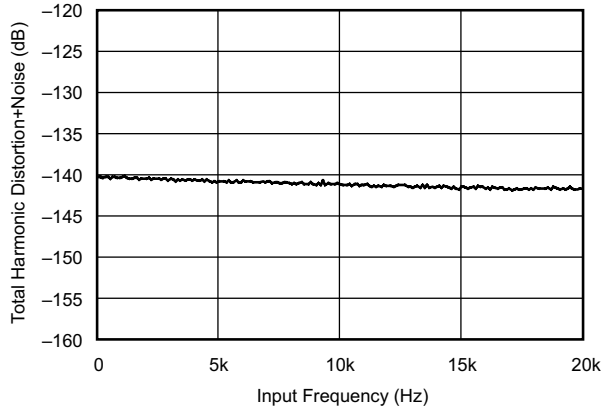


192 kHz:48 kHz

Figure 44. THD+N vs Input Amplitude f_{IN} = 1 kHz

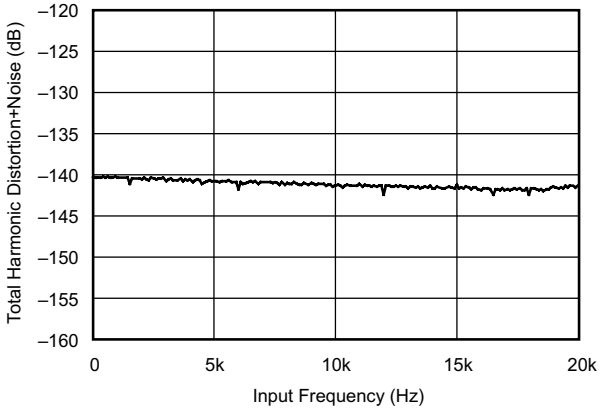
Typical Characteristics (continued)

At T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V, unless otherwise noted.



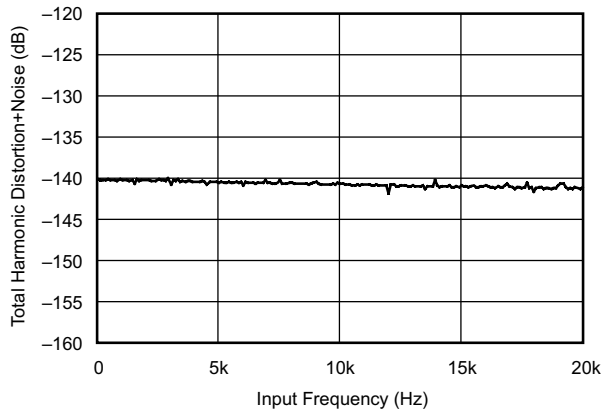
44.1 kHz:48 kHz

Figure 45. THD+N vs Input Frequency, 0-dBFS Input



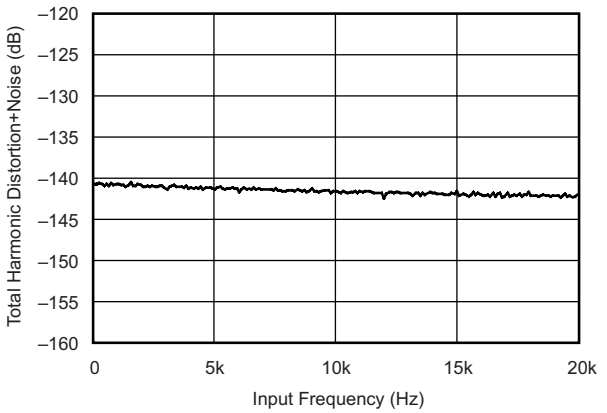
48 kHz:44.1 kHz

Figure 46. THD+N vs Input Frequency, 0-dBFS Input



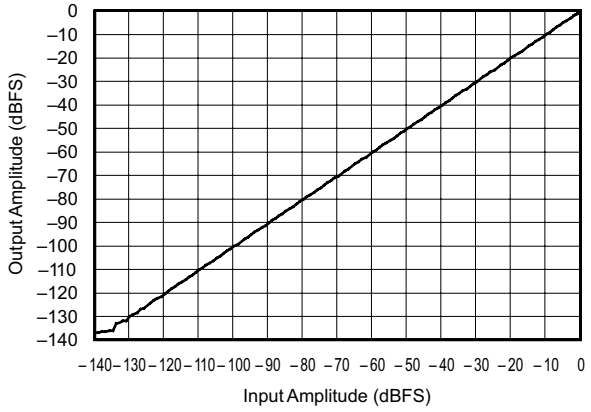
48 kHz:96 kHz

Figure 47. THD+N vs Input Frequency, 0-dBFS Input



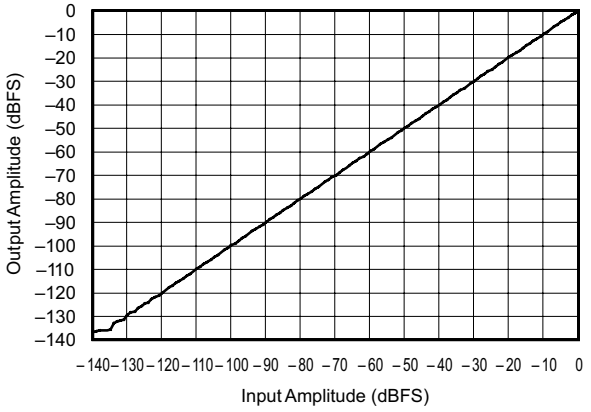
96 kHz:48 kHz

Figure 48. THD+N vs Input Frequency, 0-dBFS Input



44.1 kHz:48 kHz

Figure 49. Linearity With f_{IN} = 200 Hz

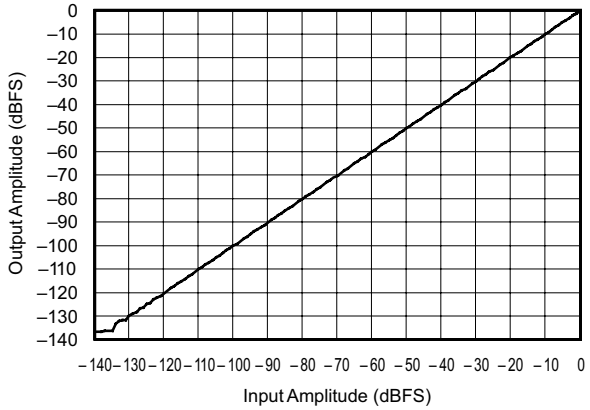


48 kHz:44.1 kHz

Figure 50. Linearity With f_{IN} = 200 Hz

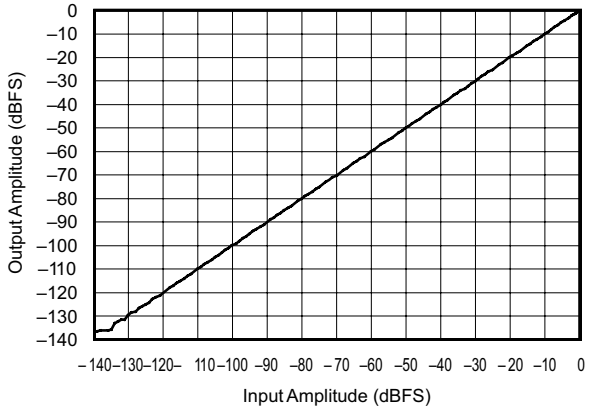
Typical Characteristics (continued)

At T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V, unless otherwise noted.



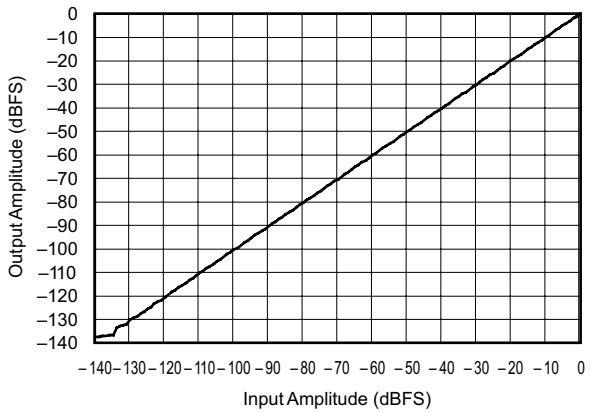
48 kHz:48 kHz

Figure 51. Linearity With f_{IN} = 200 Hz



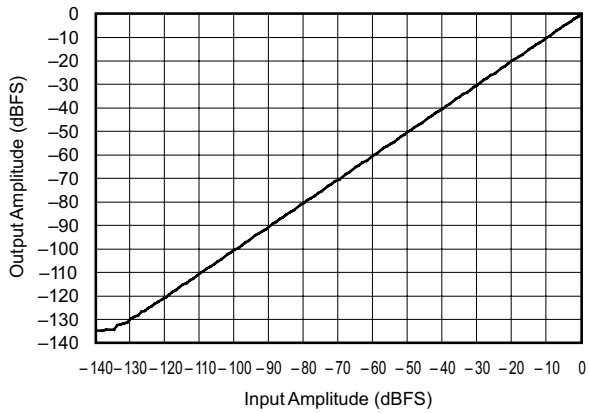
48 kHz:96 kHz

Figure 52. Linearity With f_{IN} = 200 Hz



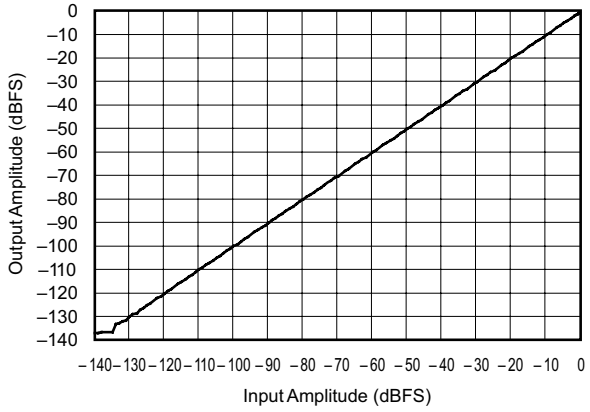
96 kHz:48 kHz

Figure 53. Linearity With f_{IN} = 200 Hz



44.1 kHz:192 kHz

Figure 54. Linearity With f_{IN} = 200 Hz



192 kHz:44.1 kHz

Figure 55. Linearity With f_{IN} = 200 Hz

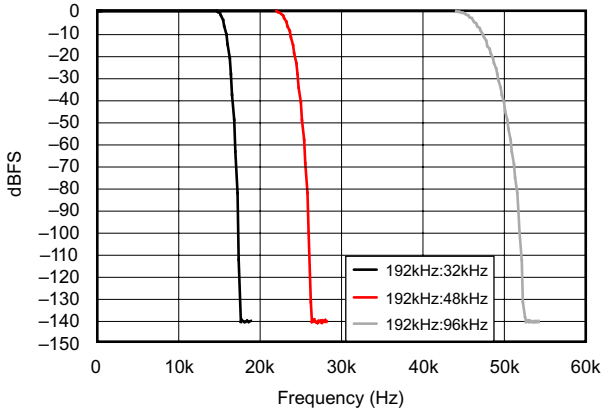


Figure 56. Frequency Response With 0-dBFS Input

Typical Characteristics (continued)

At T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V, unless otherwise noted.

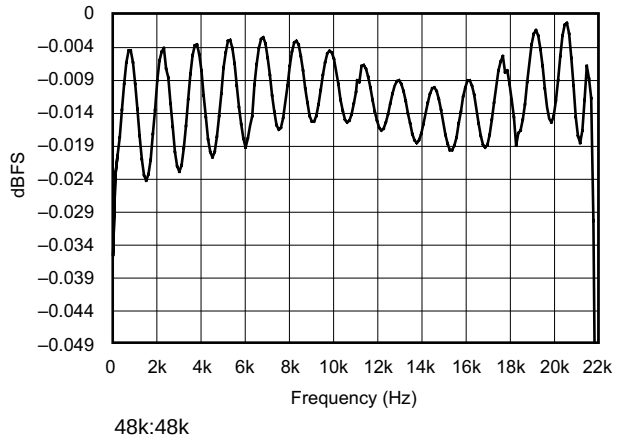


Figure 57. Pass Band Ripple

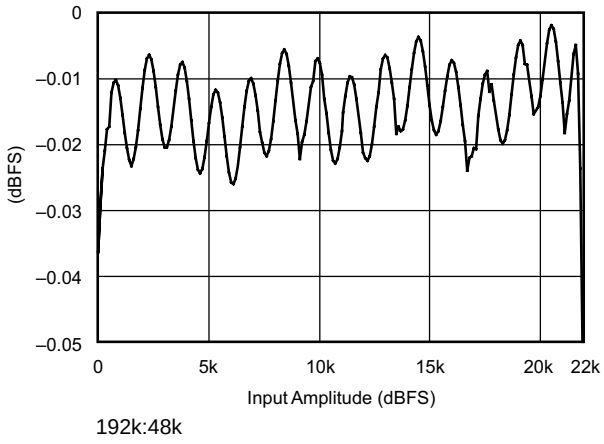


Figure 58. Pass Band Ripple

9 Parameter Measurement Information

Dynamic performance can be measured with an Audio Precision System Two Cascade or Cascade Plus (or any newer Audio Precision product, along with the SRC4192EVM). (http://www.ti.com/tool/src4192evm). Schematics available from the *SRC4190/92/93EVM - User Guide* (SBAU088).

10 Detailed Description

10.1 Overview

The SRC4192-Q1 device is an asynchronous, sample-rate converter (ASRC) designed for professional audio applications. Operation at input and output sampling frequencies up to 212 kHz is supported, with an input and output sampling ratio range of 16:1 to 1:16. Excellent dynamic range and Total Harmonic Distortion + Noise (THD+N) are achieved by employing high-performance, linear-phase digital filtering with image rejection better than 140 dB. Digital filtering options allow for lower group-delay processing. The digital filtering options include a low group-delay option for the interpolation and resampler function.

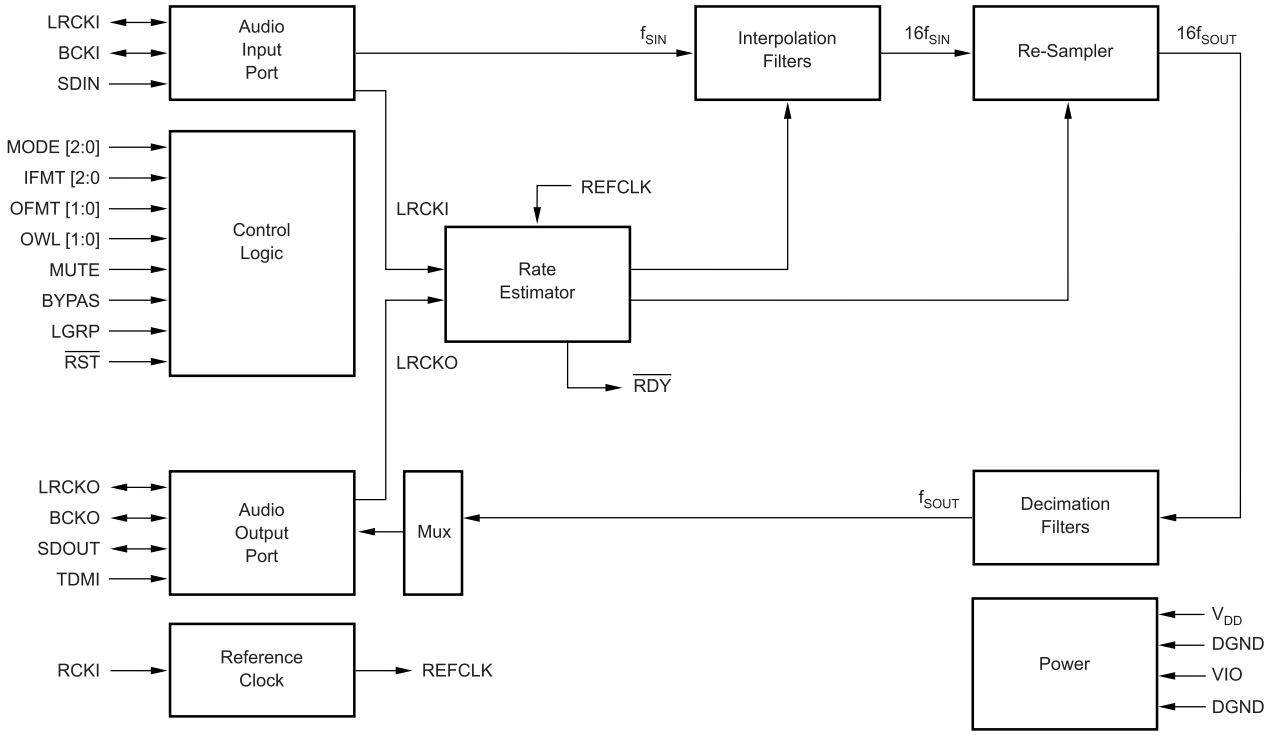
The audio input and output ports support standard audio data formats, as well as a TDM interface mode. Word lengths of 24 bits, 20 bits, 18 bits, and 16 bits are supported. Both ports can operate in slave mode, deriving their word and bit clocks from external input and output devices. Alternatively, one port can operate in master mode while the other remains in slave mode. In master mode, the LRCK and BCK clocks are derived from the reference clock input, RCKI. The flexible configuration of the input and output ports allows connection to a wide variety of audio data converters, interface devices, digital signal processors, and programmable logic.

A bypass mode is included, which allows audio data to be passed directly from the input port to the output port, bypassing the ASRC function. The bypass option is useful for passing through encoded or compressed audio data, or nonaudio control or status data.

A soft mute function is available on the SRC4192-Q1 device. The soft mute function provides artifact-free operation, while allowing muting or level adjustment of the audio output signal. The mute attenuation is typically –144 dB, while the digital attenuation control is adjustable from 0 dB to –127.5 dB in 0.5-dB steps.

The *Functional Block Diagram* shows a functional block diagram of the SRC4192-Q1 device. Audio data is received at the input port, clocked by either the audio data source in slave mode, or by the SRC4192-Q1 in master mode. The output-port data is also clocked by either the audio data source in slave mode, or by the SRC4192-Q1 in master mode. The input data is passed through interpolation filters which up-sample the data, which is then passed on to the resampler. The rate estimator compares the input and output sampling frequencies by comparing LRCKI, LRCKO, and a reference clock. The results include an offset for the FIFO pointer and the coefficients required for re-sampling function.

10.2 Functional Block Diagram



10.3 Feature Description

10.3.1 Input Port Operation

The audio input port is a three-wire synchronous serial interface that can operate in either slave or master mode. The SDIN input (pin 4) is the serial audio data input. Audio data is input at the SDIN pin in one of three standard audio data formats: Philips I^2S, Left-Justified, or Right-Justified. The audio data word length can be up to 24-bits for I^2S and Left-Justified formats, while the Right-Justified format supports 16-bit, 18-bit, 20-bit, or 24-bit data. The data formats are shown in Figure 59, while critical timing parameters are shown in Figure 60 and listed in the *Electrical Characteristics* section.

Feature Description (continued)

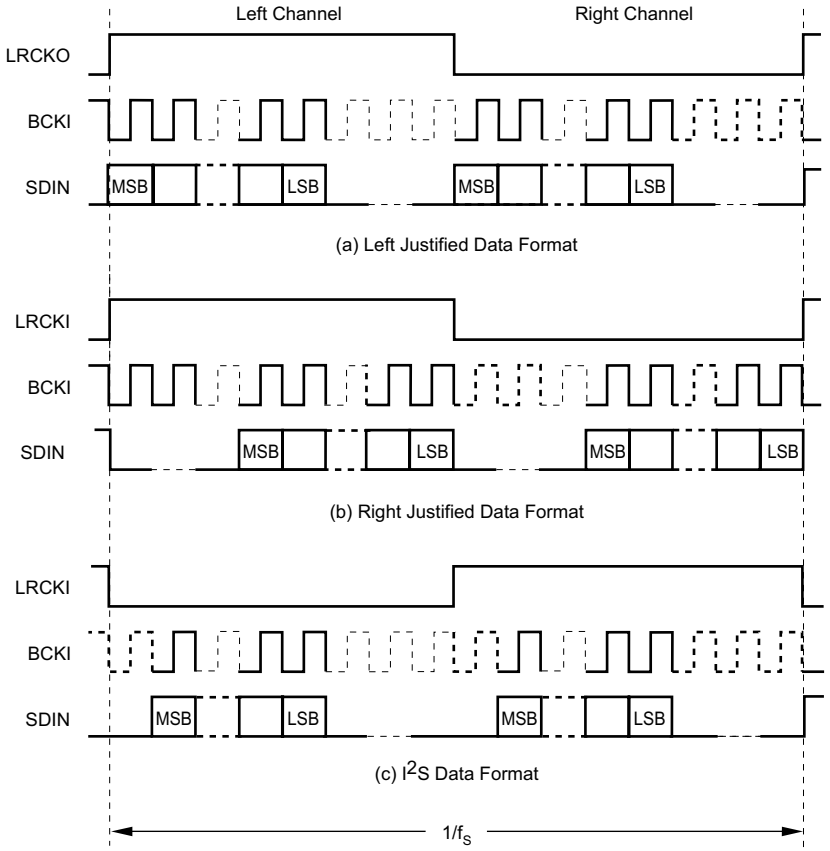


Figure 59. Input Data Formats

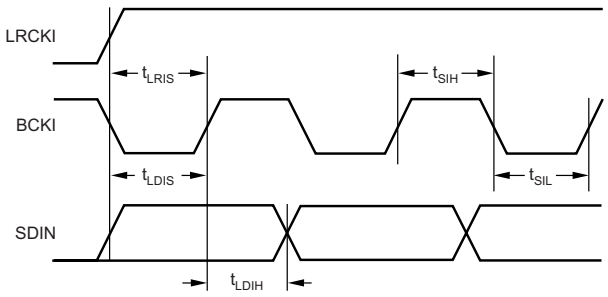


Figure 60. Input Port Timing

The bit clock is either an input or an output at BCKI (pin 5). In slave mode, BCKI is configured as an input pin, and can operate at rates from 32 f_S to 128 f_S,with a minimum of one clock cycle per data bit. In master mode, BCKI operates at a fixed rate of 64 f_S.

The left/right word clock, LRCKI (pin 6), can be configured as an input or output pin. In slave mode, LRCKI is an input pin, while in master mode LRCKI is an output pin. In either case, the clock rate is equal to f_S, the input sampling frequency. The LRCKI duty cycle is fixed to 50% for master mode operation.

Table 1 shows data format selection for the input port. For the SRC4192, the IFMT0 (pin 10), IFMT1 (pin 11), and IFMT2 (pin 12) inputs are used to set the input port data format.

Feature Description (continued)

Table 1. Input Port Data Format Selection

IFMT2	IFMT1	IFMT0	INPUT PORT DATA FORMAT
0	0	0	24-Bit Left Justified
0	0	1	24-Bit I^2S
0	1	0	Unused
0	1	1	Unused
1	0	0	16-Bit Right Justified
1	0	1	18-Bit Right Justified
1	1	0	20-Bit Right Justified
1	1	1	24-Bit Right Justified

10.3.2 Output Port Operation

The audio output port is a four-wire synchronous serial interface that can operate in either Slave or Master mode. The SDOUT output (pin 23) is the serial audio data output. Audio data is output at the SDOUT pin, which can be in one of four data formats: Philips I^2S, Left-Justified, Right-Justified, or TDM. The audio data word length can be 16 bits, 18 bits, 20 bits, or 24 bits. For all word lengths, the data is triangular PDF dithered from the internal 28-bit data path. The data formats (with the exception of TDM mode) are shown in Figure 61, while critical timing parameters are shown in Figure 62 and listed in the *Electrical Characteristics* section. The TDM format and timing are shown in Figure 66 and Figure 67, respectively, while examples of standard TDM configurations are shown in Figure 68 and Figure 69.

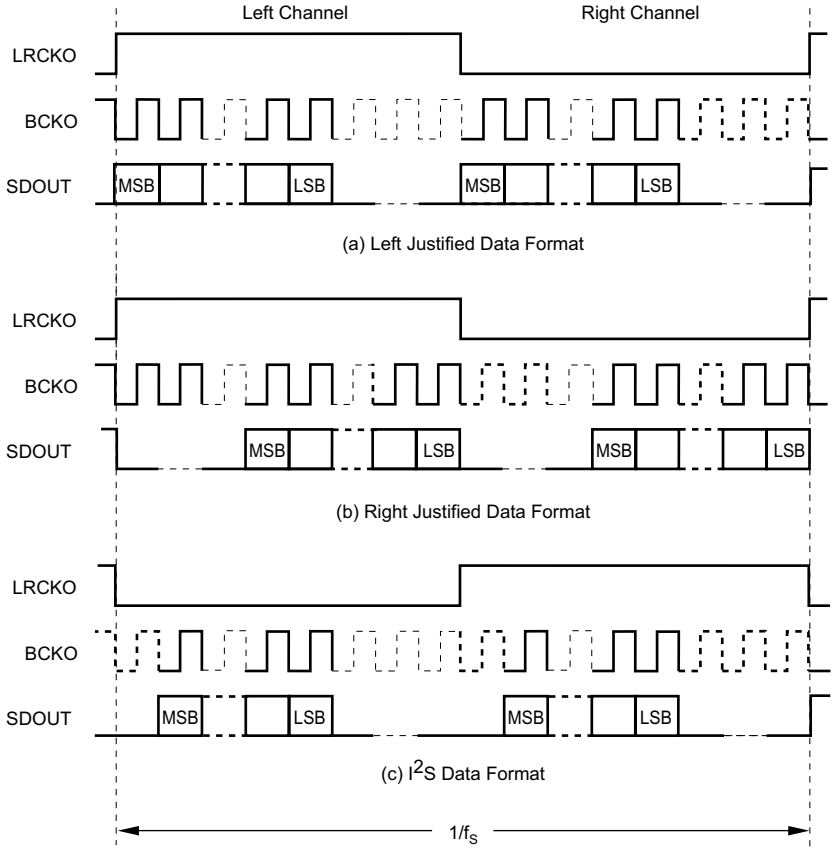


Figure 61. Output Data Formats

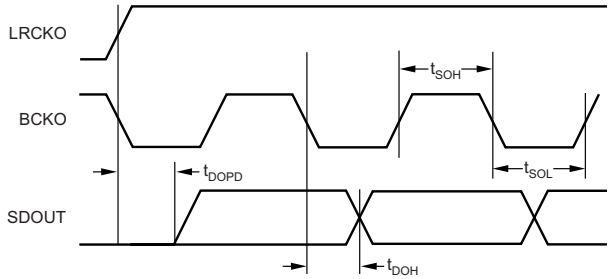


Figure 62. Output Port Timing

The bit clock is either input or output at BCKO (pin 25). In Slave mode, BCKO is configured as an input pin, and can operate at rates from 32 f_S to 128f_S, with a minimum of one clock cycle for each data bit. The exception is the TDM mode, where the BCKO must operate at N × 64 f_S, where N is equal to the number of SRC4192 devices included on the TDM interface. In master mode, BCKO operates at a fixed rate of 64 f_S for all data formats except TDM, where BCKO operates at the reference clock (RCKI) frequency. Additional information regarding TDM mode operation is included in the *Application and Implementation* section.

The left/right word clock, LRCKO (pin 24), can be configured as an input or output pin. In slave mode, LRCKO is an input pin, while in master mode it is an output pin. In either case, the clock rate is equal to f_S, the output sampling frequency. The clock duty cycle is fixed to 50% for I^2S, Left-Justified, and Right-Justified formats in master mode. The LRCKO pulse width is fixed to 32 BCKO cycles for the TDM format in master mode.

Table 2 illustrates data format selection for the output port. For the SRC4192-Q1, the OFMT0 (pin 19), OFMT1 (pin 18), OWL0 (pin 17), and OWL1 (pin 16) inputs are used to set the output port data format and word length.

Table 2. Output Port Data Format Selection

OFMT1	OFMT0	OUTPUT PORT DATA FORMAT
0	0	Left-Justified
0	1	I^2S
1	0	TDM
1	1	Right-Justified
OWL1	**OWL0**	**OUTPUT PORT DATA WORD LENGTH**
0	0	24 bits
0	1	20 bits
1	0	18 bits
1	1	16 bits

10.3.3 Soft Mute Function

The soft mute function of the SRC4192-Q1 device is invoked by forcing the MUTE input (pin 14) high. The soft mute function slowly attenuates the output signal level down to all zeroes ±1LSB of dither, which provides an artifact-free muting of the audio output port.

10.3.4 Ready Output

The SRC4192-Q1 device includes an active low ready output called $\overline{RDY}$ (pin 15). The $\overline{RDY}$ pin is an output from the rate estimator block, which indicates that the input-to-output sampling frequency ratio has been determined. The ready signal can be used as a flag or indicator output. The ready signal can also be connected to the active high MUTE input (pin 14) to provide an auto-mute function, so that the output port is muted when the rate estimator is in transition.

10.4 Device Functional Modes

10.4.1 Reset and Power Down Operation

The SRC4192-Q1 device can be reset using the $\overline{RST}$ input (pin 13). The device does not have an internal power-on reset, therefore the user should force a reset sequence after power up to initialize the device. To force a reset, the reference clock input must be active, with an external clock source supplying a valid reference clock signal (refer to Figure 73). The user must assert $\overline{RST}$ low for a minimum of 500 ns, and then bring $\overline{RST}$ high again to force a reset. Figure 63 shows the reset timing for the SRC4192-Q1 device.

The SRC4192-Q1 device also supports a power-down mode. Power-down mode can be set by either holding the $\overline{RST}$ input low

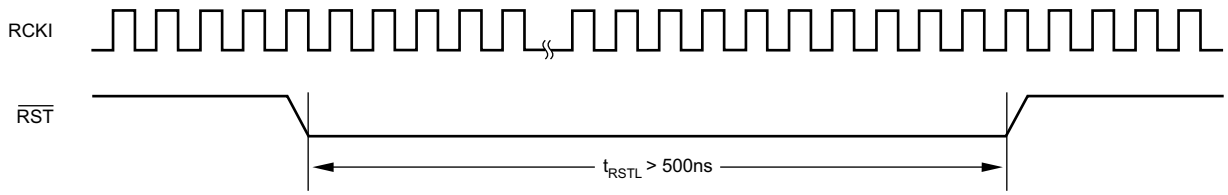


Figure 63. Reset Pulse Width Requirement

10.4.2 Audio Port Modes

The SRC4192-Q1devices supports seven serial-port modes, shown in Table 3. The audio port mode is selected using the MODE0 (pin 26), MODE1 (pin 27), and MODE2 (pin 28) inputs.

In slave mode, the port LRCK and BCK clocks are configured as inputs, and receive their clocks from an external audio device. In master mode, the LRCK and BCK clocks are configured as outputs, being derived from the reference clock input (RCKI). Only one port can be set to master mode at any given time, as indicated in Table 3.

Table 3. Setting the Serial Port Modes

MODE2	MODE1	MODE0	SERIAL PORT MODE
0	0	0	Both Input and Output Ports are Slave mode
0	0	1	Output Port is Master mode with RCKI = 128 f_S
0	1	0	Output Port is Master mode with RCKI = 512 f_S
0	1	1	Output Port is Master mode with RCKI = 256 f_S
1	0	0	Both Input and Output Ports are Slave mode
1	0	1	Input Port is Master mode with RCKI = 128 f_S
1	1	0	Input Port is Master mode with RCKI = 512 f_S
1	1	1	Input Port is Master mode with RCKI = 256 f_S

10.4.3 Bypass Mode

The SRC4192-Q1 device includes a bypass function, which routes the input port data directly to the output port bypassing the ASRC function. Bypass mode can be invoked by forcing the BYPAS input (pin 9) high for the devices. The BYPAS pin and control bit should be set to 0 for normal operation.

No dithering is applied to the output data in bypass mode, and the digital attenuation and mute functions are also unavailable.

11 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

This section of the data sheet provides practical applications information for hardware and systems engineers designing the SRC4192-Q1 device into the end equipment.

11.1.1 Interfacing to Digital Audio Receivers and Transmitters

The input and output ports of the SRC4192-Q1 device are designed to interface to a variety of audio devices, including receivers and transmitters commonly used for AES/EBU, S/PDIF, and CP1201 communications.

Texas Instruments manufactures the DIR9001 digital audio interface receiver and DIT4096/4192 digital audio transmitters to address these applications.

Figure 64 shows interfacing the DIR9001 device to the input port of the SRC4192 device. The DIR9001 device operates from a single 3.3-V supply, which requires the V_{IO} supply (pin 7) for the SRC4192 device to be set to 3.3 V for interface compatibility.

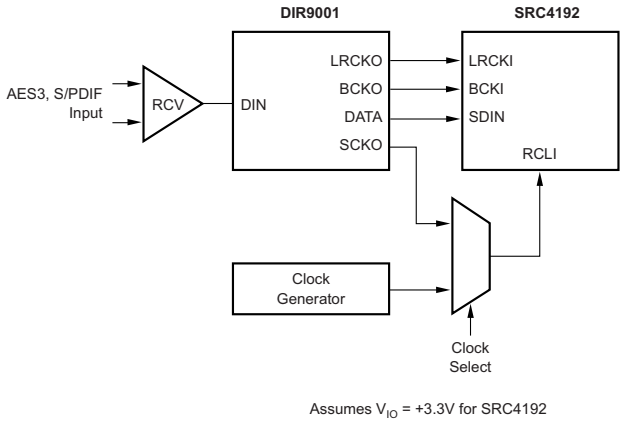
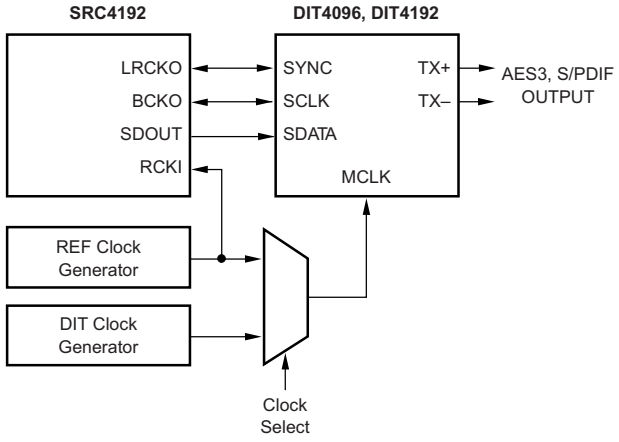


Figure 64. Interfacing the SRC4192-Q1 to the DIR9001 Digital Audio Interface Receiver

Figure 65 shows the interface between the output port of the SRC4192-Q1 device and the audio serial port of the DIT4096 or DIT4192 device. Again, the V_{IO} supplies for both the SRC4192-Q1 device and DIT4096/4192 device are set to 3.3 V for compatibility.

Application Information (continued)



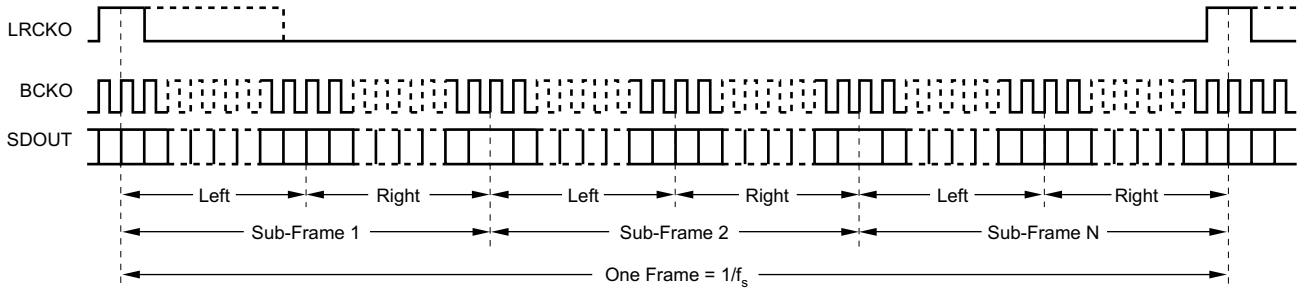
Assumes V_{IO} = +3.3V for SRC4192 and DIT4096, DIT4192

Figure 65. Interfacing the SRC4192-Q1 to the DIT4096/4192 Digital Audio Interface Transmitter

Like the output port of the SRC4192-Q1 device, the audio serial port of the DIT4096 and DIT4192 device can be configured as a master or slave. In cases where the output port of the SRC4192-Q1 device is set to master mode, use the reference clock source (RCKI) as the master clock source (MCLK) for the DIT4096/4192 device, to ensure that the transmitter is synchronized to the output port data of the SRC4192-Q1 device.

11.1.2 TDM Applications

The SRC4192-Q1 device supports a TDM output mode, which allows multiple devices to be daisy-chained together to create a serial frame. Each device occupies one subframe within a frame, and each sub-frame carries two channels (Left followed by Right). Each sub-frame is 64 bits long, with 32 bits allotted for each channel. The audio data for each channel is left justified within the allotted 32 bits. Figure 66 shows the TDM frame format, while Figure 67 shows TDM input timing parameters, which are listed in the *Electrical Characteristics* section.



N = Number of Daisy-Chained Devices
One Sub-Frame contains 64 bits, with 32 bits per channel.
For each channel, the audio data is left justified, MSB first format, with the word length determined by the OWL[1:0] pins/bits.

Figure 66. TDM Frame Format

Application Information (continued)

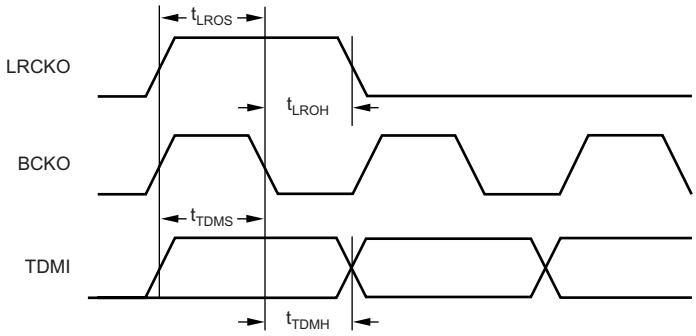


Figure 67. Input Timing for TDM Mode

The frame rate is equal to the output sampling frequency, f_s. The BCKO frequency for the TDM interface is N × 64 f_s, where *N* is the number of devices included in the daisy chain. For Master mode, the output BCKO frequency is fixed to the reference clock (RCKI) input frequency. The number of devices that can be daisy-chained in TDM mode is dependent upon the output sampling frequency and the BCKO frequency, leading to the following numerical relationship:

Number of Daisy-Chained Devices = (f_{BCKO} / f_s) / 64 (1)

where

- f_{BCKO} = Output Port Bit Clock (BCKO), 27.648-MHz maximum
- f_s = Output Port Sampling (or LRCKO) Frequency, 216-kHz maximum.

This relationship holds true for both slave and master modes.

Figure 68 and Figure 69 show typical connection schemes for TDM mode. Although the TMS320C671x DSP device family is shown as the audio processing engine in the figures, other TI digital signal processors with a multi-channel buffered serial port (McBSPTM) can also function with this arrangement. Interfacing to processors from other manufacturers is also possible. Refer to Figure 62 in this data sheet, along with the equivalent serial port timing diagrams shown in the DSP data sheet, to determine compatibility.

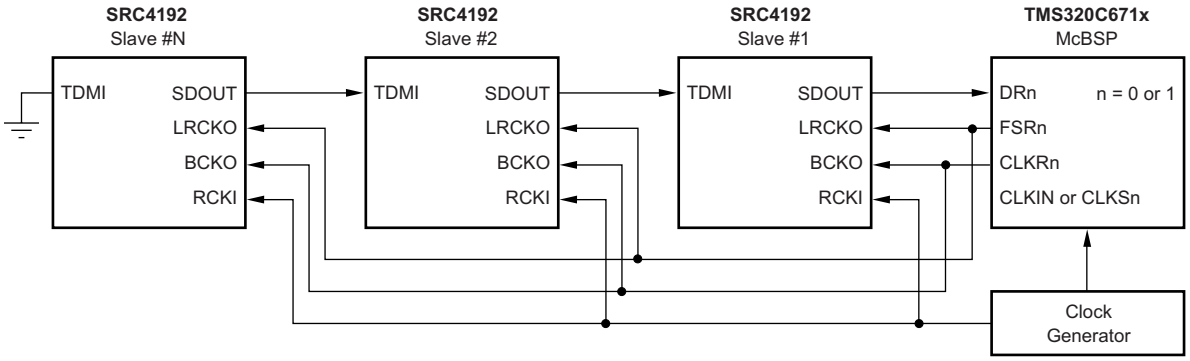


Figure 68. TDM Interface where all Devices are Slaves

Application Information (continued)

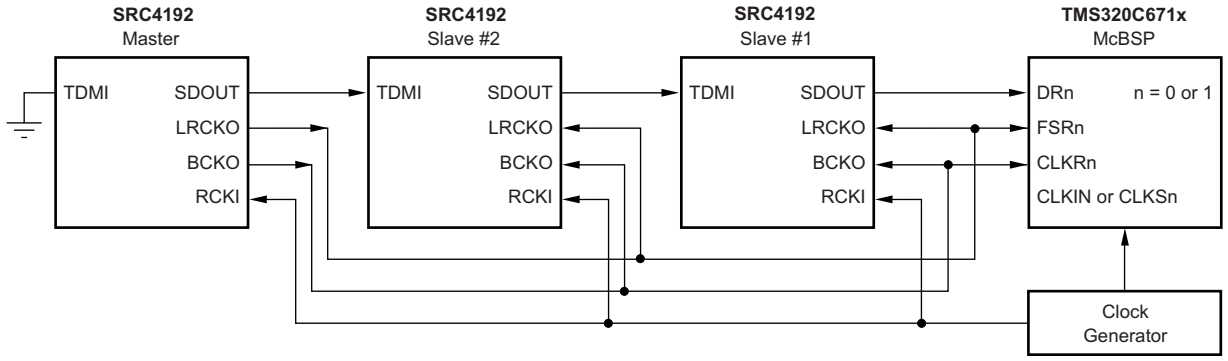


Figure 69. TDM Interface where one Device is Master to Multiple Slaves

11.2 Typical Application

Figure 70 shows the typical connection diagram for the SRC4192-Q1. Recommended values for power supply bypass capacitors are included. The capacitors should be placed as close to the IC package as possible.

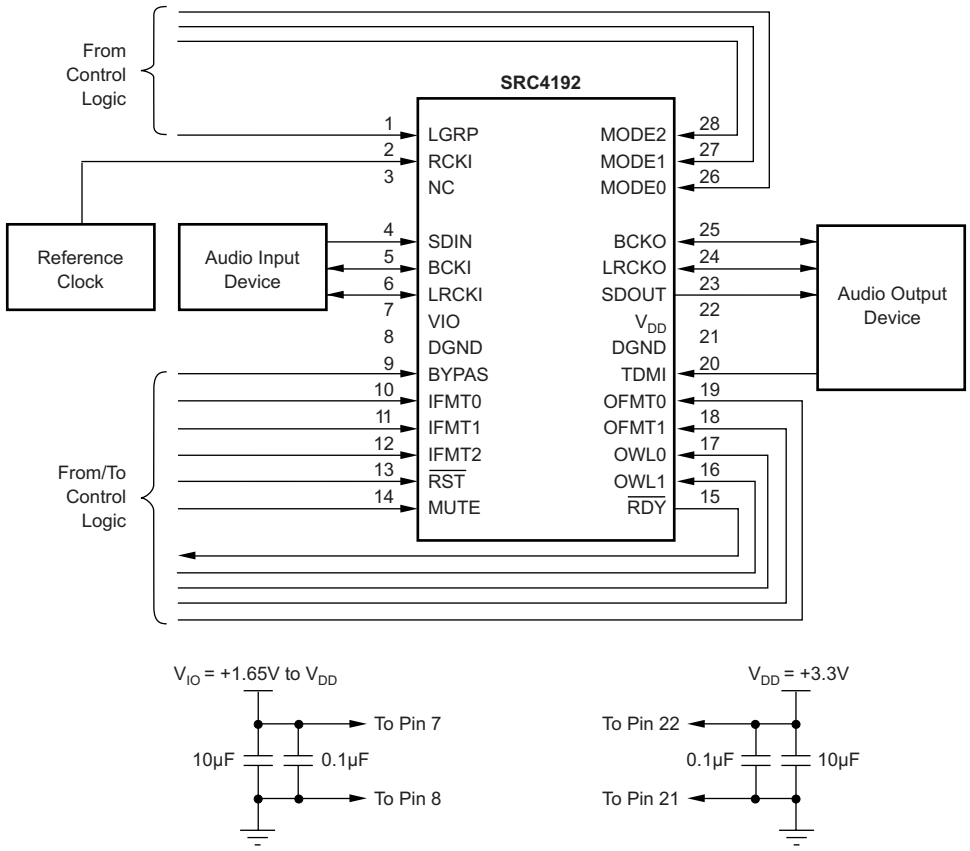


Figure 70. Typical Connection Diagram for the SRC4192-Q1

Typical Application (continued)

11.2.1 Design Requirements

The following lists design requirements:

- Control: Hardware, I^2C, or SPI
- Audio input: PCM serial data
- Audio output: PCM serial data
- Reference clock

11.2.2 Detailed Design Procedure

11.2.2.1 Control Method

The SRC4192-Q1 is a hardware controlled device. The SRC4192-Q1 control pins can be connected to V_{DD} or GND directly or by the GPIO of a host controller.

11.2.2.2 Audio Input and Output

The Audio input and output ports can handle 16-bit, 18-bit, 20-bit, or 24-bit right justified PCM serial data as well as 24-bit I2S or left justified PCM serial data at up to a 212-kHz sampling rate. A TDM format is also available. Both input and output can operate in slave mode, or one can operate as master while the other operates as a slave. A 16:1 or 1:16 is the max ratio supported between the input and output audio sampling rates.

11.2.3 Application Curves

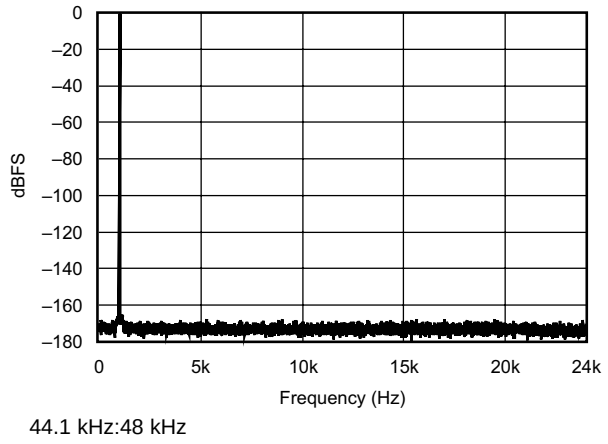


Figure 71. FFT With 1-kHz Input Tone at 0 dBFS

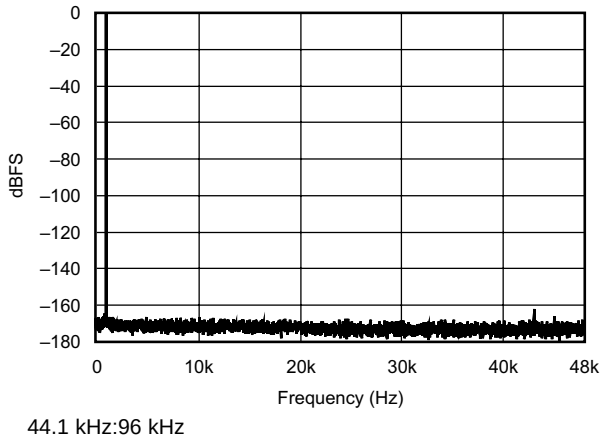


Figure 72. FFT With 1-kHz Input Tone at 0 dBFS

12 Power Supply Recommendations

To ensure compatibility, the VDD_IO and VDD_CORE supplies of the AD1896 device must be set to 3.3 V, while the V_{IO} and V_{DD} supplies of the SRC4192-Q1 device must be set to 3.3 V.

13 Layout

13.1 Layout Guidelines

13.1.1 Reference Clock

The SRC4192-Q1 device requires a reference clock for operation. The reference clock is applied at the RCKI input (pin 2). Figure 73 shows the reference clock connections and requirements for the SRC4192-Q1. The reference clock can operate at 128 f_S, 256 f_S, or 512 f_S, where f_S are the input or output sampling frequency. The maximum external reference clock input frequency is 50 MHz.

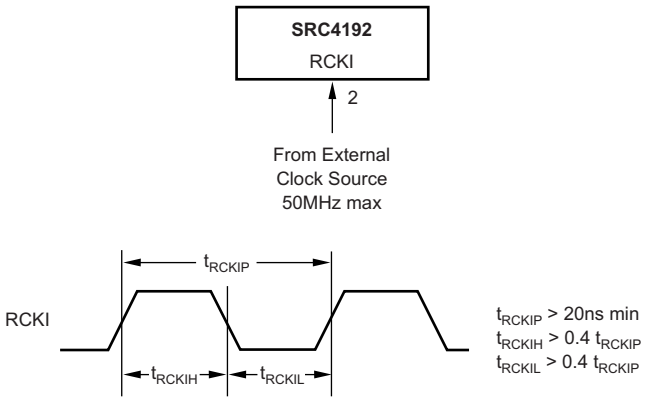


Figure 73. Reference Clock Input Connections and Timing Requirements

13.1.2 Pin Compatibility With the Analog Devices AD1896

The SRC4192-Q1 device is pin-and function-compatible with the AD1896 device when observing the guidelines indicated in the following paragraphs.

13.1.2.1 Crystal Oscillator

The SRC4192-Q1 does not have an on-chip crystal oscillator. An external reference clock is required at the RCKI input (pin 2).

13.1.2.2 Reference Clock Frequency

The reference clock input frequency for the SRC4192-Q1 must be no higher than 30 MHz, to match the master clock frequency specification of the AD1896 device. In addition, the SRC4192-Q1 device does not support the 768 f_S reference clock rate.

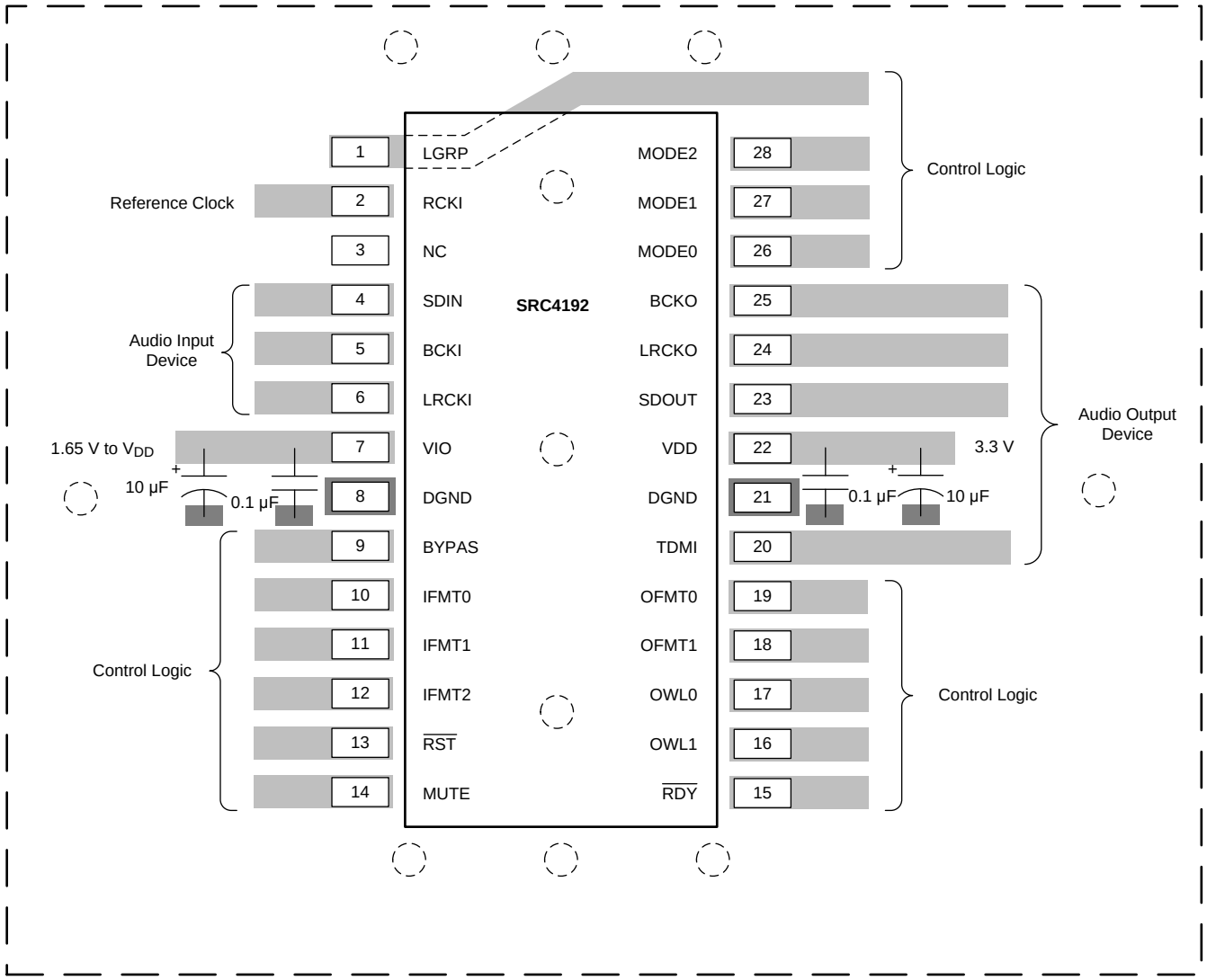
13.1.2.3 Master Mode Maximum Sampling Frequency

When the input or output ports are set to master mode, the maximum sampling frequency must be limited to 96 kHz to support the AD1896 device specification, despite the fact that the SRC4192-Q1 device supports a maximum sampling frequency of 212 kHz in master mode. The user should consider building an option into their design to support the higher sampling frequency of the SRC4192-Q1 device.

13.1.2.4 Matched Phase Mode

Because of the internal architecture of the SRC4192-Q1 device, it does not require or support the matched phase mode of the AD1896 device. Given multiple SRC4192-Q1 devices, if all reference clock (RCKI) inputs are driven from the same clock source, the devices will be phase-matched.

13.2 Layout Example



(1) TI recommends placing a top-layer ground pour for shielding around the SRC4192 device and connecting the ground pour to the lower main PCB-ground plane with multiple vias.

Figure 74. SRC4192-Q1 Layout Example

14 Device and Documentation Support

14.1 Documentation Support

14.1.1 Related Documentation

For related documentation, see the following: *SRC4192EVM Evaluation Module,* SBAU088

14.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

14.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

14.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

14.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SRC4192QDBRQ1	PREVIEW	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SRC4192Q	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SRC4192-Q1 :

- Catalog: SRC4192

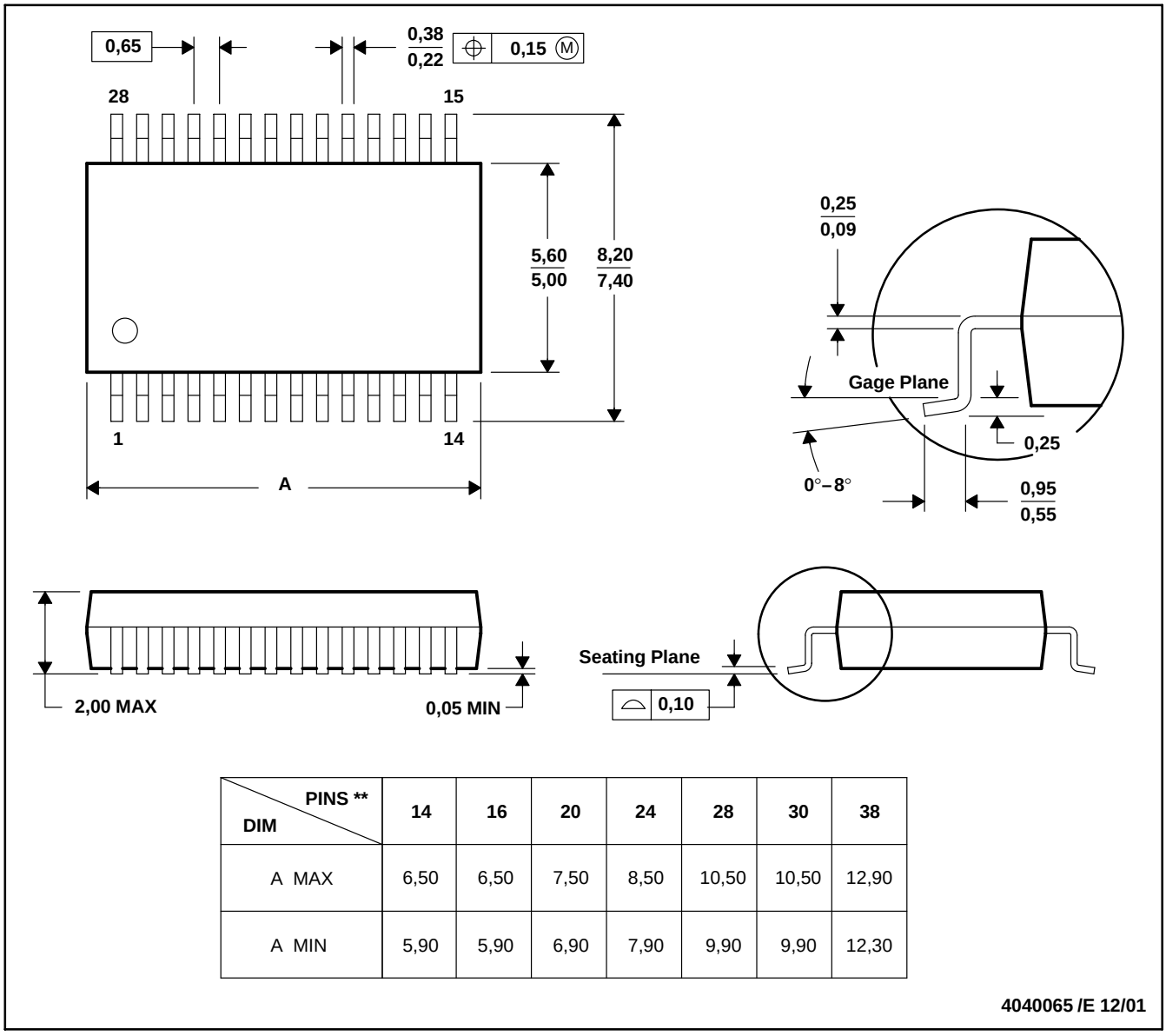
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265