PGA450Q1EVM User’s Guide

User's Guide

Literature Number: SLDU007C
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PGA450Q1EVM User's Guide

1 Read This First

The PGA450-Q1 is an interface device for ultrasonic transducers used in automotive parking assistance and blind spot detection applications. The device functions as the driver and receiver for a wide range of transducers with frequency ranges from 40 kHz to 70 kHz. The PGA450-Q1 device incorporates an analog front end (AFE) and a 8051W microprocessor core. The AFE includes voltage regulators, an amplifier, an ADC, an oscillator, and a temperature sensor. The PGA450-Q1 device also implements a LIN 2.1 physical layer for communication. For more details, see the device data sheet.

2 About This Manual

This user's guide describes the characteristics, operation, and use of the PGA450Q1EVM. An EVM description, GUI description, interface requirements, and complete schematic are included.

3 EVM Overview

The features of this EVM are as follows:

- Single power-supply input for basic operation
- Example push-pull transformer and 58-kHz transducer
- LIN master transceiver
- RS-232 transceiver for UART testing and debug
- PC control with a graphical user interface and USB communications board

For a given PGA450Q1EVM installation, the following items apply:

- The PGA450Q1EVM can have either a through-hole or surface-mount transformer installed on it. When a through-hole transformer is installed, ensure that the case corners are not touching the surface mount pads.
- The PGA450Q1EVM can be used to drive either a single-ended or push-pull transformer. The selection of the drive method is achieved through jumper selection.
- The USB communication board 5-V power supply must be enabled for LIN communication to work. The 5-V power supply provides power to the LIN master transceiver installed on the board.
- In order to communicate with the PGA450-Q1 device using SPI, the 8051W inside the device must be put in the reset state.

4 Power-Supply Requirements and Connections

4.1 Power Supply

Only one main power supply is needed. Apply 7 VDC to 18 VDC to the PGA450Q1EVM that supplies power to the entire board, except for the USB communications board and LIN which are powered by the USB communication PCB. Connect a power supply to the banana jacks, P1 “VPWR_IN” and P3 “GND” or use the screw terminal P2.

4.2 Controlling and Powering the PGA450Q1EVM via the USB Interface Board

The PGA450Q1EVM is shipped with a USB interface board that provides a link from the PC-controlled GUI (described later) to the EVM. Connect the USB interface board to the PGA450-Q1 device by connecting the 30-pin female header on the interface board to P6, the male 30-pin header on the PGA450Q1EVM. The TI logo on the interface board should face up when it is plugged in. Figure 1 shows the interface board connected to the PGA450Q1EVM.

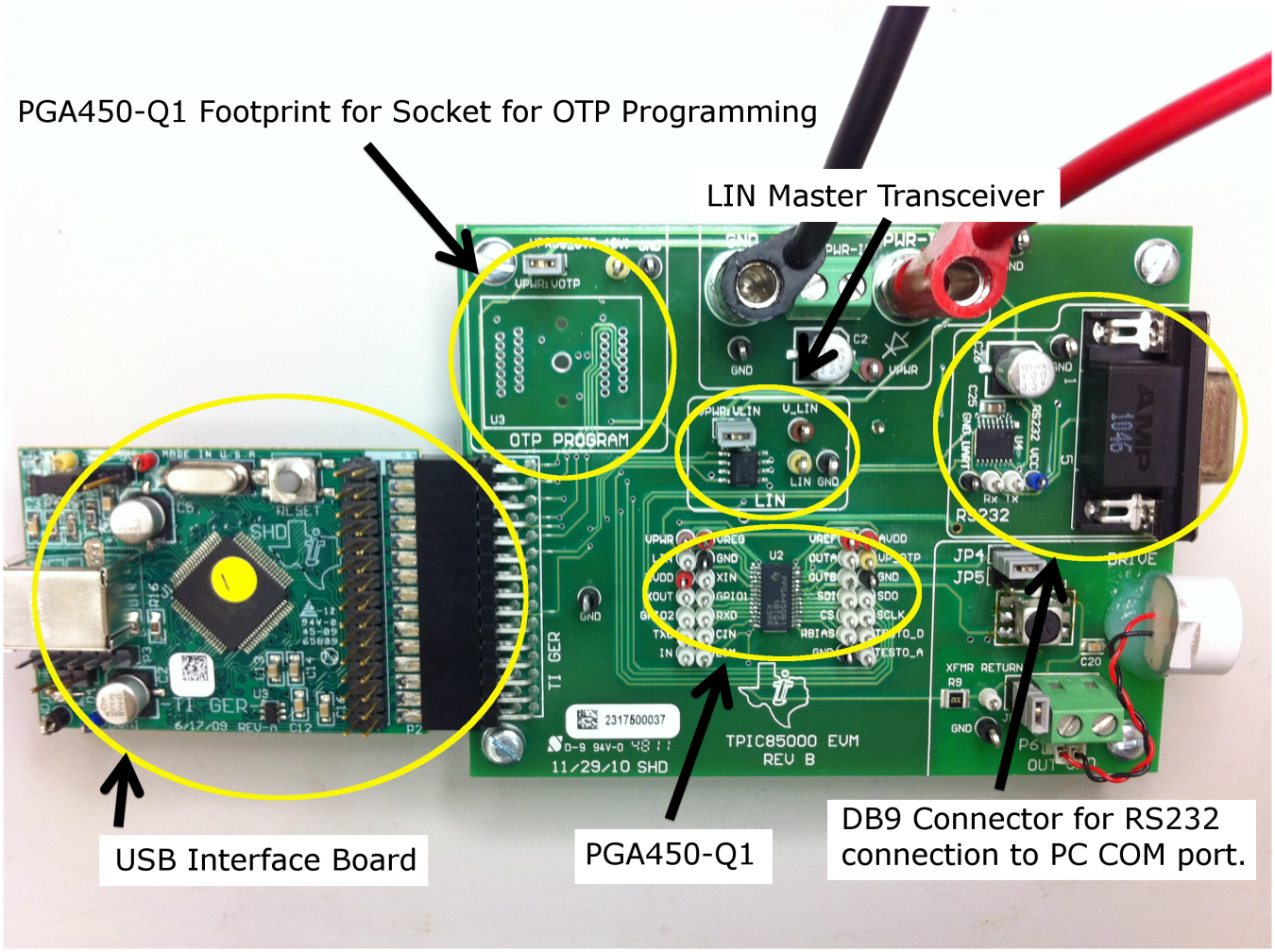


Figure 1. PGA450Q1EVM Setup

Connecting the Transducer

A transducer is included with the EVM. Solder the transducer connector to the through-holes at P6. Alternatively, use the screw terminal to connect the transducer.

5 Jumper Settings

There are several jumpers and 0-Ω resistors located on the board, which are used to configure the connections to the PGA450-Q1 device and the rest of the EVM. The default settings and their effects are listed below.

5.1 Jumpers

Table 1 shows the function of each specific jumper setting on the EVM.

Table 1. Jumpers

Reference	Jumper Setting	Function
VPWR:VOTP	Closed	VP_OTP power supply input on the PGA450-Q1 device is connected to the 8-V voltage supply on the EVM.
	Open	VP_OTP power supply input on the PGA450-Q1 device is not connected to the 8-V voltage supply on the EVM.
VPWR:VLIN	Closed	VPWR is connected to V_LIN, which is the LIN bus voltage.
	Open	VPWR is not connected to V_LIN, which is the LIN bus voltage.
JP3	Closed	The secondary of the transformer on the EVM is connected to the PGA450-Q1 device on the EVM.
	Open	The secondary of the transformer on the EVM is not connected to the PGA450-Q1 device on the EVM.
JP4	Closed	The transformer primary top terminal is connected to the OUTA pin on the PGA450-Q1 device, for push-pull configuration.(1)
	Open	The transformer primary top terminal is not connected to the OUTA pin on the PGA450-Q1 device.
JP5	Closed	The transformer primary top terminal is connected to the VREG pin on the PGA450-Q1 device, for single-ended configuration.
	Open	The transformer primary top terminal is not connected to the VREG pin on the PGA450-Q1 device.

(1) The transformer provided with the EVM is push-pull. When using the single-ended configuration, JP4 must be disconnected and JP5 must be closed

5.2 Default Jumper Settings

Table 2. Default Jumper Settings(1)

Reference	Jumper Position	Function
VPWR:VOTP	Open	VP_OTP power supply input on the PGA450-Q1 device is not connected to the 8-V voltage supply on the EVM.
VPWR:VLIN	Closed	VPWR is connected to V_LIN, which is the LIN bus voltage.
JP3	Closed	The secondary of the transformer on the EVM is connected to the PGA450-Q1 device on the EVM.
JP4	Closed	The transformer primary terminal 1 is connected to the OUTA pin on the PGA450-Q1 device for push-pull configuration.
JP5	Open	The transformer primary terminal 1 is not connected to the VREG pin on the PGA450-Q1 device.

(1) Ensure the TI-GER USB Interface board has no jumpers populated except for the 5-V digital I/O-level option located adjacent to the red 5-V test-point. The HEX jumper should not be installed, nor should any of the pins on pin block P3 be shorted; these are reserved for TI only.

5.3 0-Ω Resistors

The 0-Ω resistor R2 is used to connect the programming voltage to the PGA450-Q1 device that is soldered to the PCB. This resistor is not populated on the PCB. The soldered device has had the OTP programmed for DEVRAM usage.

Table 3. Default 0-Ω Resistor Setting

Reference	Install	Function
R2	DNP	The VP_OTP pin of the device does not have OTP programming voltage.

Although they are installed to default settings in the factory, it is recommended that the user verify that the jumpers and 0-Ω resistors are installed to their default settings before powering on the EVM.

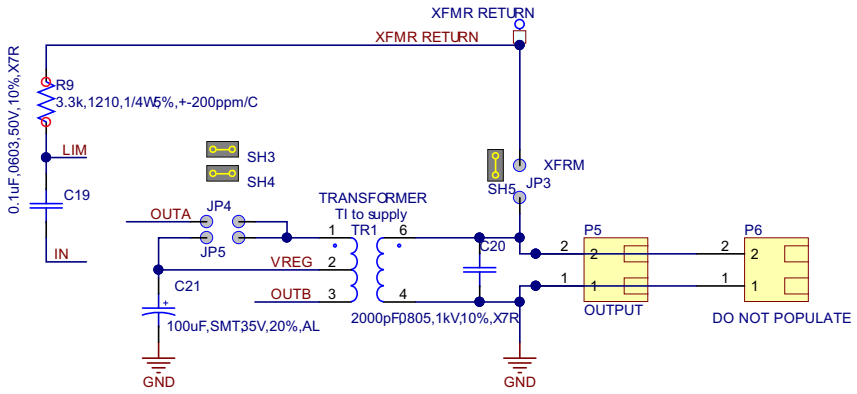
6 Socket for Programming OTP

The PGA450Q1EVM runs from the PGA450-Q1 device that is soldered to the board. In addition, the EVM provides a footprint for a socket to enable programming the OTP in devices that are for customer-board use. The socket is not populated by default on the EVM. The part number for the recommended socket is OTS-28-0.65-01.

The GUI then can be used to select the target PGA450-Q1 device when programming OTP (the two options are the soldered device, or the device in the socket). More details of how to do this are described in the OTP section.

7 Transformer and Transducer

A matched transformer-transducer pair is included on the PGA450Q1EVM.



NOTE: C20 is a temperature compensation capacitor for the XDCR. Match C20 to the selected XDCR. If XDCR is Murata MA58MF14-7N, 2000-pF capacitance is installed, and 1500-pF capacitance is provided as an alternative. If XDCR is Murata MA58AF14-0N. 1500-pF capacitance is installed. Alternative specifications include: 1500 pF, 0805, 250 V, 20%, NPO

Figure 2. Transformer and Connector for the Transducer

A matched transformer-transducer pair is included on the PGA450Q1EVM. Table 4 lists closed-top transducers and tunable push-pull transformers from various manufacturer numbers that can be matched with a tuning capacitor to create a sensor pair. By default, the transducer and transformer provided with the EVM are the Murata MA58MF14-7N and Mitsumi K5-R4, respectively.

Table 4. Transducer and Transformer Manufacturer Part Numbers

Manufacturer	Part Number
Transducer (at P5 or P6)	
Murata	MA58MF14-7N
Murata	MA58AF14-0N
Transformer (TR1)	
Mitsumi	K5-R4
Toko	N1342DEA-0008BQE=P3

Murata has provided the following note with regard to the availability and ability to order their ultrasonic sensors:

- For small quantity sample requests, inquire online at the Murata website: https://www.murata.com/en-us/contactform.
- For consumer-grade applications exposed to controlled environments, consider open-structure sensors, such as the Murata MA40H1S-R. Distributors will typically have these sensors readily available for purchase online.
- For automotive-grade sensors (such as the transducers listed in Table 4 for applications exposed to

harsh environments, consider closed-top waterproof sensors, and inquire with distributors. The distributors will then request an order with Murata. Lead times for these sensors may vary up to several weeks.

Key ultrasonic sensor specifications are frequency, sensitivity, and directivity. The transformer is used to excite the transducer. The transformer is center tapped to double the voltage. Typically, a tuning capacitor is needed to match the resonant frequency between the transducer and transformer.

$$C_{TUNE} = \frac{C_T \times L_T}{L_{SEC}} - C_{PT} \quad (1)$$

C_{PT}, R_T, L_T, and C_T are characteristics of the transducer, L_{SEC} is the secondary inductance of the transformer, and C_{TUNE} is an external capacitor placed across the terminals of the transducer.

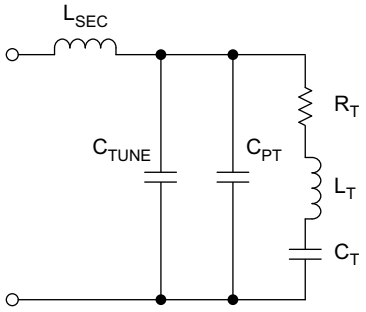


Figure 3. Equivalent Circuit of Transformer-Transducer Sensor Pair

8 PGA450-Q1 Communication Interfaces

The PGA450-Q1 device has several communication options including: SPI, LIN, and UART. All of these communication interfaces and related circuitry are present on the PGA450Q1EVM.

8.1 SPI

SPI is the main communication method on the PGA450-Q1 device. The 8051W inside the device must be put in reset to communicate using SPI. The SPI signals can be monitored with the CS, SCLK, SDI, and SDO test points on the EVM.

8.2 LIN

The EVM includes a LIN transceiver, which is the master transceiver. The PGA450-Q1 device is always a slave on the LIN bus and has the slave transceiver integrated inside the device.

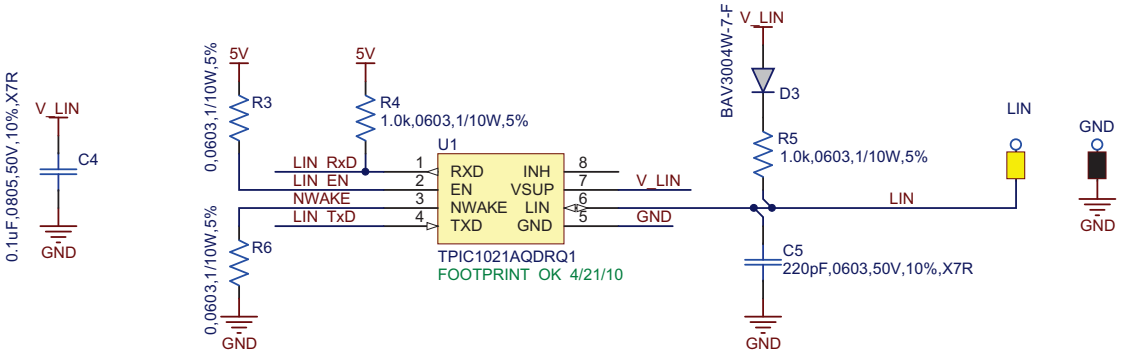


Figure 4. LIN Master Transceiver

The 5-V supply in Figure 4 is provided by the USB communication board.

8.3 UART

An RS-232 transceiver (MAX3221) is present on the EVM that can be used as a debugging interface from the 8051 MCU to a host PC. The circuit connects the TXD and RXD pins on the PGA450-Q1 device to the MAX3221 device. The RX and TX RS-232 signals are routed to a standard DB-9 connector on the EVM. The RS-232 circuit is shown in Figure 5.

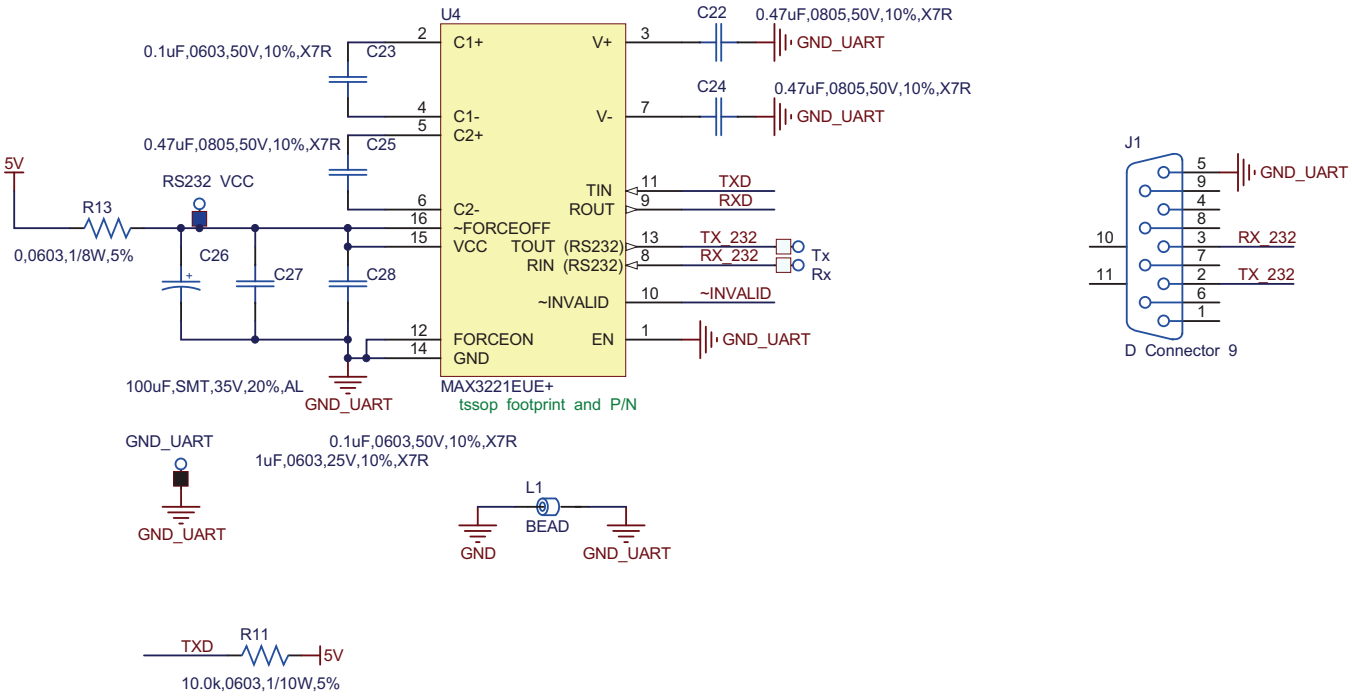


Figure 5. RS232 Transceiver

9 Controlling the PGA450-Q1 Memory Spaces With the GUI

The PGA450Q1EVM is controlled by the user through a PC with the USB communication board and associated GUI. The PGA450Q1EVM GUI provides ways to manipulate all of the register spaces present inside the PGA450-Q1 device (ESFR, EEPROM, RAM, OTP, DEVELOPMENT RAM). The following sections describe how to manipulate the register spaces.

9.1 Using the Register Grids to Manipulate the Register Spaces

Most of the register spaces have register grids associated with them that provide a simple way to read/write the registers in the grid. There are eight buttons that are associated with the grid operations: ZERO GRID, DESELECT GRID, SAVE GRID, RECALL GRID, READ SELECTED, WRITE SELECTED, READ ALL, and WRITE ALL. These buttons perform operations on whichever register grid is currently displayed. For example, when the GUI first loads, the ESFR register tab is displayed, if any of the previously listed buttons are pressed they perform operations on the ESFR register space. Each of the GRID functions is in one of the following sections.

9.1.1 ZERO GRID

The ZERO GRID button replaces the contents of the entire grid with 0.

9.1.2 DESELECT GRID

The DESELECT GRID button removes any selections that have been made in the grid without performing any operations on the registers that were selected.

9.1.3 SAVE GRID

The SAVE GRID button takes the contents of the register grid and saves them to a .TXT file. The data is saved in comma-separated-values format.

9.1.4 RECALL GRID

The RECALL GRID button opens a prompt that allows the user to select a .TXT file that was produced during the SAVE GRID operation and then loads the grid with the contents from the .TXT file.

9.1.5 READ SELECTED

The READ SELECTED button performs a read operation on any registers in the grid that have been selected by clicking the desired register number. Any selected registers are displayed blue.

9.1.6 WRITE SELECTED

The WRITE SELECTED button will perform a write operation on any registers in the grid that have been selected by clicking the register number or modifying the register contents. Any selected registers are displayed in blue and any modified registers are highlighted in yellow. Any blue or yellow registers are written to when the WRITE SELECTED button is pressed.

9.1.7 READ ALL

The READ ALL button performs a read operation on every register in the grid.

9.1.8 WRITE ALL

The WRITE ALL button performs a write operation on every register in the grid.

9.2 ESFR Registers

The ESFR register displays all the function registers that are specific to PGA450-Q1 functionality. The user can set each register manually through SPI or define register values in 8051W firmware. An *Evaluation* tab on the right side helps to set the ESFR registers for quick evaluation. More details of the *Evaluation* tab are described in a later section.

9.3 EEPROM Registers

The EEPROM in the PGA450-Q1 device comprises 32 bytes of EEPROM and an EEPROM cache. When the EEPROM grid is updated in the GUI, only the cache is updated.

9.3.1 Program EEPROM

The *Program EEPROM* button writes 0x01 to the EE_CTRL ESFR to program the EEPROM memory cells. The EEPROM memory cells are programmed with the values that are in the EEPROM cache inside the PGA450-Q1 device.

The contents in the GUI are first transferred to the cache and then the cache is programmed.

9.3.2 Reload EEPROM

The *Reload EEPROM* button reloads the EEPROM cache inside the PGA450-Q1 device with the values in the EEPROM memory cells. It then performs a READ ALL to update the grid with the refreshed contents of the EEPROM bank.

The contents of the EEPROM cache can be updated on the GUI by clicking on the READ SELECTED or READ ALL button.

9.4 RAM

The RAM tab is set up only for individual register read/writes without the use of the grid. When this tab is displayed, the READ SELECTED / READ ALL and WRITE SELECTED / WRITE ALL buttons perform the same operations, respectively.

The PGA450-Q1 device has 512 bytes of general-purpose RAM. This general-purpose RAM is memory-mapped into two different memory spaces inside the PGA450-Q1 device: internal memory space (0x00–0xFF) and external memory space (0x0300–0x03FF).

The user must select the appropriate memory space in the Combo Box before making the Read/Write request. Note the valid address range for the two RAM sections.

9.5 OTP

The OTP tab is set up only for individual register read/writes without the use of the grid. When this tab is displayed, the READ SELECTED / READ ALL and WRITE SELECTED / WRITE ALL buttons perform the same operations, respectively. The OTP tab also contains buttons used to load a .HEX 8051 program file into the 8051 MCU in the PGA450-Q1 device.

The PGA450Q1EVM could potentially have two devices: a device that is soldered on the EVM and a device that is in the socket. The GUI allows programming of either device. When the device choice is made, the GUI automatically resets the microprocessor for the respective device so that it is ready to load OTP through SPI

NOTE: The OTP program requires R2 to be populated and the VPWR:VOTP jumper to be installed. This connects the VPROG_OTP 8-V supply on the VP_OTP pin during programming. See the data sheet for more details.

9.5.1 Load .HEX File Into GUI

The *Load .HEX File into GUI* button is used to load the contents of a .HEX file into the GUI RAM for use with other operations. When the button is pressed, a second window opens that allows the user to locate and open the desired .HEX file on the PC. See Figure 6 for an example of this operation.

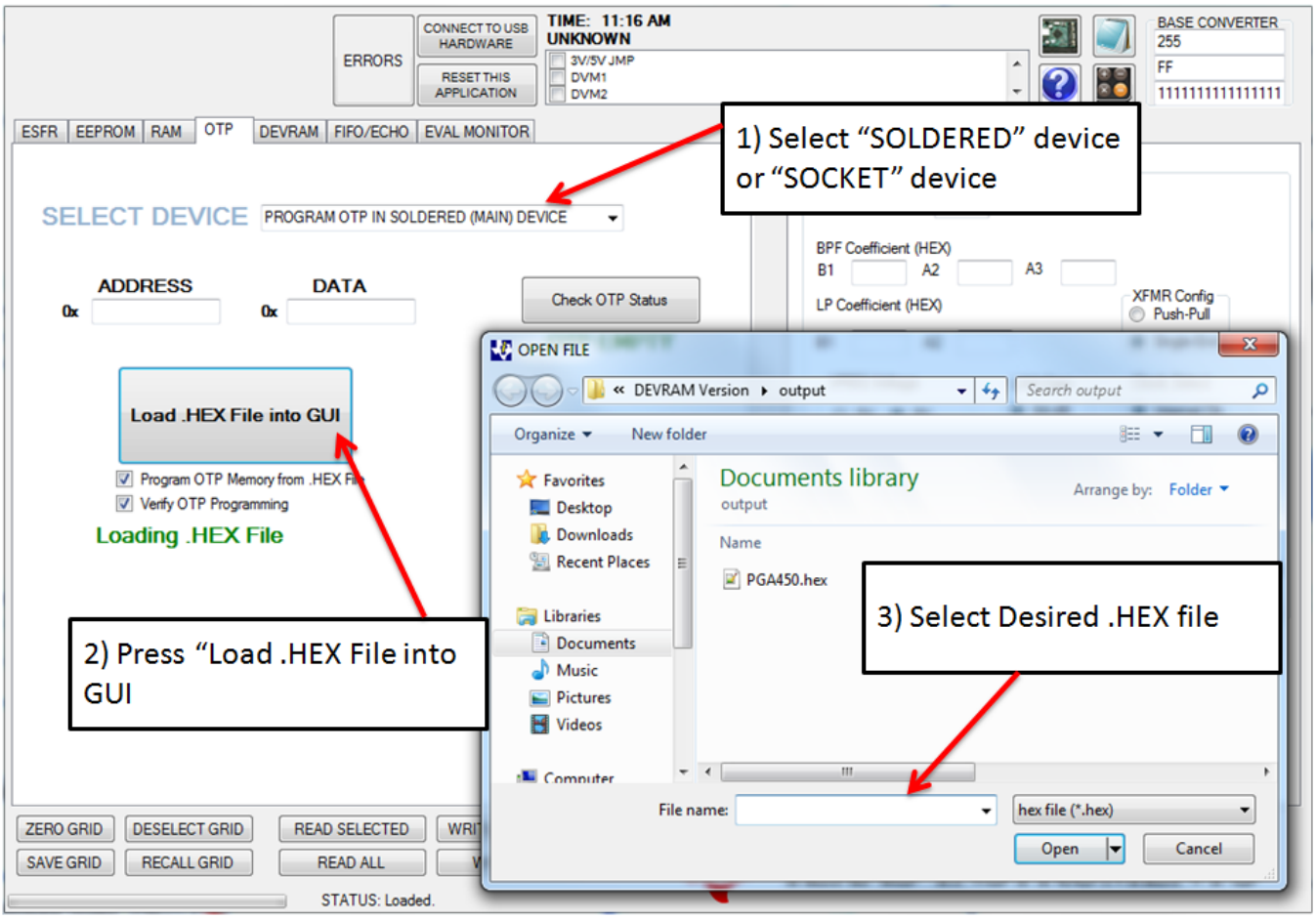


Figure 6. Loading a .HEX File Into the GUI

9.5.2 Program OTP Memory from .HEX File

If the *Program OTP Memory from .HEX File* check box was checked (default) when the .HEX file was loaded into the GUI, the OTP memory is programmed with the contents of the .HEX file.

9.5.3 Verify OTP Programming

If the *Verify OTP Programming* button was also checked (default), then after the OTP memory is finished programming, the GUI reads the contents of the OTP memory through SPI and verifies against the .HEX file. If the OTP memory matches the contents of the .HEX file, the GUI displays the message “OTP Memory Verification Successful,” as seen in Figure 7.

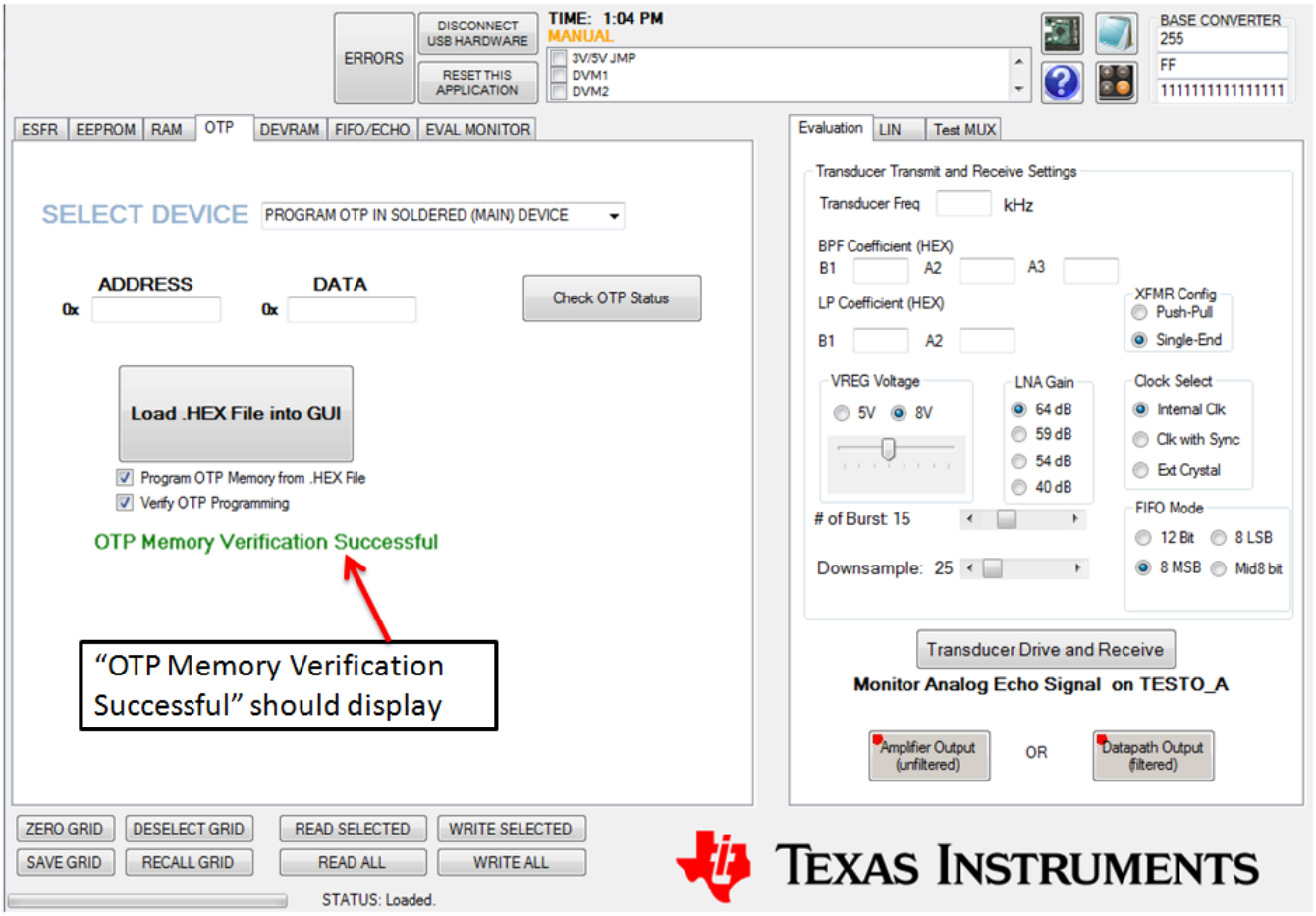


Figure 7. OTP Memory Successful Programming Verification

Check OTP Status

Press the "Check OTP Status" button to verify what is currently programmed into OTP. The three possible results are:

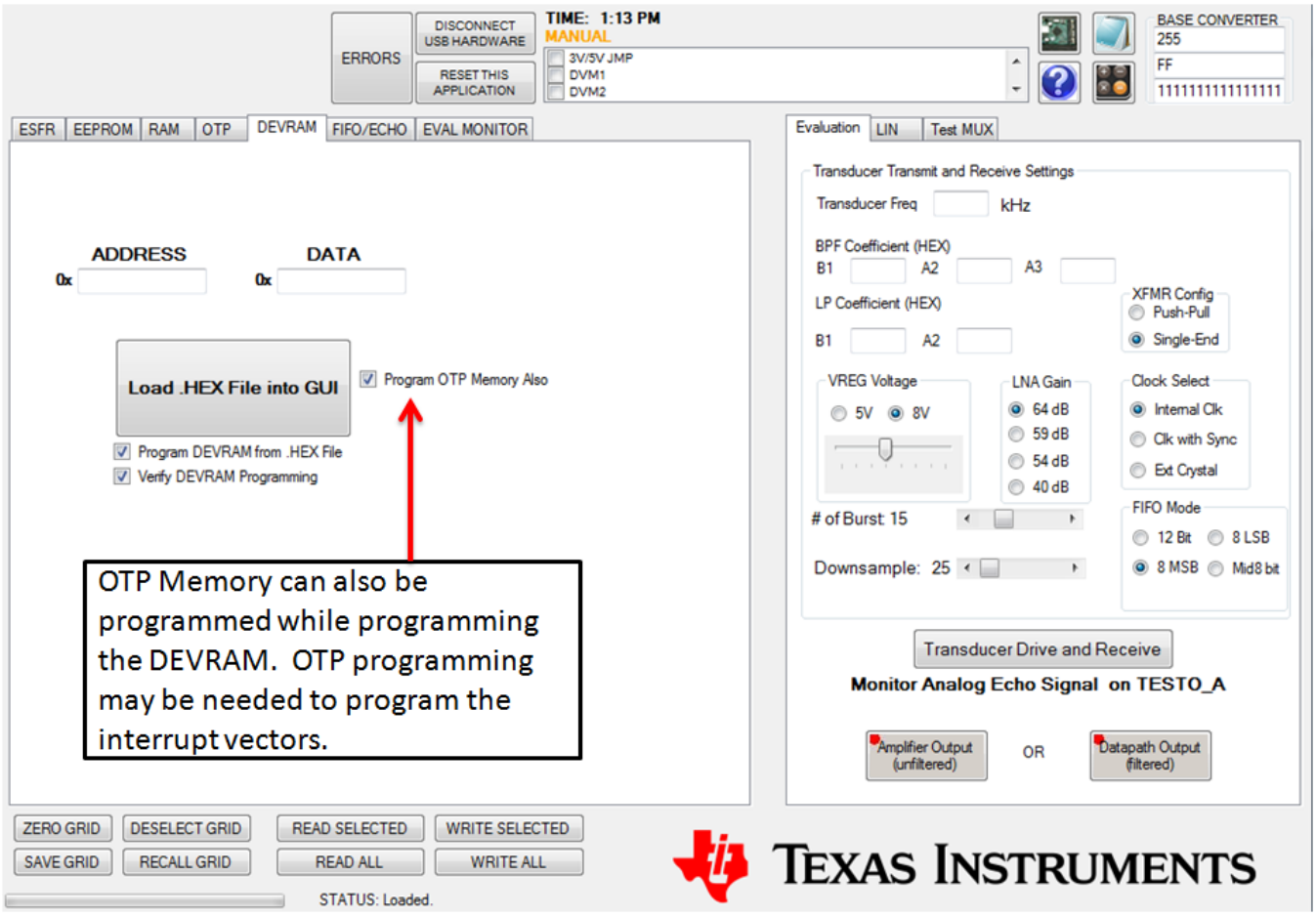
- Programmed to Jump to DEVRAM: The jump to DEVRAM statement has been programmed into the OTP. This means that programs loaded into the DEVRAM will execute.
- OTP Empty: Nothing has been programmed in the OTP.
- Programmed: The OTP has been programmed with something other than the jump to DEVRAM statement.

9.6 DEVRAM

The DEVRAM tab is set up only for individual register read/writes, without the use of the grid. When this tab is displayed, the READ SELECTED / READ ALL and WRITE SELECTED / WRITE ALL buttons perform the same operations, respectively. The DEVRAM tab also contains buttons used to load a .HEX 8051 program file into the 8051 MCU in the PGA450-Q1 device.

The process of loading the .HEX file into the DEVRAM is identical to that of OTP.

For a pristine IC that has never been programmed (OTP Status reads "OTP Empty"), in order to run software from DEVRAM, the OTP memory must be programmed with some specific instructions to redirect the 8051 µP to DEVRAM. This must only be done once. To do this, check the "Program OTP Memory Also" button, and the GUI will program the OTP with this jump statement as well as program the DEVRAM with the selected HEX file.



Note that OTP programming may be required if the interrupt vectors are not programmed

Figure 8. OTP Memory can be programmed while programming the Development RAM

9.7 FIFO/ECHO

9.7.1 FIFO

The PGA450-Q1 device has a FIFO RAM that contains the output of the digital data path. The contents of the FIFO RAM can be displayed on the GUI and/or can be plotted in Excel.

The FIFO RAM is displayed in the form of a grid. The GUI grid contents can be updated either by clicking on the READ ALL button or by clicking on the READ SELECTED button.

The FIFO RAM contents can be displayed on the GUI and plotted in Excel by clicking the *Read and Save FIFO Data to File* button.

NOTE: Note: Microsoft Office version 2007 or above is required for this function to work properly.

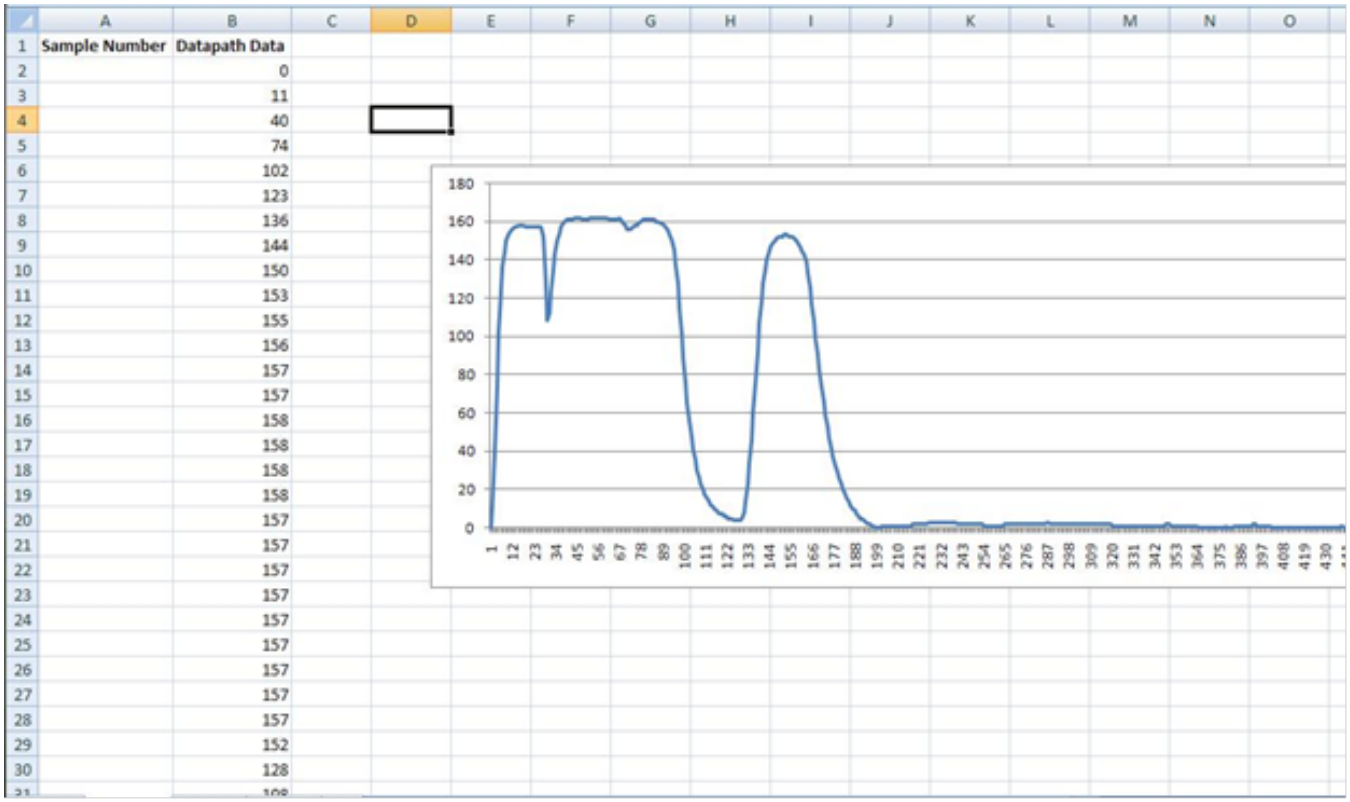


Figure 9. Echo Data Stored in FIFO RAM Plotted in Excel

EVAL Monitor

This tab graphs the output of the digital data path directly in the GUI. The 8051W microcontroller must be in reset to use this tab.

No. of Loops

This option selects how many times the GUI will transmit a burst and plot the echo data.

Trigger

If "Auto" is displayed, the GUI will continue sending bursts and plotting the echo data until the "Loops Complete" count matches the "No. of Loops." If "USER" is displayed, the GUI will stop and wait for the user to press the green flashing "Trigger" button before continuing.

Resolution

This button has three options, "FULL", "1/2", and "1/4". The "FULL" setting plots all of the echo data points, but takes more time. The "1/2" and "1/4" options reduce the number of data points plotted which results in faster plotting.

Clear Plot

The "CLR" button clears all data from the graph. If the "Clear Plot" option is checked, echo data will be cleared from the plot every loop. If "Clear Plot" is not checked, every loop will plot the new echo data in a new color on top of the existing data on the graph.

Export Data to Excel

This option exports the echo data to Excel for each loop.

Start/Stop

Click on the "Start" button to start the first loop. Click on "Stop" at any time to stop the program immediately.

10 LIN Master

The PGA450Q1EVM GUI communicates with the PGA450-Q1 device using LIN. The USB Communication board UART is the LIN master, and the PGA450-Q1 device is the LIN slave. The GUI can be used to configure the LIN frames that are transmitted to the PGA450-Q1 device.

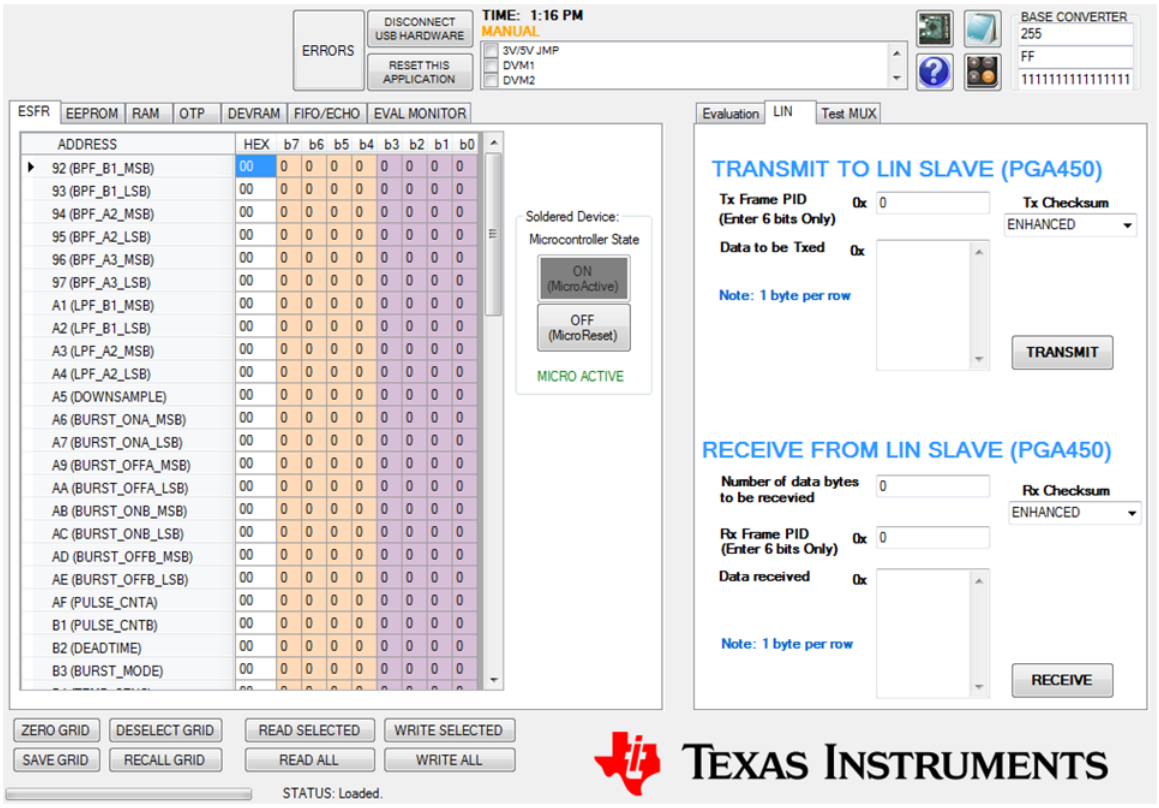


Figure 10. LIN Master on GUI

In order to transmit data to PGA450-Q1 device using a LIN frame, the user must do the following:

1. Enter the Frame PID in Edit Box corresponding to “Tx Frame PID”. The PID must be entered in hex. Note that valid PID ranges from 0x00 to 0x3F. The GUI software calculates the parity bits using the LIN 2.1 method before the PID is transmitted to the slave.
2. Enter 0–8 bytes of data in the “Data to be Txed” box. Each data byte must be entered in Hex.
3. Select the CLASSIC or ENHANCED checksum, which must match the LIN checksum setting in the PGA450-Q1 ESFR LIN_CFG register.
4. Click on the TRANSMIT button

In order to receive data from PGA450-Q1 device using a LIN frame, the user must do the following:

1. Enter the Frame PID in Edit Box corresponding to “Rx Frame PID”. The PID must be entered in hex. Note that valid PID ranges from 0x00 to 0x3F. The GUI software calculates the parity bits using the LIN 2.1 method before the PID is transmitted.
2. Enter the number of data bytes the user expects back from the PGA450-Q1 device.
3. Select the CLASSIC or ENHANCED checksum
4. Click on the RECEIVE button

The data received from the PGA450-Q1 device is displayed in the *Data Received* box.

If the data communication is not working, try *Reset This Application*, which power-cycles the LIN master IC on the EVM.

11 Keil uVision Settings for Programming Firmware to the PGA450-Q1 DEVRAM or OTP Memory

11.1 Objective

To modify the source code made available through the PGA450Q1EVM firmware installer, download the Keil C51 Development Tool for all 8051 devices, which includes the uVision IDE necessary to open and edit the PGA450-Q1 project file. Keil products use a license management system. Without a current license, the product runs as a *lite* or *evaluation* edition with a few limitations.

11.2 Setup

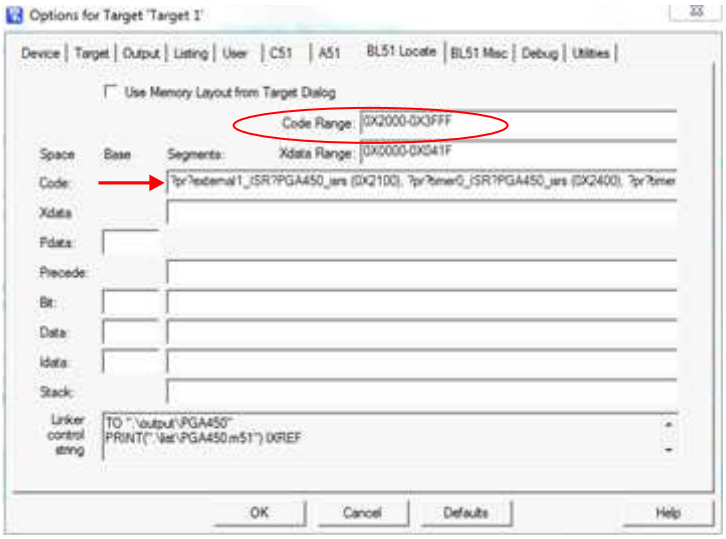


Figure 11. DEVRAM Target Options

To Program to DEVRAM:

1. Change the code range to the DEVRAM memory space.
   (a) Right click on *Target 1* in the project window, and select *Options for Target*.
   (b) Go to the *BL51 Locat*e tab, and modify the *Code Range* to go from 0x2000–0x3FFF.
2. Copy the following to the *Code* box:
   ?pr?external1_ISR?PGA450_isrs (0X2100),
   ?pr?timer0_ISR?PGA450_isrs (0X2400),
   ?pr?timer1_ISR?PGA450_isrs (0X2800),
   ?pr?serial_ISR?PGA450_isrs (0X2C00),
   ?pr?linPID_ISR?PGA450_isrs (0X3000),
   ?pr?linSciRxData_ISR?PGA450_isrs (0X3400),
   ?pr?linSciTxData_ISR?PGA450_isrs (0X3800),
   ?pr?external0_ISR?PGA450_isrs (0X3900),
   ?pr?linSync_ISR?PGA450_isrs (0X3D00)
3. Comment out the OTP section in STARTUP.A51, and uncomment the OTP section
   (a) An example of this is shown in Figure 13.

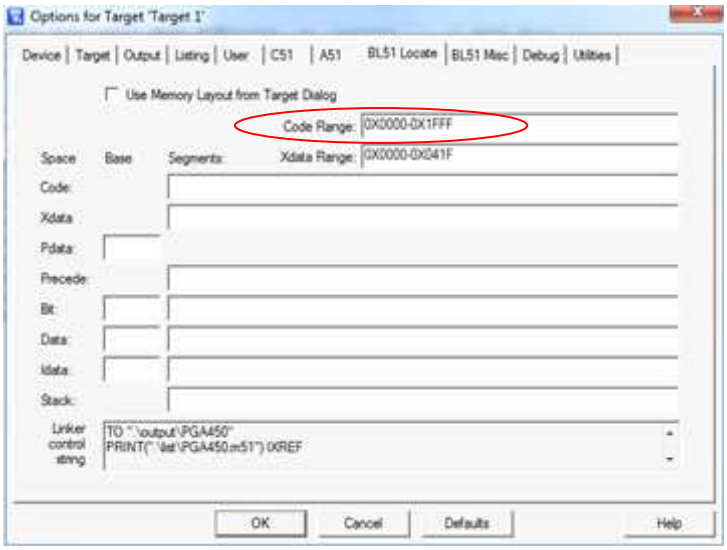


Figure 12. OTP Target Options

To Program to OTP:

1. Change the code range to the OTP memory space
   (a) Right click on *Target 1* in the project window, and select *Options for Target*.
   (b) Go to the *BL51 Locate* tab, and modify the *Code Range* to go from 0x0000–0x1FFF.
2. Delete everything in the *Code* box.
3. Comment out the DEVRAM section in STARTUP.A51, and uncomment the OTP section.
   (a) An example of this is shown in Figure 14.

```
114  //------------ For DEVRAM program
115
116  ?STACK          SEGMENT   IDATA
117
118                  RSEG    ?STACK
119                  DS      1
120
121                  EXTRN CODE (?C_START)
122                  PUBLIC  ?C_STARTUP
123
124                  CSEG    AT      0
125  ?C_STARTUP:     LJMP    STARTUP1
126
127                  CSEG    AT      0x2000  ; relocate to Development RAM:
128  //------end of DEVRAM program section
129
130  //OTP section currently commented out
131  /*
132  //----------- For OTP program
133  ?C_C51STARTUP   SEGMENT   CODE
134  ?STACK          SEGMENT   IDATA
135
136                  RSEG    ?STACK
137                  DS      1
138
139                  EXTRN CODE (?C_START)
140                  PUBLIC  ?C_STARTUP
141
142                  CSEG    AT      0
143  ?C_STARTUP:     LJMP    STARTUP1
144
145                  RSEG    ?C_C51STARTUP
146
147  //--------end of OTP program section
148  */
```

Figure 13. DEVRAM STARTUP.A51 Example

```
115  //DEVRAM section currently commented out
116  /*
117  //-------------- For DEVRAM program
118
119  ?STACK          SEGMENT   IDATA
120
121                  RSEG    ?STACK
122                  DS      1
123
124                  EXTRN CODE (?C_START)
125                  PUBLIC  ?C_STARTUP
126
127                  CSEG    AT      0
128  ?C_STARTUP:     LJMP    STARTUP1
129
130                  CSEG    AT      0x2000  ; relocate to Development RAM:
131  //----------end of DEVRAM program section
132  */
133
134  //--------------- For OTP program
135  ?C_C51STARTUP   SEGMENT   CODE
136  ?STACK          SEGMENT   IDATA
137
138                  RSEG    ?STACK
139                  DS      1
140
141                  EXTRN CODE (?C_START)
142                  PUBLIC  ?C_STARTUP
143
144                  CSEG    AT      0
145  ?C_STARTUP:     LJMP    STARTUP1
146
147                  RSEG    ?C_C51STARTUP
148
149  //----------end of OTP program section
150
```

Figure 14. OTP STARTUP.A51 Example

Instructions: Build the *PGA450.uvproj* to generate the custom .HEX file used to program the internal 8051 core. The *LIN Demonstration using PGA450Q1EVM Firmware Rev 2.1* provides instructions on how to upload the .HEX file using the EVM GUI.

12 Use Case

The purpose of this section is to provide step-by-step instructions on the setup and some basic evaluation procedures.

12.1 Evaluation Through SPI Communication

In order to provide a quick evaluation of the IC performance using the TI EVM and GUI without having to develop sophisticated 8051 µP software, the GUI provides an intuitive interface tab, *Evaluation Tab*, that collects all necessary information regarding the transducer drive and receive. For transducer drive, it includes: transducer frequency; transducer drive voltage, VREG; transformer configuration; and number of drive pulses. For transducer signal receive, it includes signal-processing parameters: LNA gain setting; BPF and LPF coefficient; clock selection; FIFO mode; and FIFO downsample size.

1. Make sure all jumpers are connected according to the default settings, see Section 5.2.
2. Connect the hardware and power supply, see Section 4. Make sure USB cable is connected to the computer and the interface board. It is recommended to monitor power supply current. Normal idle current is around 6 mA. Active current is around 15 mA.
3. Launch GUI software on computer.
4. Click the "OFF (Micro Reset)" button to put the Micro in reset, then click READ ALL to read the default register values. Some default values are loaded in the table grid. If all are 0 or FF values, this means that there is an error with communication to the device. Check the hardware setup or restart the GUI software.

   Fill out the "Evaluation" tab with the values shown in Figure 15.

   Use the "Eval Monitor" tab to send bursts and view the resulting echo data.

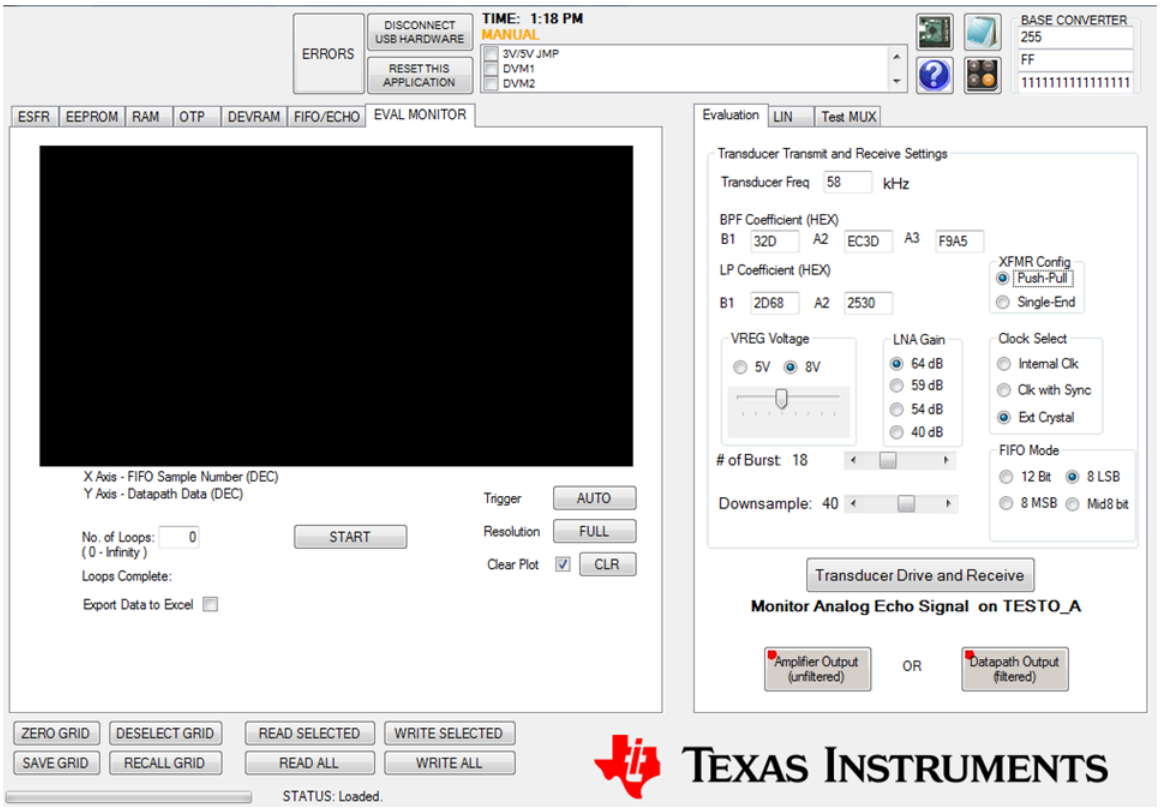


Figure 15. Evaluation Tab Setting

After all information is entered, make sure the device is in the micro reset state, then hit the *Transducer Drive and Receive* button to start the burst and receive.

12.2 Monitoring the Signal Path

The PGA450-Q1 device has two useful test modes that allow users to quickly observe the echo signal as an amplified analog signal or from a DAC output which converts a digitally filtered echo signal. In the *Evaluation* tab, quick-access buttons *Amplifier Output (unfiltered)* and *Datapath Output (filtered)* are available. The signal is viewable on the DACO pin. Only one mode can be selected at a time. See Figure 16 and Figure 17 for the captured waveforms.

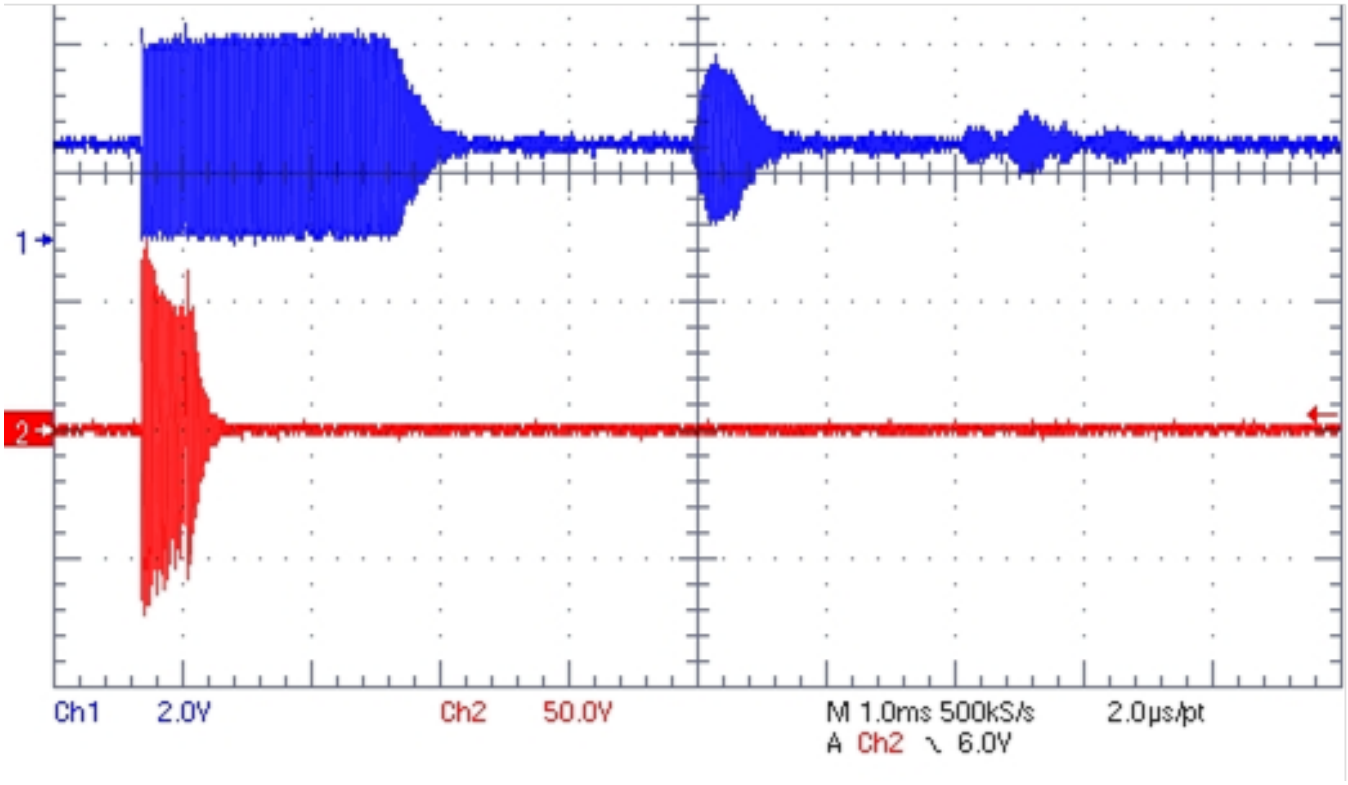


Figure 16. Echo Analog Waveform Output (Channel1), Drive voltage (Channel 2)

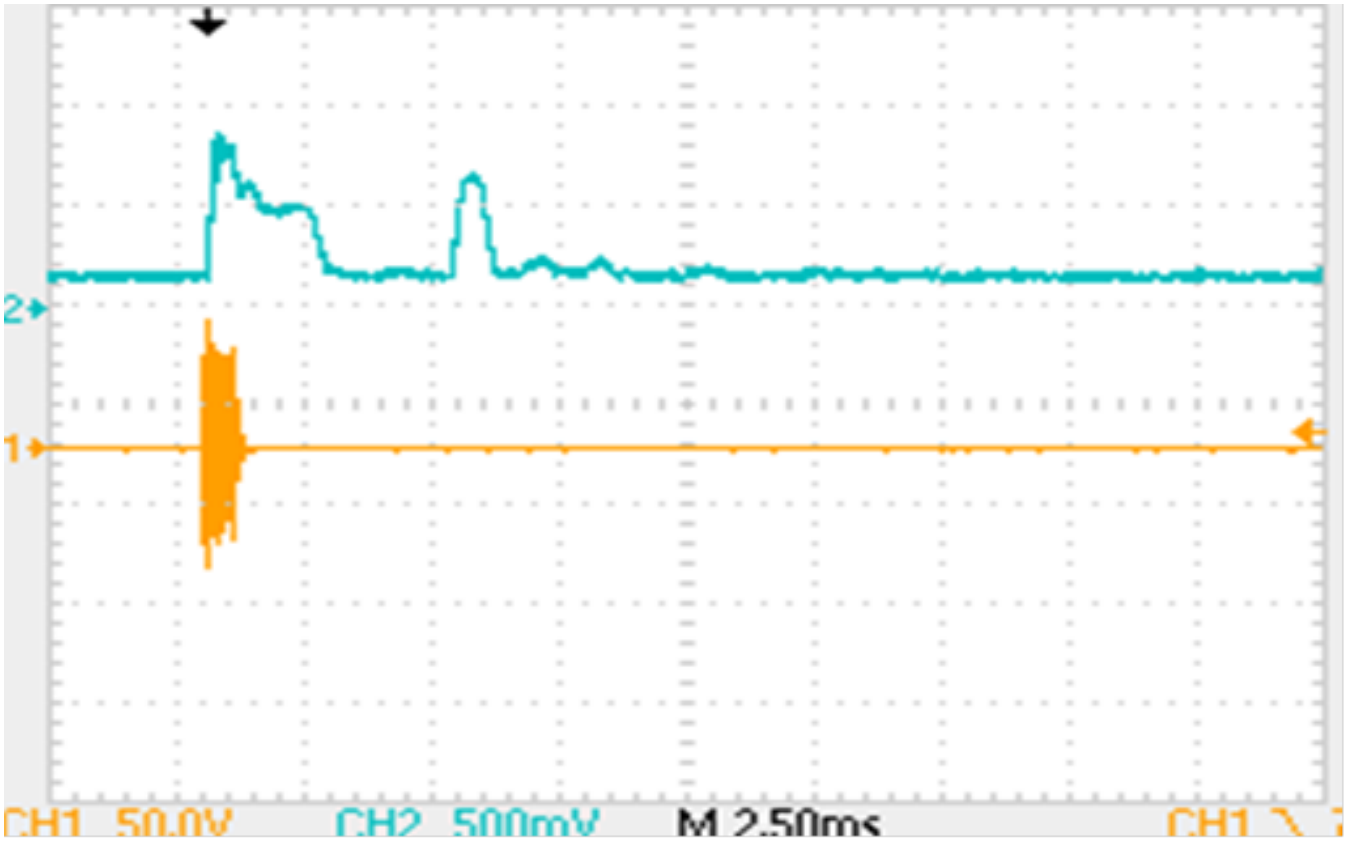


Figure 17. DAC Output of Filtered Signal (Channel 2) and Drive Voltage (Channel 1)

13 PGA450Q1EVM Schematics and Layout Drawings

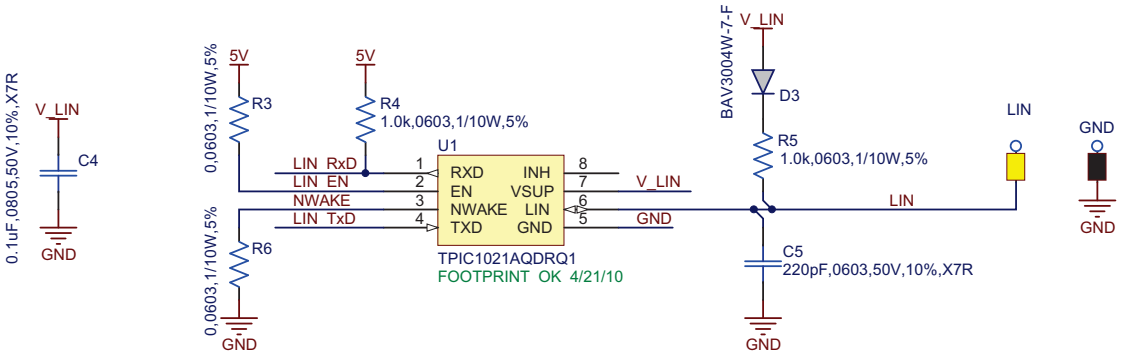


Figure 18. Schematic, LIN

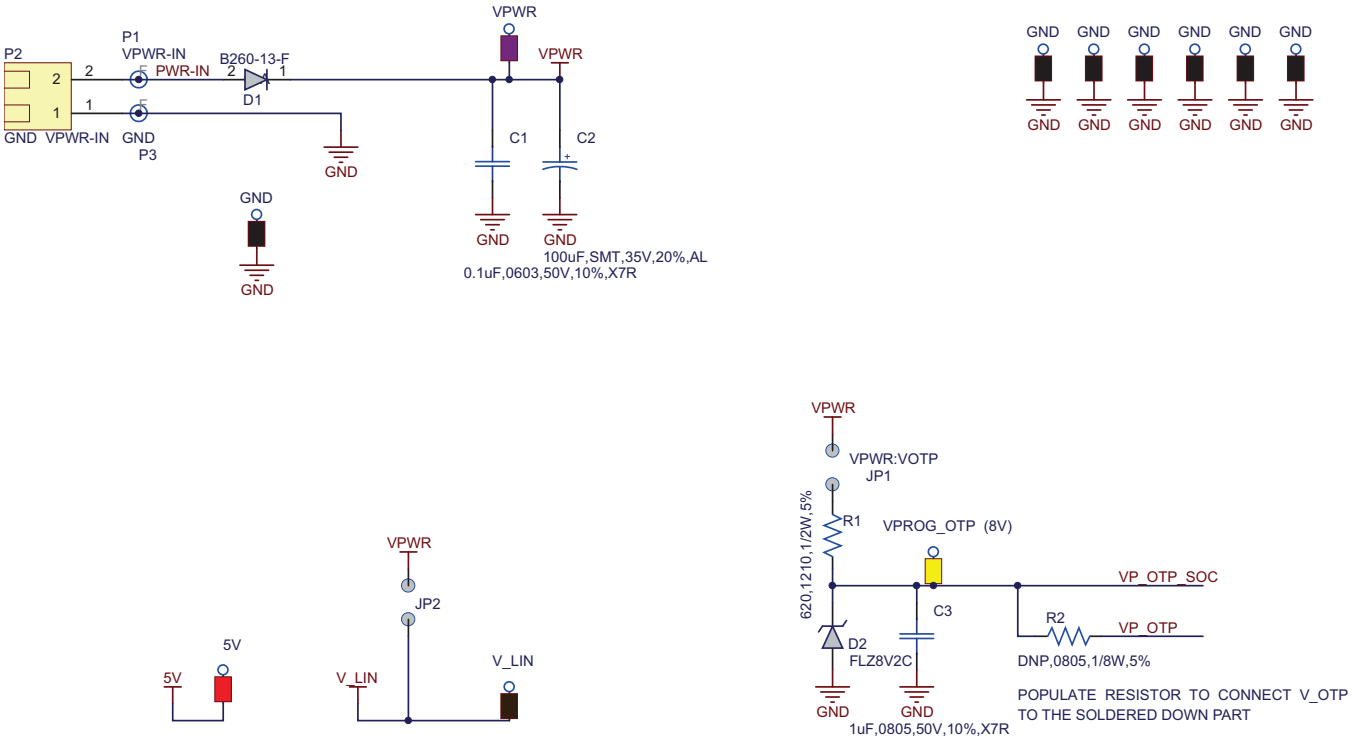


Figure 19. Schematic, Power

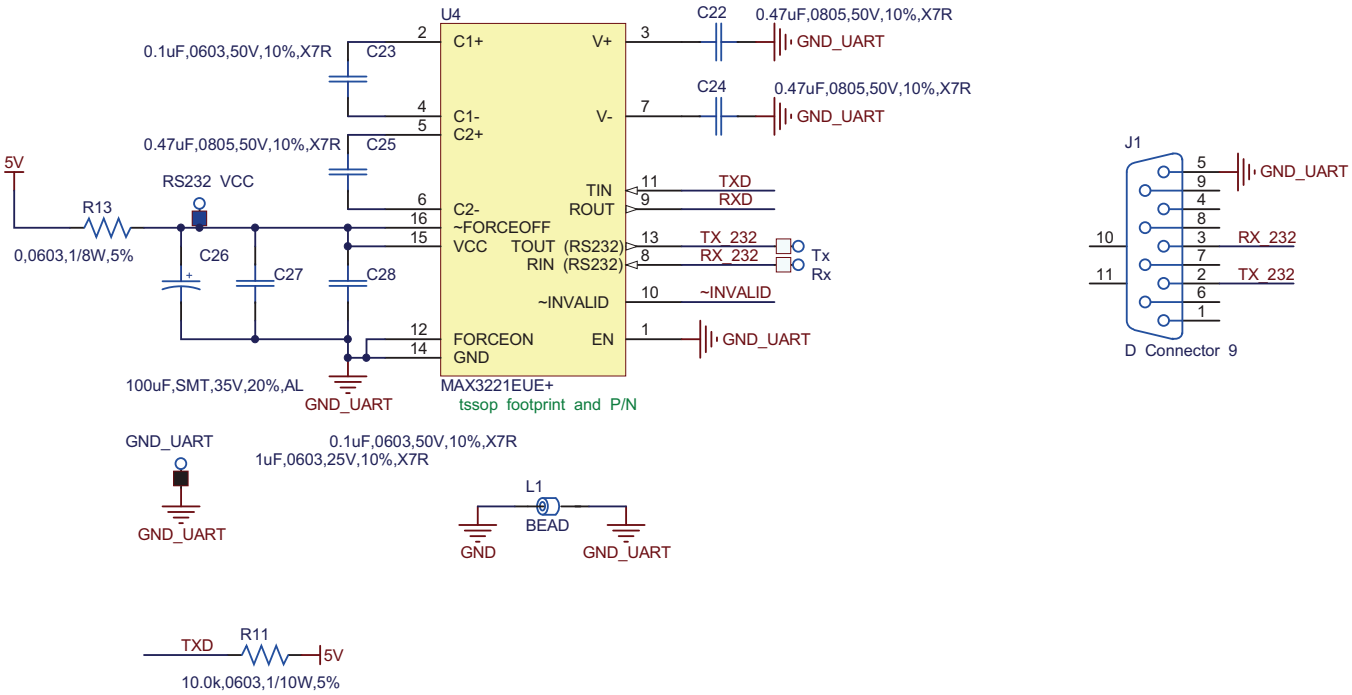


Figure 20. Schematic, RS232

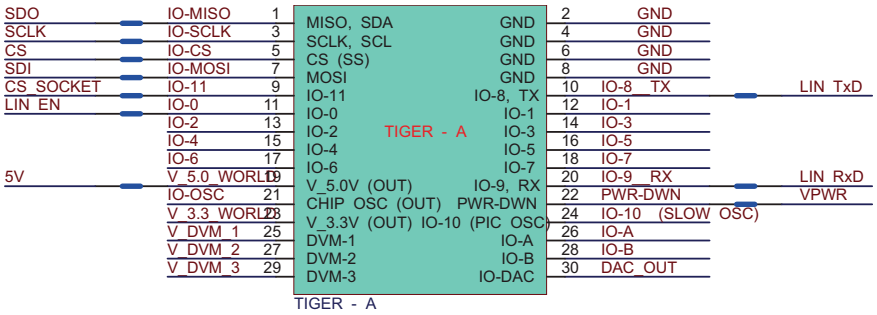
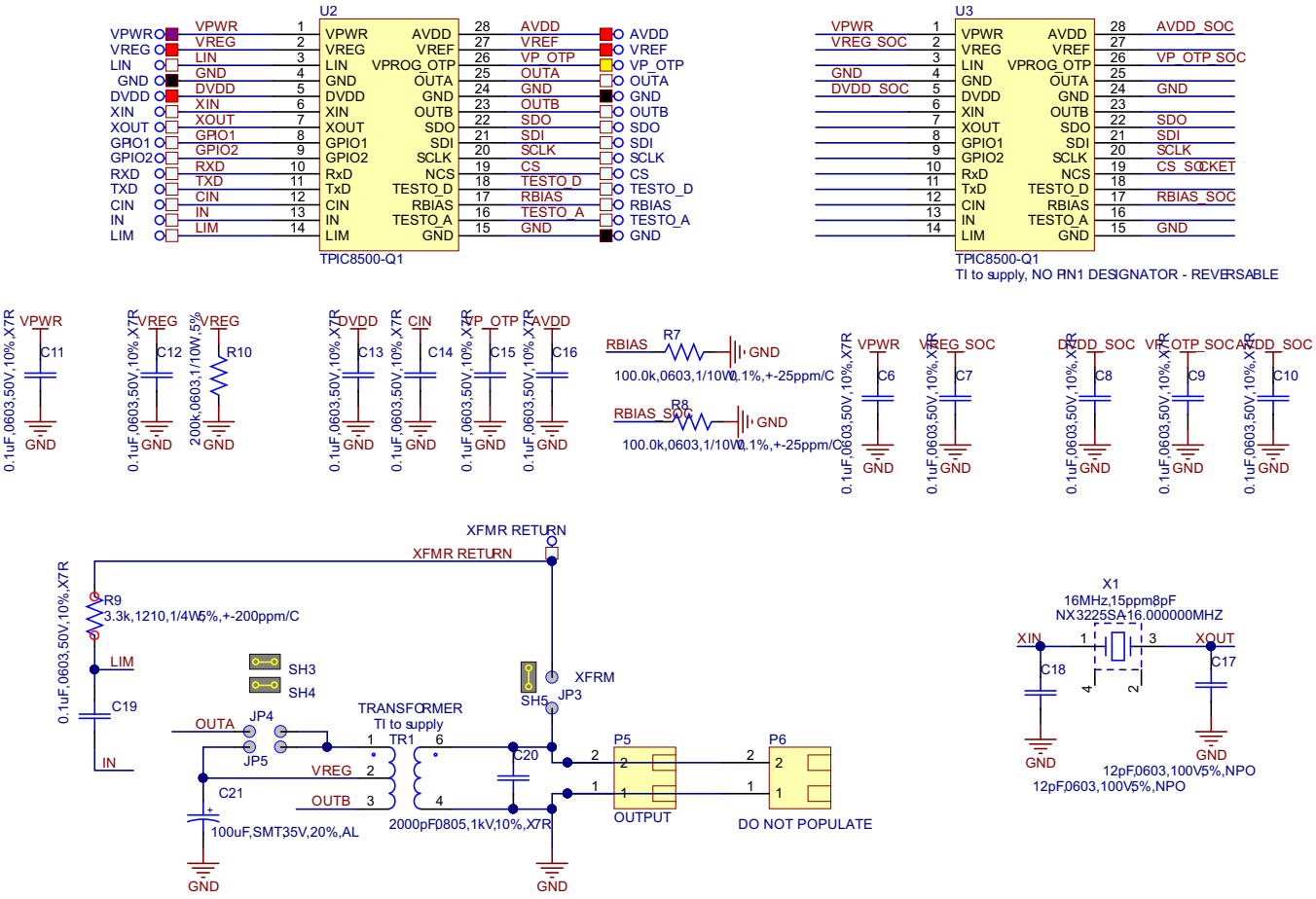


Figure 21. Schematic, USB Controller



NOTE: C20 is a temperature compensation capacitor for the XDCR. Match C20 to the selected XDCR. If XDCR is Murata MA58MF14-7N, 2000-pF capacitance is installed, and 1500-pF capacitance is provided as an alternative. If XDCR is Murata MA58AF14-0N. 1500-pF capacitance is installed. Alternative specifications include: 1500 pF, 0805, 250 V, 20%, NPO

Figure 22. Schematic, PGA450-Q1 (TPIC8500-Q1)

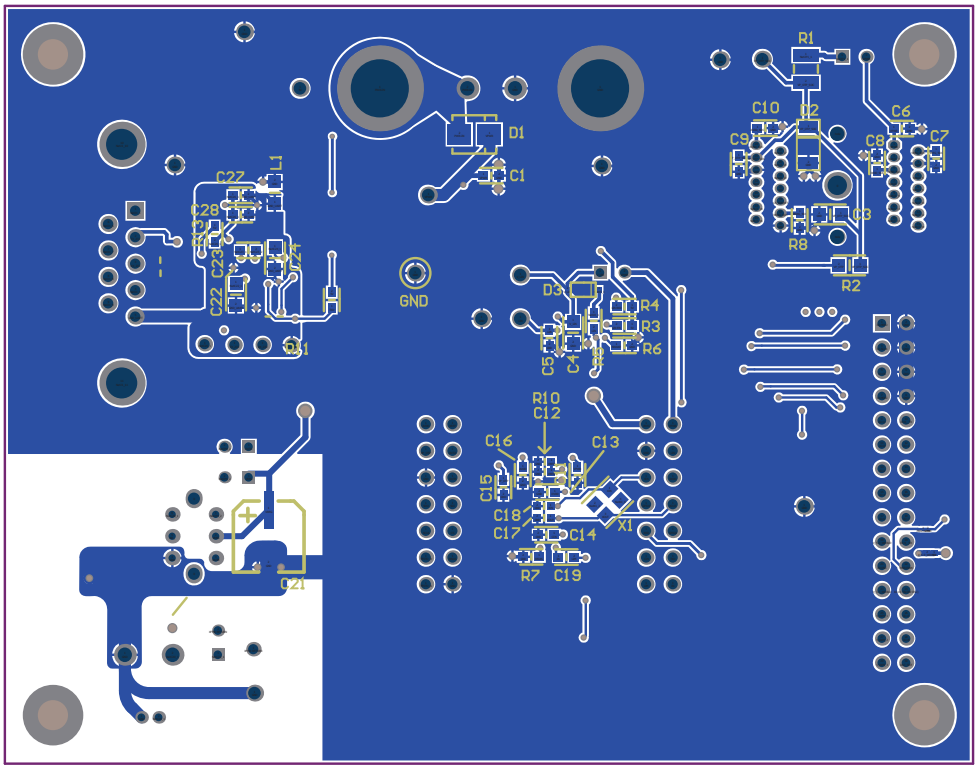


Figure 23. PCB Layout, Bottom

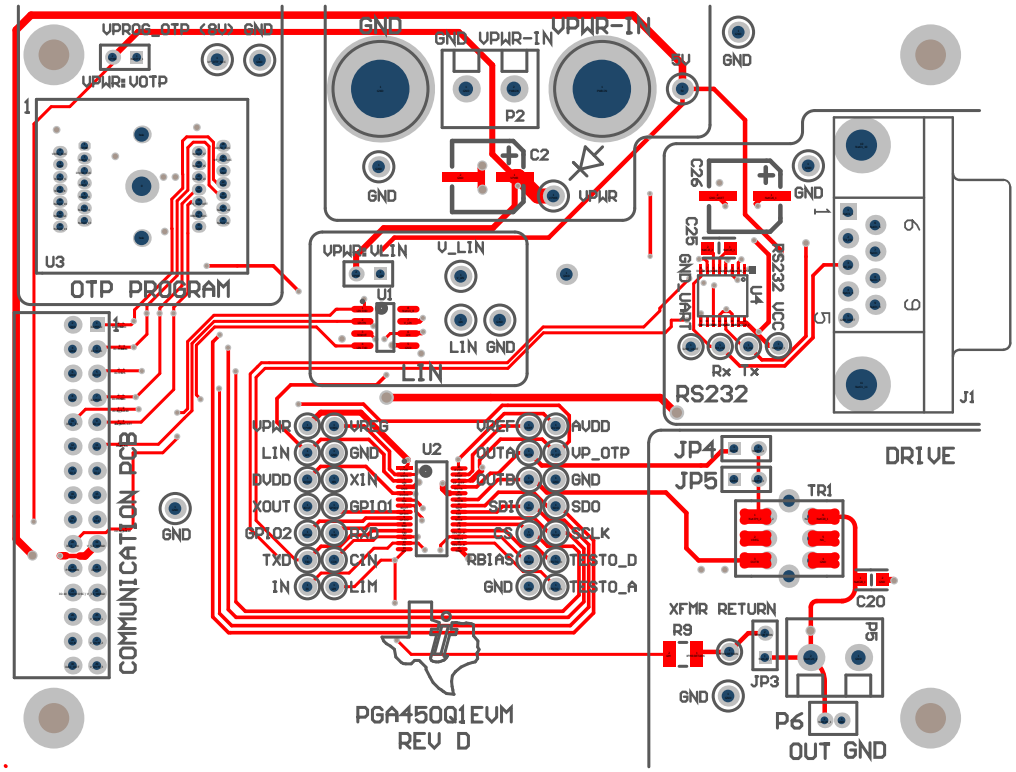


Figure 24. PCB Layout, Top

Revision History

Changes from B Revision (June 2015) to C Revision **Page**

- Changed the *Transformer and Connector for the Transducer* schematic 8
- Changed the Murata part numbers for the transducer in the *Transformer and Transducer* section 8
- Added Murata note on availability of ultrasonic sensors 9
- Changed the *Schematic, PGA450-Q1 (TPIC8500-Q1)* 26
- Changed the *PCB Layout, Top* layout image 27

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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