



October 2015

FDN5630

# FDN5630

## 60V N-Channel PowerTrench® MOSFET

### General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

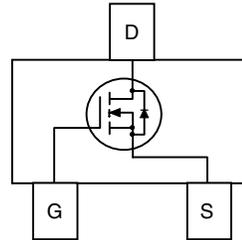
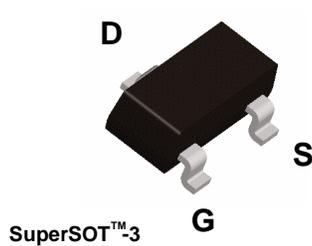
This MOSFET features very low  $R_{DS(ON)}$  in a small SOT23 footprint. Fairchild's PowerTrench technology provides faster switching than other MOSFETs with comparable  $R_{DS(ON)}$  specifications. The result is higher overall efficiency with less board space.

### Features

- 1.7 A, 60 V.  $R_{DS(ON)} = 0.100 \Omega @ V_{GS} = 10 \text{ V}$   
 $R_{DS(ON)} = 0.120 \Omega @ V_{GS} = 6 \text{ V}$ .
- Optimized for use in high frequency DC/DC converters.
- Low gate charge.
- Very fast switching.
- SuperSOT™ - 3 provides low  $R_{DS(ON)}$  in SOT23 footprint.

### Applications

- DC/DC converter
- Motor drives



### Absolute Maximum Ratings $T_A = 25 \text{ C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	60	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current - Continuous (Note 1a) - Pulsed	1.7	A
		10	
$P_D$	Power Dissipation for Single Operation (Note 1a) (Note 1b)	0.5	W
		0.46	
$T_J, T_{stg}$	Operating and Storage Junction Temperature Range	-55 to +150	$^{\circ}\text{C}$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	250	$^{\circ}\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	75	$^{\circ}\text{C/W}$

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
5630	FDN5630	7	8mm	3000 units

**Electrical Characteristics** $T_A = 25\text{ C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$		63		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA

**On Characteristics** (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1	2.4	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$		-6.9		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 1.7\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 1.7\text{ A}, T_J = 125^\circ\text{C}$ $V_{GS} = 6\text{ V}, I_D = 1.6\text{ A}$		0.073 0.127 0.083	0.100 0.180 0.120	$\Omega$
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 1.7\text{ V}$	5			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 1.7\text{ A}$		6		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		400	560	pF
$C_{oss}$	Output Capacitance			65	95	pF
$C_{riss}$	Reverse Transfer Capacitance			27	40	pF

**Switching Characteristics** (Note 2)

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$		10	20	ns
$t_r$	Turn-On Rise Time			6	15	ns
$t_{d(off)}$	Turn-Off Delay Time			15	28	ns
$t_f$	Turn-Off Fall Time			5	15	ns
$Q_g$	Total Gate Charge	$V_{DS} = 20\text{ V}, I_D = 1.7\text{ A},$ $V_{GS} = 10\text{ V},$		7	10	nC
$Q_{gs}$	Gate-Source Charge			1.6		nC
$Q_{gd}$	Gate-Drain Charge			1.2		nC

**Drain-Source Diode Characteristics and Maximum Ratings**

$I_S$	Maximum Continuous Drain-Source Diode Forward Current			0.42		A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 0.42\text{ A}$ (Note 2)		0.72	1.2	V

**Notes:**

1:  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.



a)  $250^\circ\text{C/W}$  when mounted on a  $0.02\text{ in}^2$  Pad of 2 oz. Cu.



b)  $270^\circ\text{C/W}$  when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2: Pulse Test: Pulse Width  $\leq 300\text{ }\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$

## Typical Characteristics

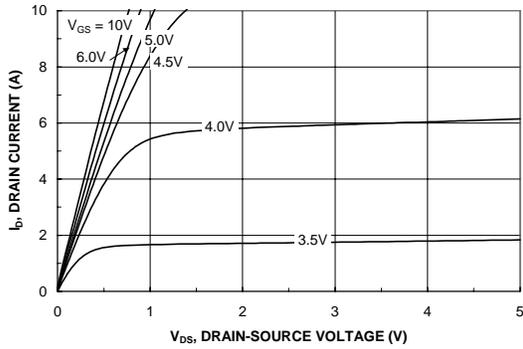


Figure 1. On-Region Characteristics.

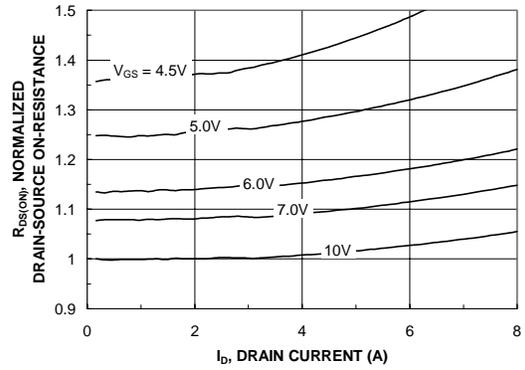


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

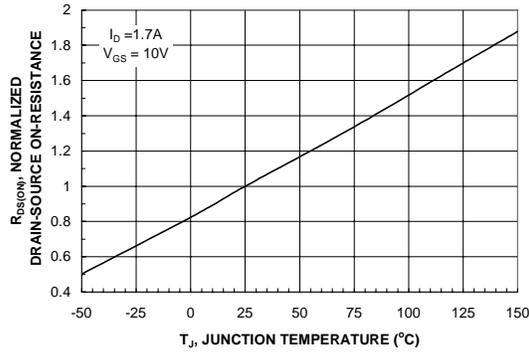


Figure 3. On-Resistance Variation with Temperature.

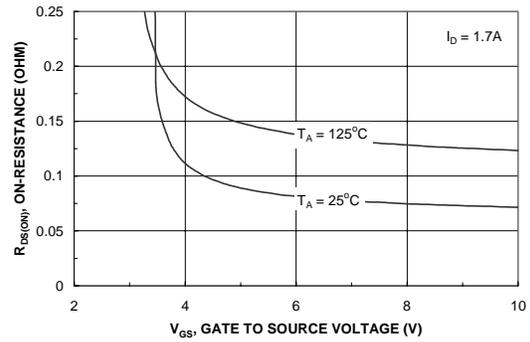


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

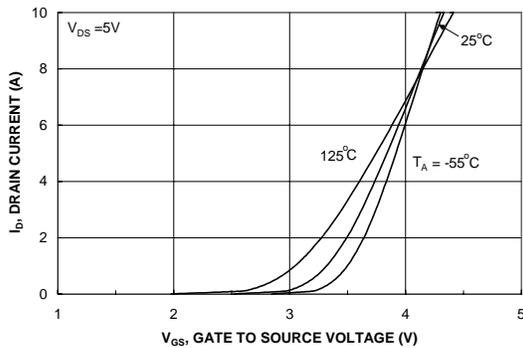


Figure 5. Transfer Characteristics.

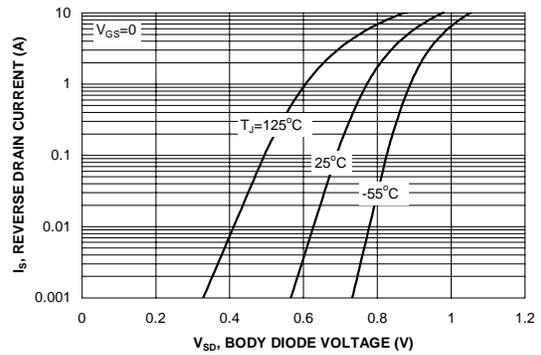
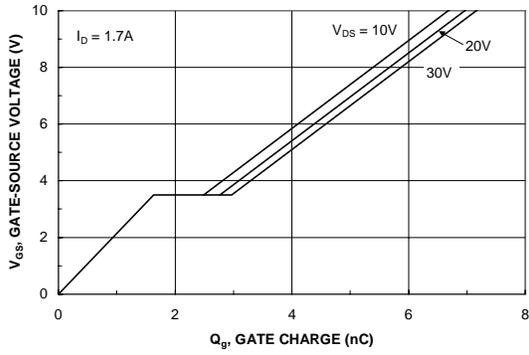
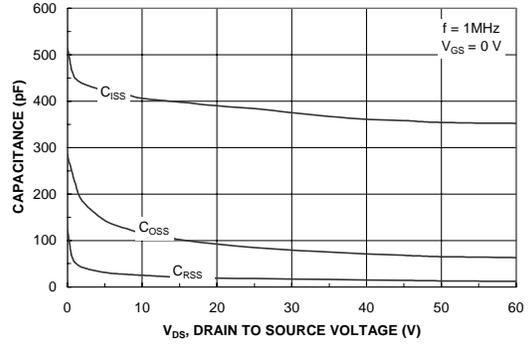


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

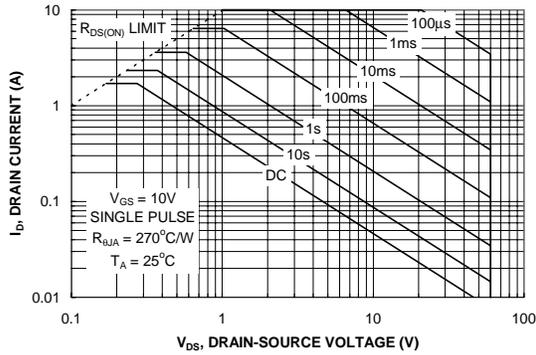
**Typical Characteristics** (continued)



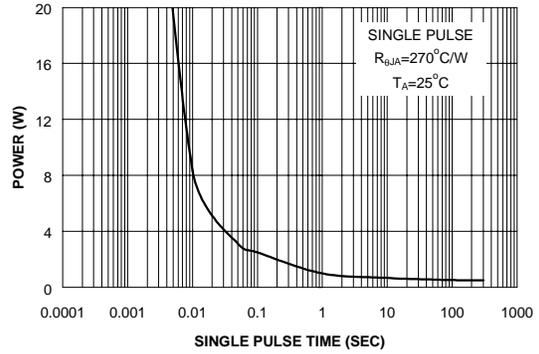
**Figure 7. Gate Charge Characteristics.**



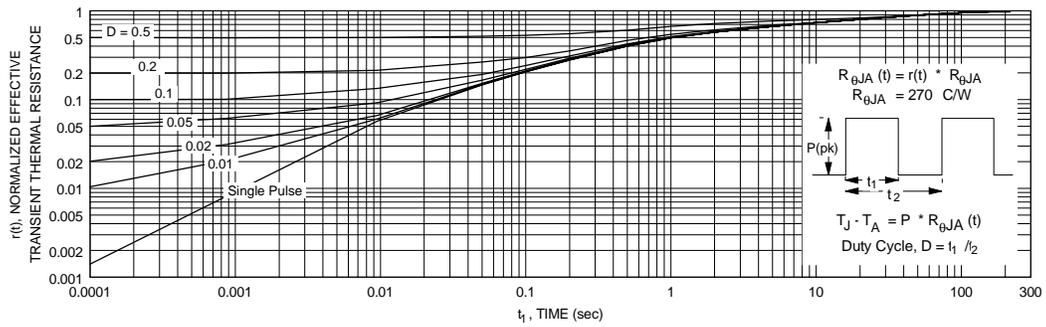
**Figure 8. Capacitance Characteristics.**



**Figure 9. Maximum Safe Operating Area.**

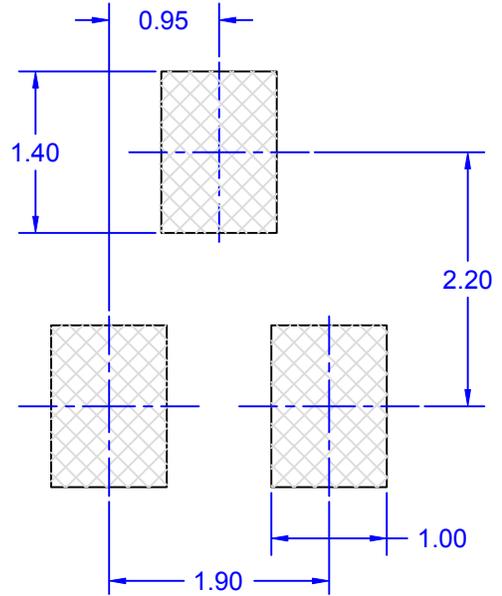
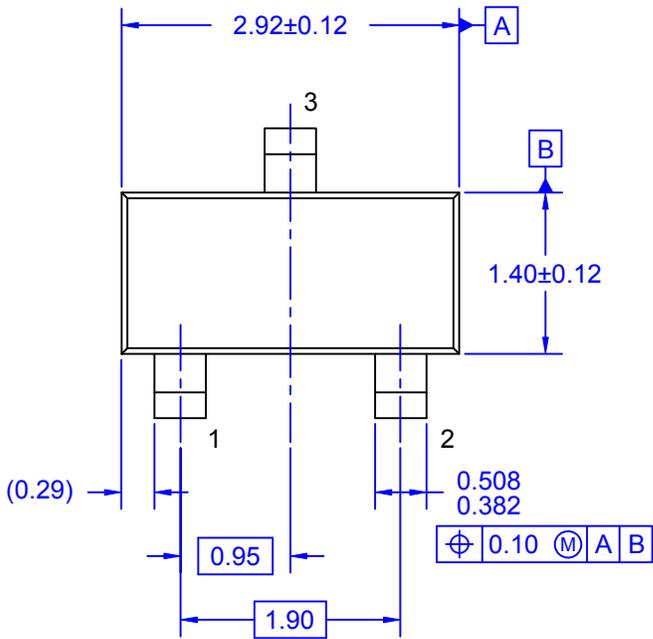


**Figure 10. Single Pulse Maximum Power Dissipation.**

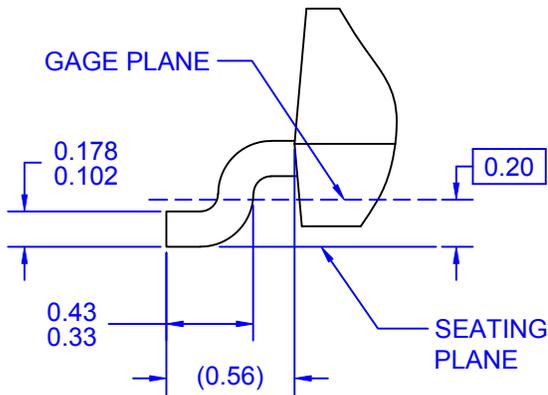
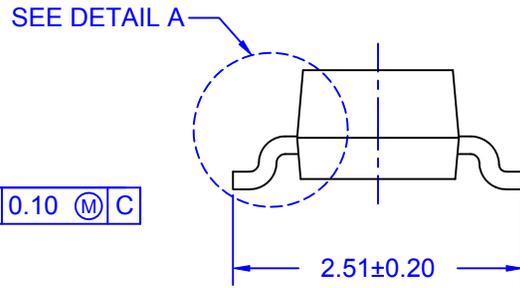
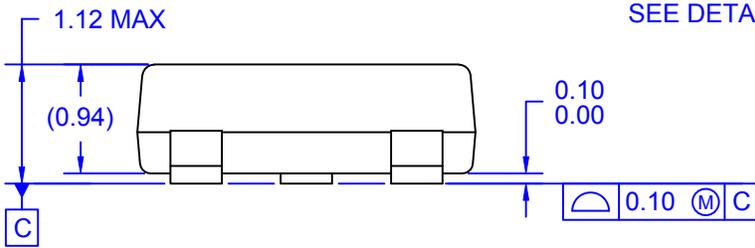


**Figure 11. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.



LAND PATTERN RECOMMENDATION



**DETAIL A**  
 SCALE: 50:1

NOTES: UNLESS OTHERWISE SPECIFIED

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- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 2009.
- E) DRAWING FILE NAME: MKT-MA03BREV3





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