DRV110 Power-Saving Solenoid Controller With Integrated Supply Regulation

1 Features

- Drives an External MOSFET With PWM to Control Solenoid Current
  - External Sense Resistor for Regulating Solenoid Current
- Fast Ramp-Up of Solenoid Current to Guarantee Activation
- Solenoid Current is Reduced in Hold Mode for Lower Power and Thermal Dissipation
- Ramp Peak Current, Keep Time at Peak Current, Hold Current, and PWM Clock Frequency Can Be Set Externally. They Can Also Be Operated at Nominal Values Without External Components.
- Internal Supply Voltage Regulation
  - 15-V Nominal MOSFET Gate Drive Voltage
  - External Pullup Resistor to Solenoid Supply Voltage
- Protection
  - Thermal Shutdown
  - Undervoltage Lockout (UVLO)
  - Maximum Ramp Time
  - Optional STATUS Output
- Operating Temperature Range: –40ºC to 105 ºC
- 8-Pin and 14-Pin TSSOP Package Options

2 Applications

- Electromechanical Drivers: Solenoids, Valves, Relays
- White Goods, Solar, Transportation

3 Description

The DRV110 device is a PWM current controller for solenoids. The device is designed to regulate the current with a well-controlled waveform to reduce power dissipation. The solenoid current is ramped up fast to ensure opening of the valve or relay. After initial ramping, the solenoid current is kept at peak value to ensure the correct operation, after which it is reduced to a lower hold level in order to avoid thermal problems and reduce power dissipation.

The peak current duration is set with an external capacitor. The current ramp peak and hold levels, as well as PWM frequency can independently be set with external resistors. External setting resistors can also be omitted, if the default values for the corresponding parameters are suitable for the application.

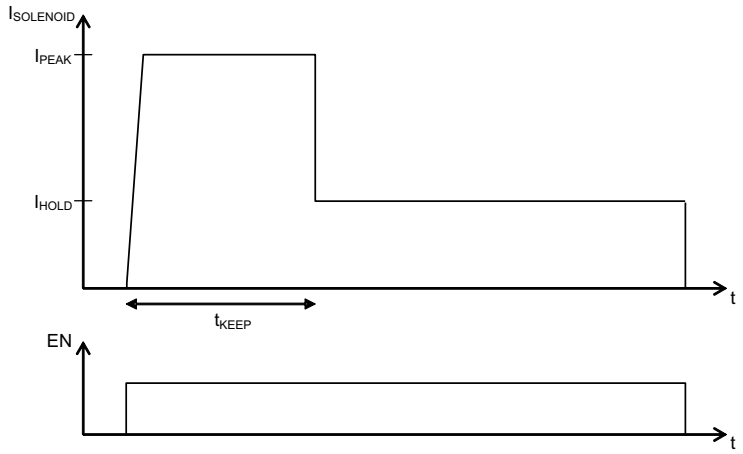
The DRV110 limits its own supply at VIN to 15 V and uses the same voltage level for the gate drive voltage of the external switching device. Typical application uses a MOSFET to drive the solenoid load.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV110	TSSOP (14)	5.00 mm × 4.40 mm
	TSSOP (8)	3.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

$I_{SOLENOID}$ vs Time



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4 Revision History

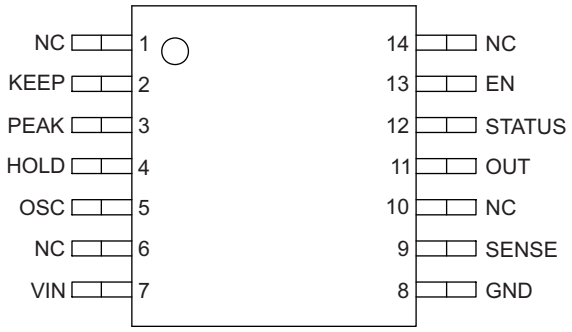
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2013) to Revision B	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

PW Package
8-Pin TSSOP
Top View

PW Package
14-Pin TSSOP
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	8-PIN PW[1]	14-PIN PW		
EN	8	13	I	Enable
GND	5	8	—	Ground
HOLD	—	4	I	Hold current set
KEEP	1	2	I	Keep time set
NC	—	1, 6, 10, 14	—	No connect
OSC	3	5	I	PWM frequency set
OUT	7	11	O	Solenoid switch gate drive
PEAK	2	3	I	Peak current set
SENSE	6	9	I	Solenoid current sense
STATUS	—	12	O	Open drain fault indicator
VIN	4	7	I	6-V to 18-V supply

(1) In the 8-pin package, the HOLD pin is not bonded out. For this package, the HOLD mode is configured to default (internal) settings.

6 Specifications

6.1 Absolute Maximum Ratings(1)(2)

		MIN	MAX	UNIT
VIN	Input voltage	–0.3	20	V
	Voltage on EN, STATUS, PEAK, HOLD, OSC, SENSE, KEEP	–0.3	7	V
	Voltage on OUT	–0.3	20	V
T_J	Operating virtual junction temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
I_Q	Supply current	1	1.5	3	mA
V_{IN}	Device will start sinking current when V_{IN} > 15 V to limit V_{IN}	6	15		V
C_{IN}	Input capacitor between VIN and GND (1)	1	4.7		µF
L	Solenoid inductance		1		H
T_A	Operating ambient temperature	–40		105	°C

(1) 4.7-µF input capacitor and full wave rectified 230-Vrms AC supply results in approximately 500-mV supply ripple.

6.4 Thermal Information

THERMAL METRIC		DRV110 PW [TSSOP] 8 PINS	DRV110 PW [TSSOP] 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	183.8	122.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance(2)	69.2	51.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance(3)	112.6	64.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter(4)	10.4	6.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter(5)	110.9	63.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance(6)	N/A	N/A	°C/W

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

6.5 Electrical Characteristics

V_{IN} = 14 V, T_A = –40°C to 105°C, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Standby current	EN = 0, V_{IN} = 14 V, bypass deactivated		200	250	µA
	Quiescent current	EN = 1, V_{IN} = 14 V, bypass deactivated		360	570	
	Internally regulated supply	EN = 0, I_{VIN} = 2 mA, bypass activated	10.5	15	19	V
		EN = 1, I_{VIN} = 2 mA, bypass activated	14.5	15	15.5	
GATE DRIVER						
V_{DRV}	Gate drive voltage	Supply voltage in regulation (I_{VIN} > 1 mA)		V_{IN}		V
I_{DRV_SINK}	Gate drive sink current	V_{OUT} = 15 V; V_{IN} = 15 V	8	15		mA
I_{DRV_SOURCE}	Gate drive source current	V_{OUT} = GND; V_{IN} = 15 V		–15	–10	mA
f_{PWM}	PWM clock frequency	OSC = GND	15	20	27	kHz
D_{MAX}	Maximum PWM duty cycle			100%		
D_{MIN}	Minimum PWM duty cycle			7.5%		
t_D	Start-up delay	Delay between EN going high until gate driver starts switching, f_{PWM} = 20 kHz			50	µs
CURRENT CONTROLLER, INTERNAL SETTINGS						
I_{PEAK}	Peak current	R_{SENSE} = 1 Ω, PEAK = GND	270	300	330	mA
I_{HOLD}	Hold current	R_{SENSE} = 1 Ω, HOLD = GND	40	50	65	mA
CURRENT CONTROLLER, EXTERNAL SETTINGS						
t_{KEEP}	Externally set keep time at peak current	C_{KEEP} = 1 µF		100		ms
V_{PEAK}	Externally set V_{PEAK}	R_{PEAK} = 50 kΩ		900		mV
		R_{PEAK} = 200 kΩ		300		
V_{HOLD}	Externally set V_{HOLD}	R_{HOLD} = 50 kΩ		150		mV
		R_{HOLD} = 200 kΩ		50		
f_{PWM}	Externally set PWM clock frequency	R_{OSC} = 50 kΩ		60		kHz
		R_{OSC} = 200 kΩ		20		
LOGIC INPUT LEVELS (EN)						
V_{IL}	Input low level				1.3	V
V_{IH}	Input high level		1.65			V
R_{EN}	Input pullup resistance		350	500		kΩ
LOGIC OUTPUT LEVELS (STATUS)						
V_{OL}	Output low level	Pulldown activated, I_{STATUS} = 2 mA			0.3	V
I_{IL}	Output leakage current	Pulldown deactivated, V(STATUS) = 5 V			2	µA
UNDERVOLTAGE LOCKOUT						
V_{UVLO}	Undervoltage lockout threshold			4.6		V
THERMAL SHUTDOWN						
T_{TSU}	Junction temperature start-up threshold			140		°C
T_{TSD}	Junction temperature shutdown threshold			160		°C

6.6 Typical Characteristics

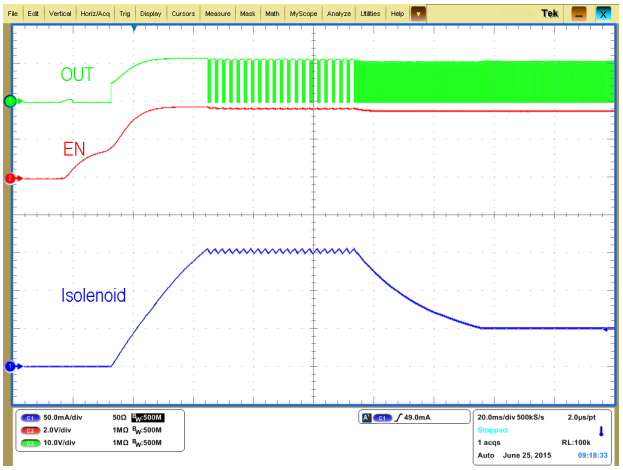


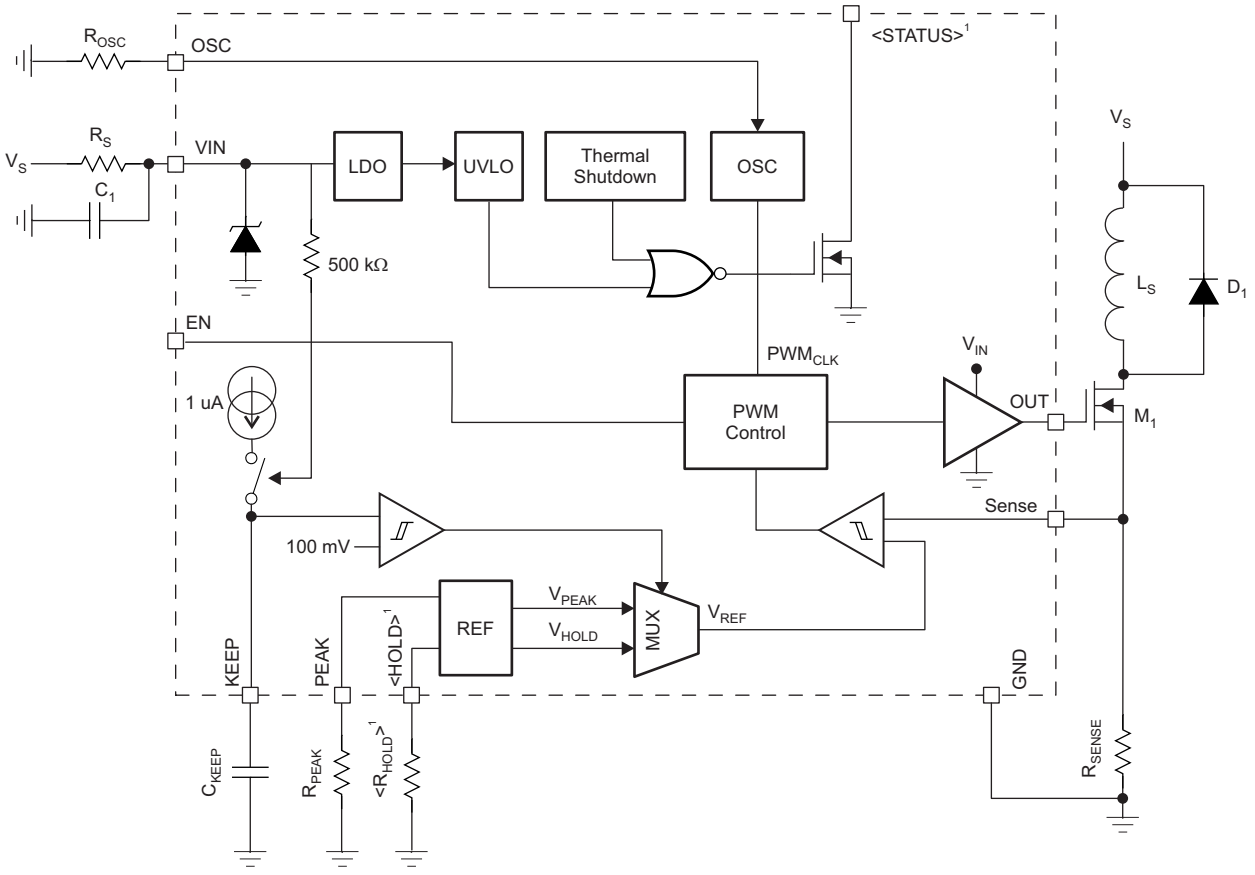
Figure 1. Solenoid Current, EN, and PWM vs Time

7 Detailed Description

7.1 Overview

The DRV110 device provides a PWM current controller for use with solenoids. The device provides a quick ramp to a high peak current value in order to ensure opening of the valve or relay. The peak current is held for a programmable time and then released to a lower value to maintain the open state of the valve or relay while reducing the total current consumption. Peak current duration, peak current amount, hold current amount (in the 14-pin package), and PWM frequency can all be controlled by external components or used at default levels by omitting these components (except peak current duration). Enable and disable of the switch is controlled by the EN pin. The DRV110 also features a wide VIN range with an internal bypass regulator to maintain VIN at an acceptable level. Finally, the 14-pin package features an open-drain pull-down path on the STATUS pin which is enabled as long as undervoltage lockout or thermal shutdown has not triggered.

7.2 Functional Block Diagram



[1]Available only in the 14-pin package

7.3 Feature Description

The DRV110 controls the current through the solenoid as shown in Figure 2. Activation starts when EN pin voltage is pulled high either by an external driver or internal pullup. In the beginning of activation, DRV110 allows the load current to ramp up to the peak value I_{PEAK} and it regulates it at the peak value for the time, t_{KEEP}, before reducing it to I_{HOLD}. The load current is regulated at the hold value as long as the EN pin is kept high. The initial current ramp-up time depends on the inductance and resistance of the solenoid. Once EN pin is driven to GND, DRV110 allows the solenoid current to decay to zero.

Feature Description (continued)

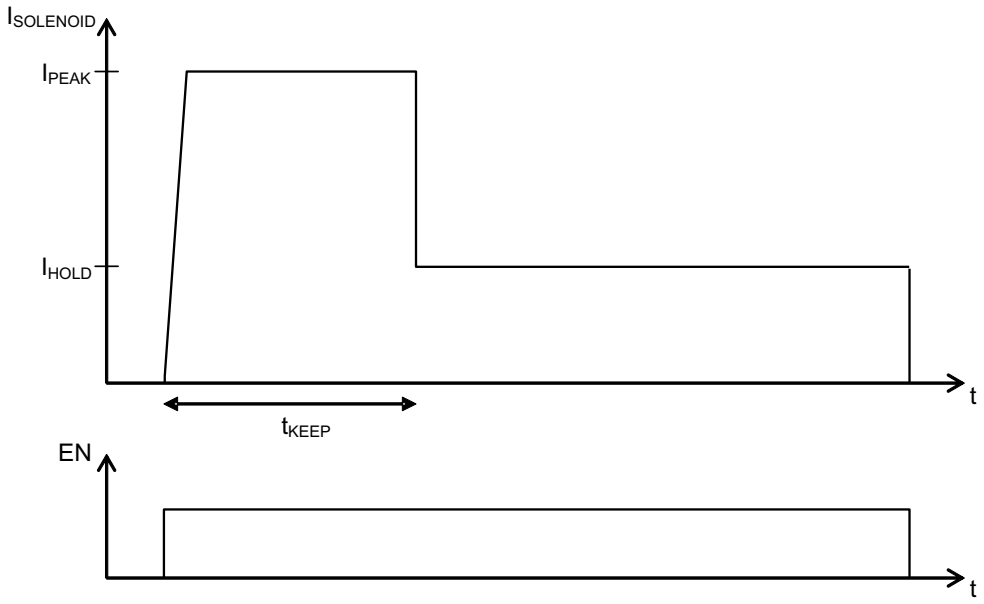


Figure 2. Typical Current Waveform Through the Solenoid

t_{KEEP} is set externally by connecting a capacitor to the KEEP pin. A constant current is sourced from the KEEP pin that is driven into an external capacitor resulting in a linear voltage ramp. When the KEEP pin voltage reaches 100 mV, the current regulation reference voltage, V_{REF}, is switched from V_{PEAK} to V_{HOLD}. Dependency of t_{KEEP} from the external capacitor size can be calculated by:

$$t_{KEEP}\left[s\right] = C_{KEEP}\left[F\right] \cdot 10^5 \left[\frac{s}{F}\right] \quad (1)$$

The current control loop regulates, cycle-by-cycle, the solenoid current by sensing voltage at the SENSE pin and controlling the external switching device gate through the OUT pin. During the ON-cycle, the OUT pin voltage is driven and kept high (equal to VIN voltage) allowing current to flow through the external switch as long as the voltage at the SENSE pin is less than V_{REF}. As soon as the voltage at the SENSE pin is above V_{REF}, the OUT pin voltage is immediately driven and kept low until the next ON-cycle is triggered by the internal PWM clock signal. In the beginning of each ON-cycle, the OUT pin voltage is driven and kept high for at least the time determined by the minimum PWM signal duty cycle, D_{MIN}.

V_{PEAK} and V_{HOLD} depend on fixed resistance values R_{PEAK} and R_{HOLD} approximately as shown in Figure 3. If the PEAK pin is connected to ground, the peak current reference voltage, V_{PEAK}, is at its default value (internal setting). The V_{PEAK} value can alternatively be set by connecting an external resistor to ground from the PEAK pin. For example, if a 50-kΩ (= R_{PEAK}) resistor is connected between PEAK and GND, and R_{SENSE} = 1 Ω, then the externally set I_{PEAK} level will be 900 mA. If R_{PEAK} = 200 kΩ and R_{SENSE} = 1 Ω, then the externally set I_{PEAK} level will be 300 mA. In case R_{SENSE} = 2 Ω instead of 1 Ω, then I_{PEAK} = 450 mA (when R_{PEAK} = 50 kΩ) and I_{PEAK} = 150 mA (when R_{PEAK} = 200 kΩ). In the 8-pin package, the HOLD reference uses the internal V_{REF} setting of 50 mV. In the 14-pin package, external setting of the HOLD current, I_{HOLD}, works in the way as the external setting for I_{PEAK} but the current levels are 1/6 of the I_{PEAK} levels. External settings for I_{PEAK} and I_{HOLD} are independent of each other. If R_{PEAK} or R_{HOLD} is decreased below 33.33 kΩ (typical value), then the reference is clamped to the internal setting of 300 mV for PEAK and 50 mV for HOLD. Approximate I_{PEAK} and I_{HOLD} values can be calculated by using the formula below.

$$I_{PEAK} = \frac{V_{REF}}{R_{SENSE}} = \frac{1\,\Omega \times 900\ mA \times 66.67\ k\Omega}{R_{PEAK}} \times \frac{1}{R_{SENSE}};\ 66.67\ k\Omega < R_{PEAK} < 2\ M\Omega \quad (2)$$

$$I_{HOLD} = \frac{V_{REF}}{R_{SENSE}} = \frac{1\,\Omega \times 150\ mA \times 66.67\ k\Omega}{R_{HOLD}} \times \frac{1}{R_{SENSE}};\ 66.67\ k\Omega < R_{HOLD} < 2\ M\Omega \quad (3)$$

Feature Description (continued)

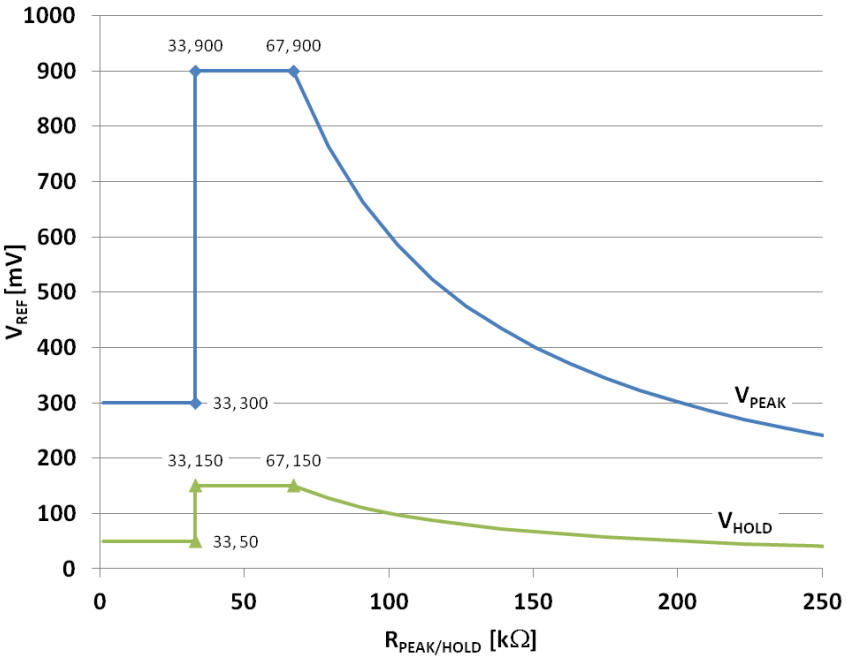


Figure 3. PEAK and HOLD Mode V_{REF} Settings

Frequency of the internal PWM clock signal, PWM_{CLK}, that triggers each OUT pin ON-cycle can be adjusted by external resistor, R_{OSC}, connected between OSC and GND. Frequency as a function of resistor value is shown in Figure 4. Default frequency is used when OSC is connected to GND directly. PWM frequency as a function of external fixed adjustment resistor value (greater than 66.67 kΩ) is given below.

$$f_{PWM} = \frac{60kHz}{R_{OSC}} \cdot 66.67k\Omega; 66.67k\Omega < R_{OSC} < 2M\Omega \quad (4)$$

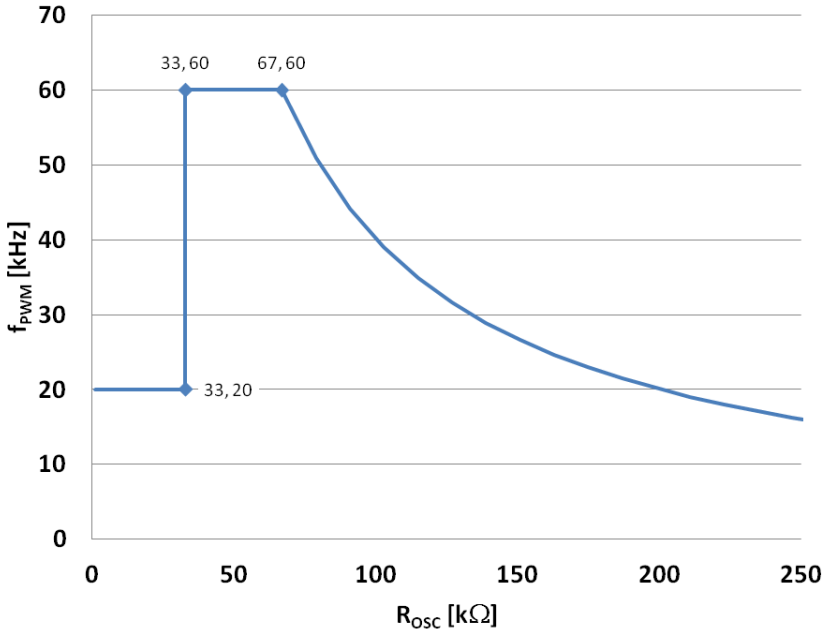


Figure 4. PWM Clock Frequency Setting

Feature Description (continued)

Voltage at the OUT pin, that is the gate voltage of an external switching device, is equal to VIN voltage during ON-cycle. The voltage is driven to ground during OFF-cycle. VIN voltages below 15 V can be supplied directly from an external voltage source. Supply voltages of at least 6 V are supported.

The DRV110 is able to regulate VIN voltage to 15 V from a higher external supply voltage, V_S, by an internal bypass regulator that replicates the function of an ideal Zener diode. This requires that the supply current is sufficiently limited by an external resistor between V_S and the VIN pin. An external capacitor connected to the VIN pin is used to store enough energy to charge the external switch gate capacitance at the OUT pin. Current limiting resistor size to keep quiescent current less than 1 mA can be calculated by Equation 5.

$$R_S = \frac{V_{S,maxDC} - 15V}{1mA + I_{Gate,AVE}} \quad (5)$$

Open-drain pulldown path at the STATUS pin is deactivated if either undervoltage lockout or thermal shutdown blocks have triggered.

7.4 Device Functional Modes

The DRV110 transitions through three different states. The first is the OFF state, where the EN pin is low and the PWM output is off. The second is the PEAK state, which begins when the EN pin is set high, and ends once t_{KEEP}has been reached. During this state, the PWM operates in order to reach the I_{PEAK} set by the R_{PEAK}. Finally, once t_{KEEP} has been reached, the PWM continues to operate, but at the I_{HOLD} level. This continues until the EN pin is set low again and the PWM turns off.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV110 device is designed to operate a solenoid valve or relay. For detailed information on using the DRV110 with 230 V AC solenoids, see *Current Controlled Driver for 230V AC Solenoids Reference Design* (TIDU584). A typical DC input design will be outlined in *Typical Application*. Approximate resistor and capacitor values for the peak current, hold current, sense, and keep time will be derived for a sample application.

8.2 Typical Application

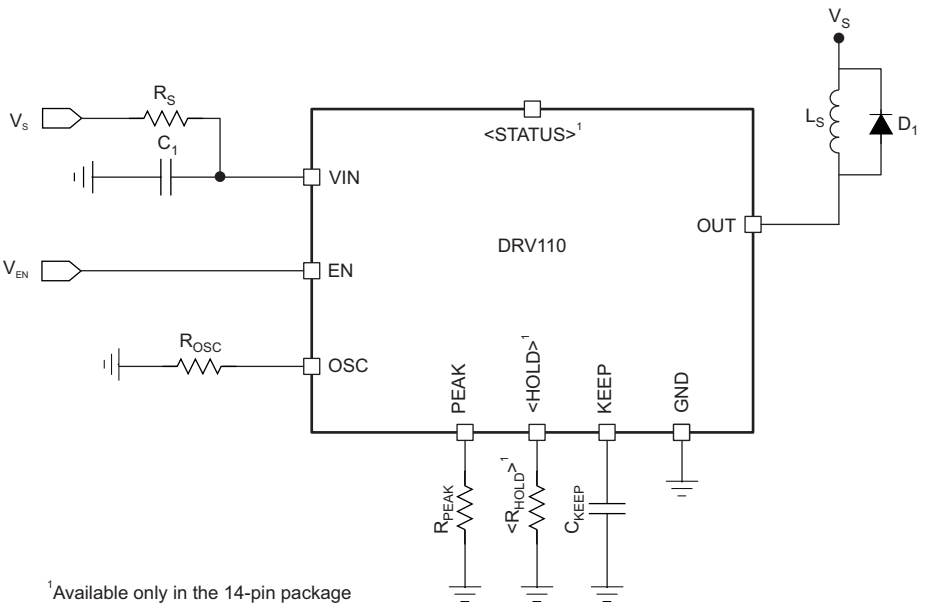


Figure 5. Default Configuration

8.2.1 Design Requirements

The key elements to identify here are the system input voltage, peak current, hold current, and peak keep time values required for the solenoid or relay being used. With these values, approximate R_S, R_{PEAK}, R_{HOLD} (for 14-pin package), C_{KEEP}, and R_{SENSE} values can be determined and the proper FET and diode can be identified. R_{OSC} can be varied in order to tune the circuit to the chosen solenoid or relay.

8.2.2 Detailed Design Procedure

First, the input voltage to the DRV110 must be considered. If this is from 6 V to 15 V, then no current-limit resistor is required and only the input capacitor is necessary. If V_{IN} exceeds 15V, then R_S must be calculated based on Equation 5 and included to prevent excess power loss and potential damage.

Next, with the known peak current, hold current, and peak keep time values, the R_{PEAK}, R_{HOLD} (for 14-pin package), C_{KEEP}, and R_{SENSE} values can be determined. Calculation will proceed based on example values shown in Table 1.

Table 1. Sample Application Values

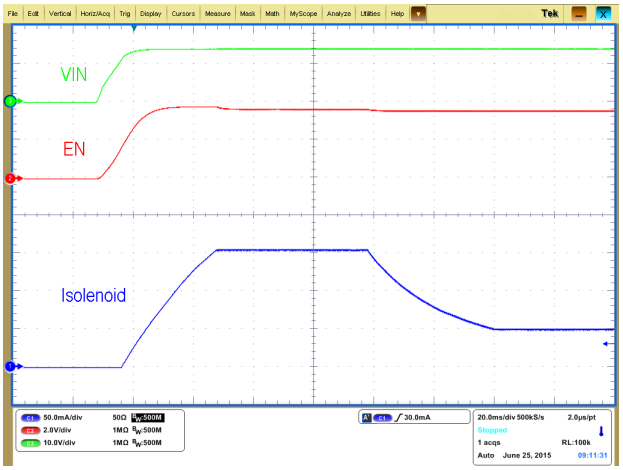
VARIABLE	VALUE
Peak current	150 mA
Hold current	50 mA
Keep time	100 ms

For I_{PEAK}, the V_{REF} range is 300 mV to 900 mV, so the I_{PEAK} range is defined by 300 mV / R_{SENSE} to 900 mV / R_{SENSE}. For I_{HOLD} with the 8-pin package, I_{HOLD} is set by 50 mV / R_{SENSE}. For I_{HOLD} with the 14-pin package, the V_{REF} range is 50 mV to 150 mV, so the I_{HOLD} range is defined by 50 mV / R_{SENSE} to 150 mV / R_{SENSE}. Based on these ranges, a suitable R_{SENSE} must be chosen. For the sample values, R_{SENSE} of 1 Ω works for both the 8-pin and 14-pin package. With R_{SENSE} chosen, R_{PEAK} and R_{HOLD} (if applicable) can be determined using Equation 2 and Equation 3. For the sample values, R_{PEAK} is set to 400 kΩ and R_{HOLD} can be shorted to GND. TI recommends that a 0-Ω resistor is used for prototyping in case changes to this value are desired.

Next, C_{KEEP} can be set based on Equation 1, 1 µF for the sample values. R_{OSC} can initially be shorted to GND, but again a 0-Ω resistor is recommended for prototyping. Additionally, a filter on the SENSE line may be added if it will be in a high noise environment and is recommended for prototyping. Typical values for this are 1 kΩ and 100 pF.

Finally, a FET and current recirculation diode must be chosen based on the current values defined in Table 1. The current recirculation diode should be a fast recovery diode.

8.2.3 Application Curves



R_{OSC} = 0 Ω R_{PEAK} = 303 kΩ R_{HOLD} = 0 Ω
R_{SENSE} = 1 Ω C_{KEEP} = 1 µF L_{ind} = 1 H
R_{ind} = 50 Ω Measured on the EVM

Figure 6. $I_{SOLENOID}$, EN, and V_{IN} vs Time

9 Power Supply Recommendations

The input supply range must be at least 6 V, and needs a current-limiting resistor above 15 V. An input capacitor of 4.7 µF (typical) is required as well. I_Q max is 3 mA, but additional current will be required to operate the solenoid or relay.

10 Layout

10.1 Layout Guidelines

Routing for the SENSE pin should be careful to avoid noise sources. Routing for the output node and sense node should be minimized. The trace for the solenoid or relay current should be wide in order to prevent any unexpected voltage drop.

10.2 Layout Example

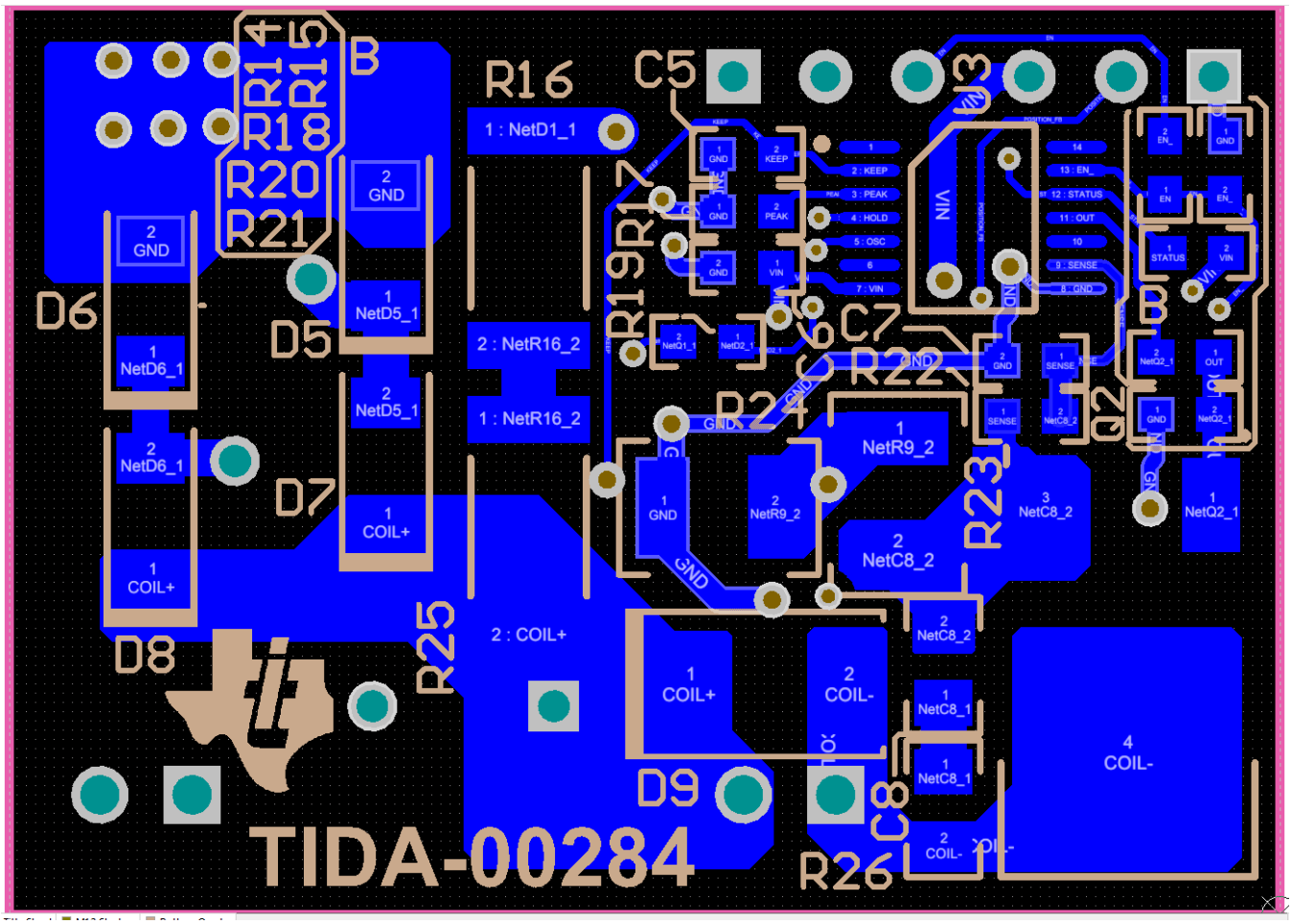


Figure 7. Layout Schematic

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- *Current Controlled Driver for 230V AC Solenoids Reference Design*, TIDU584

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV110APWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to +105	110A	Samples
DRV110PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to +105	110	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

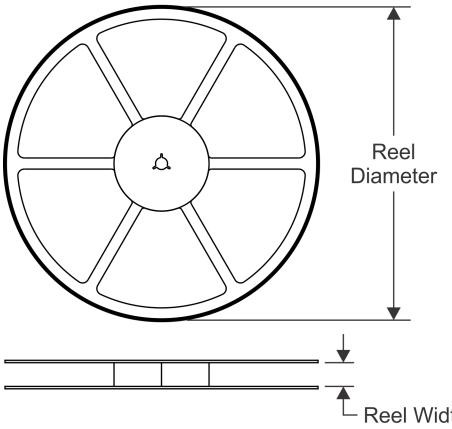
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

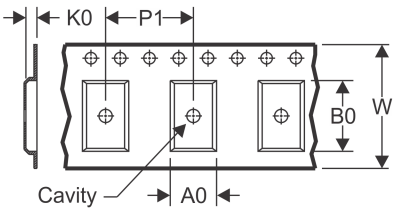
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

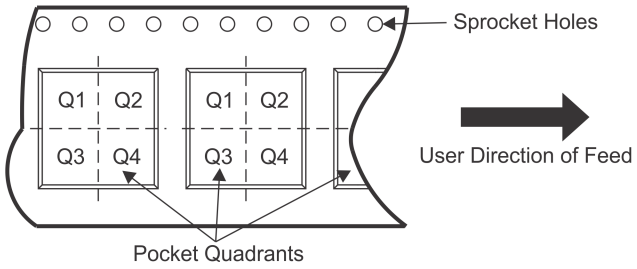


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

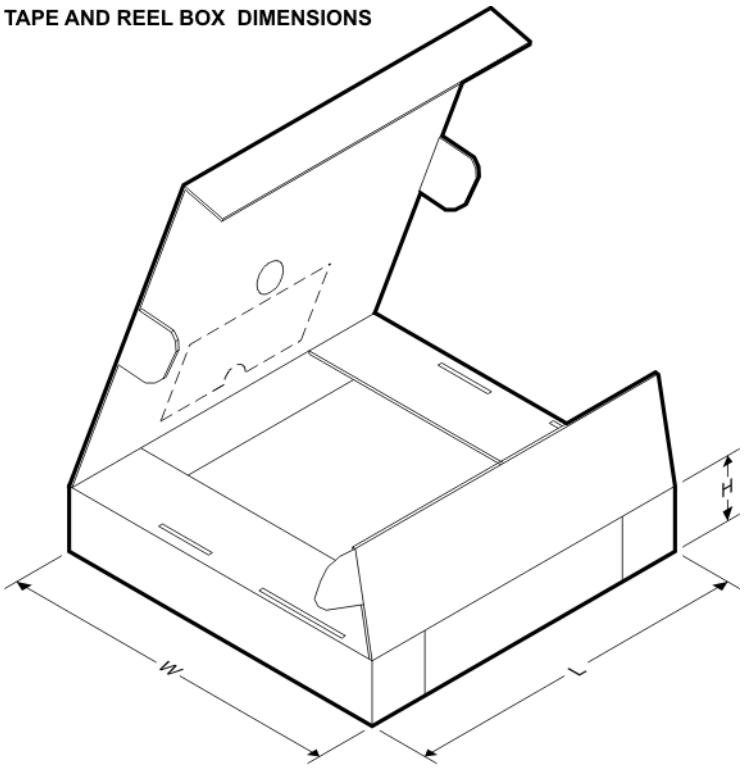
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV110APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DRV110PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

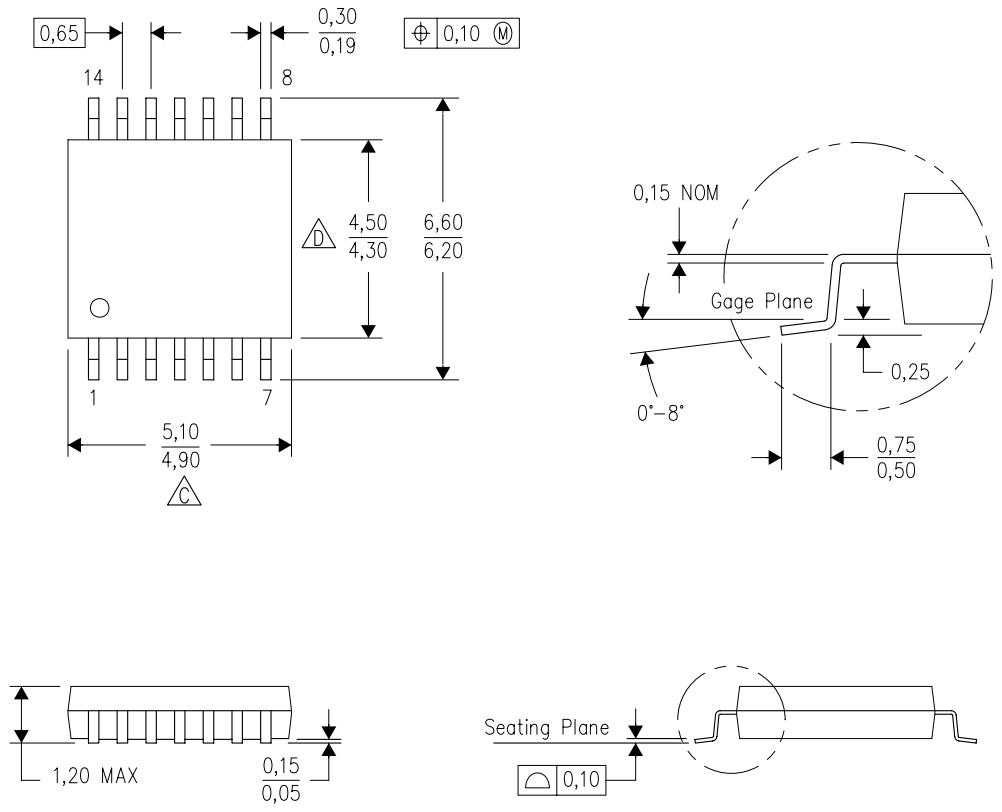
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV110APWR	TSSOP	PW	14	2000	367.0	367.0	35.0
DRV110PWR	TSSOP	PW	8	2000	367.0	367.0	35.0

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



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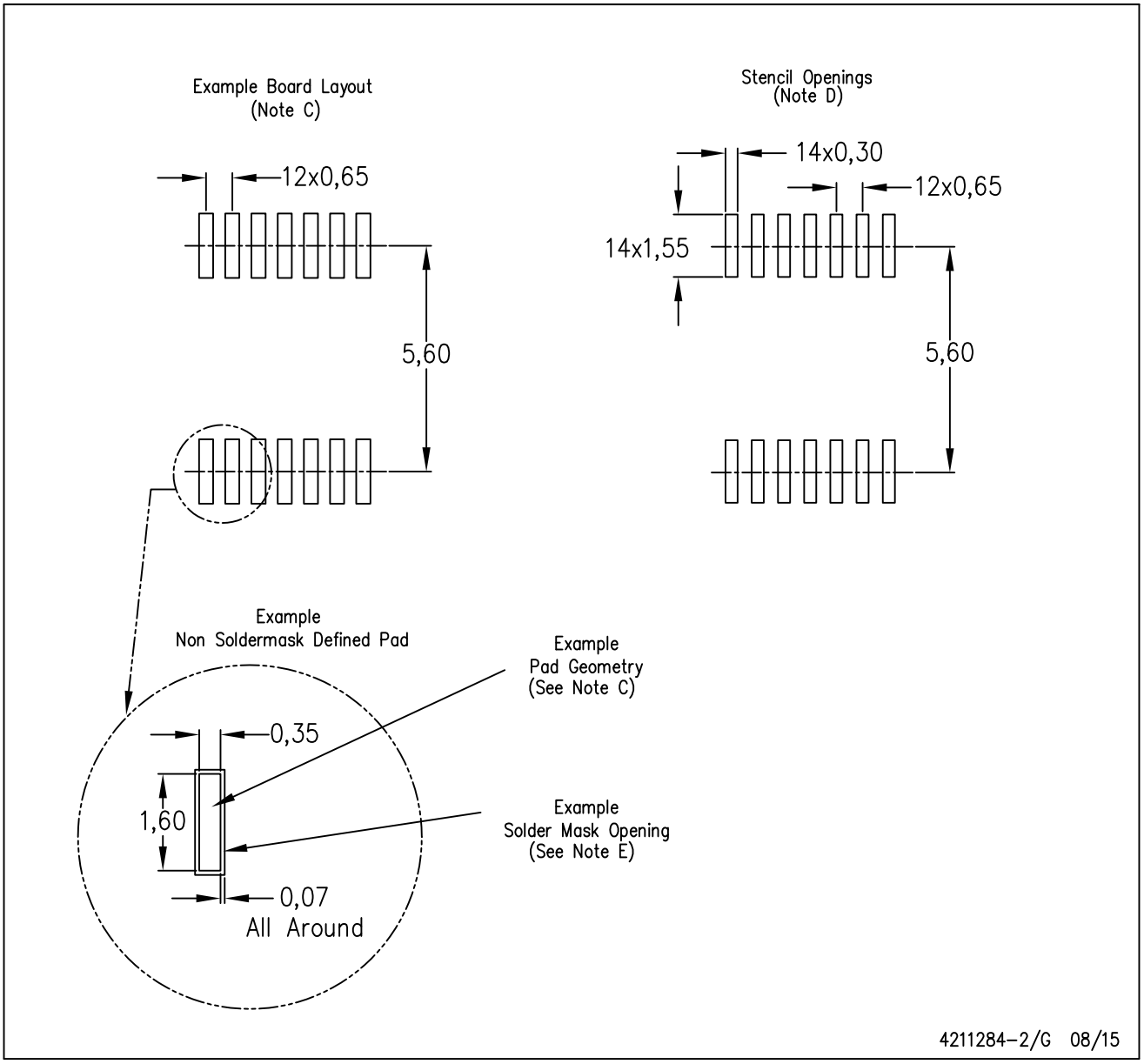
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



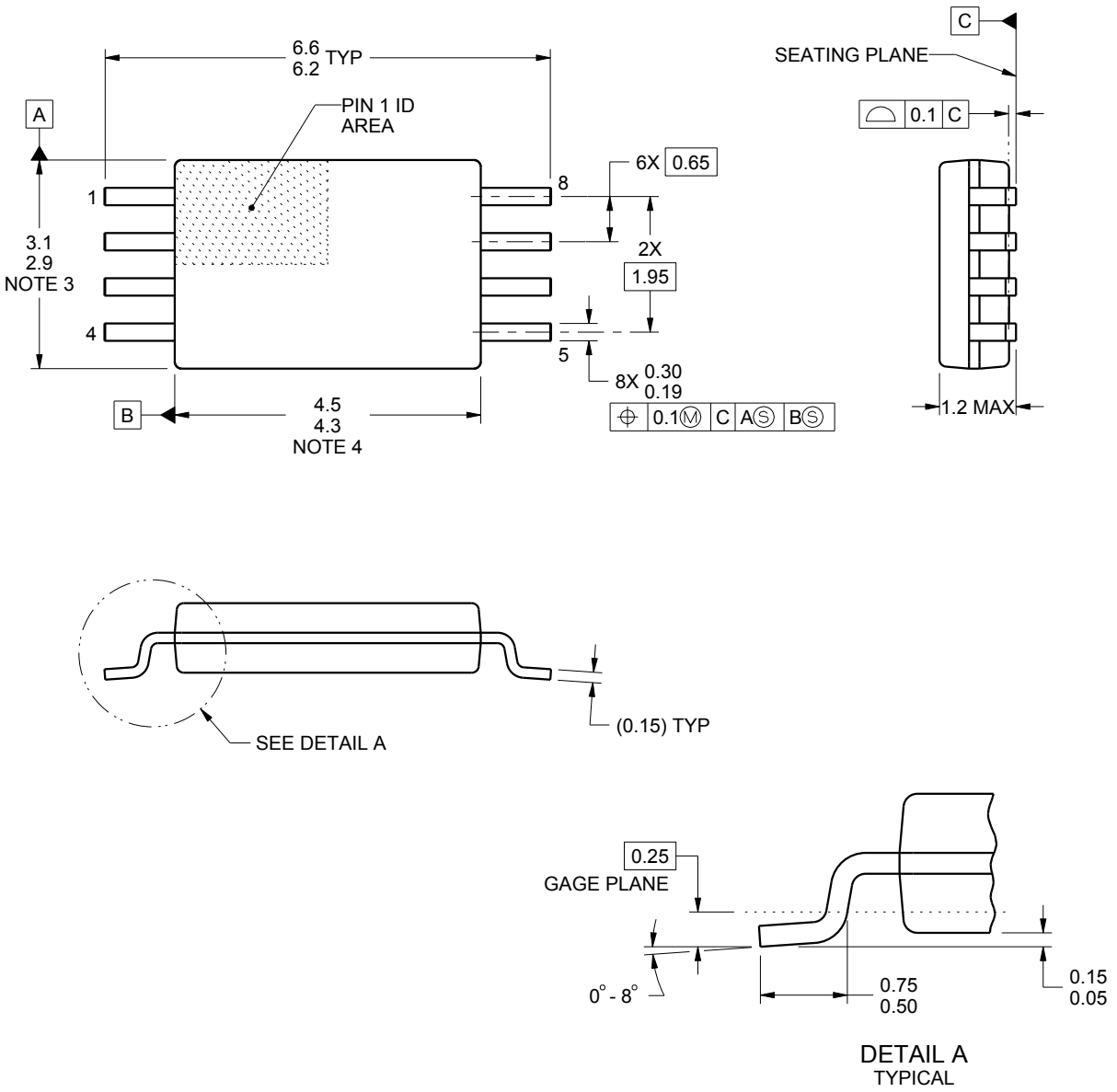
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0008A

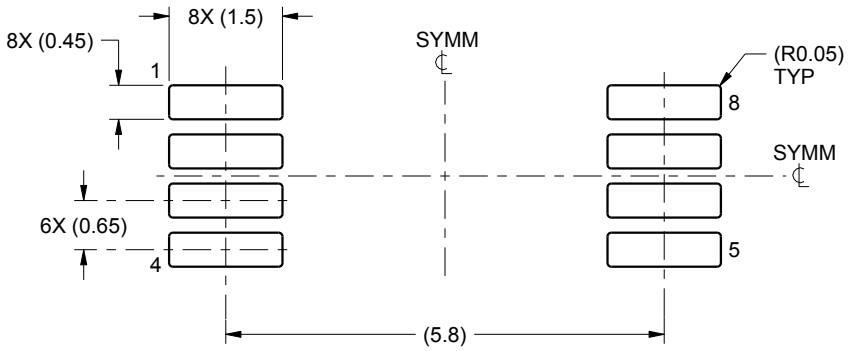
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

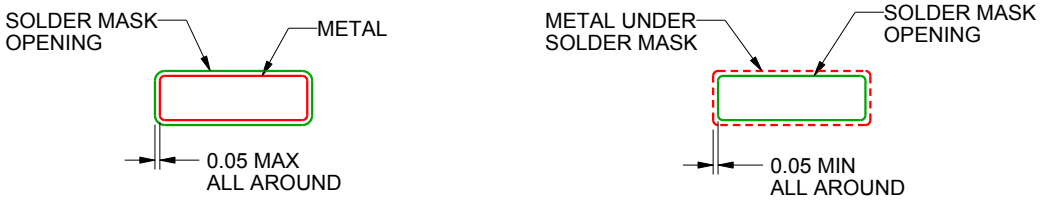


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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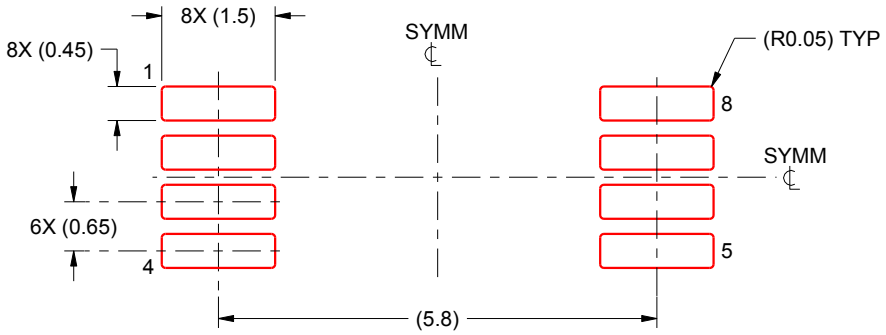
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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