

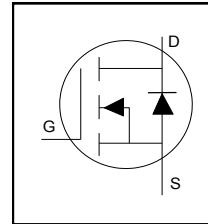
**Application**

- Optimized for UPS/Inverter Applications
- Low Voltage Power Tools

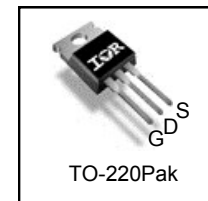
**Benefits**

- Best in Class Performance for UPS/Inverter Applications
- Very Low RDS(on) at 4.5V VGS
- Ultra-Low Gate Impedance
- Fully Characterized Avalanche Voltage and Current
- Lead-Free, RoHS Compliant

HEXFET® Power MOSFET



<b>V<sub>DSS</sub></b>	<b>30</b>	<b>V</b>
<b>R<sub>DS(on)</sub> max</b> (@ V <sub>GS</sub> = 10V)	<b>2.4</b>	<b>mΩ</b>
(@ V <sub>GS</sub> = 4.5V)	<b>3.2</b>	
<b>Q<sub>g</sub> (typical)</b>	<b>40</b>	<b>nC</b>
<b>I<sub>D</sub> (Silicon Limited)</b>	<b>171</b> Ⓞ	<b>A</b>
<b>I<sub>D</sub> (Package Limited)</b>	<b>130A</b>	



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRLB8314PbF	TO-220Pak	Tube	50	IRLB8314PbF

**Absolute Maximum Rating**

Symbol	Parameter	Max.	Units
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	V
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited)	171Ⓞ	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited)	120	
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Package Limited)	130	
I <sub>DM</sub>	Pulsed Drain Current ①	664	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Maximum Power Dissipation	125	W
P <sub>D</sub> @ T <sub>C</sub> = 100°C	Maximum Power Dissipation	63	W
	Linear Derating Factor	0.83	W/°C
T <sub>J</sub>	Operating Junction and	-55 to + 175	°C
T <sub>STG</sub>	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)		
	Mounting Torque, 6-32 or M3 Screw	10 lbf·in (1.1 N·m)	

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case ④	—	1.2	°C/W
R <sub>θCS</sub>	Case-to-Sink, Flat Greased Surface	0.50	—	
R <sub>θJA</sub>	Junction-to-Ambient	—	62	

Notes ① through ④ are on page 8

**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

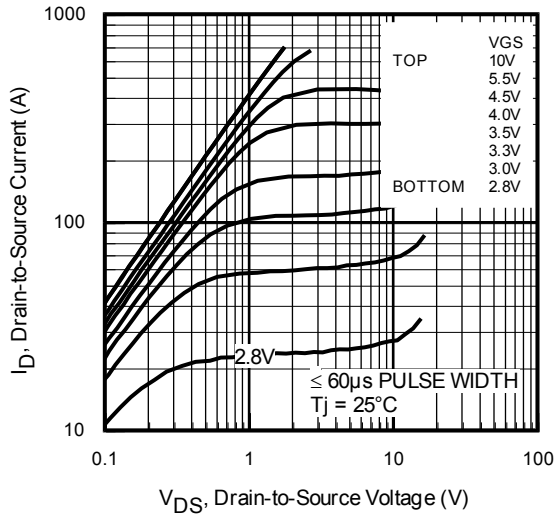
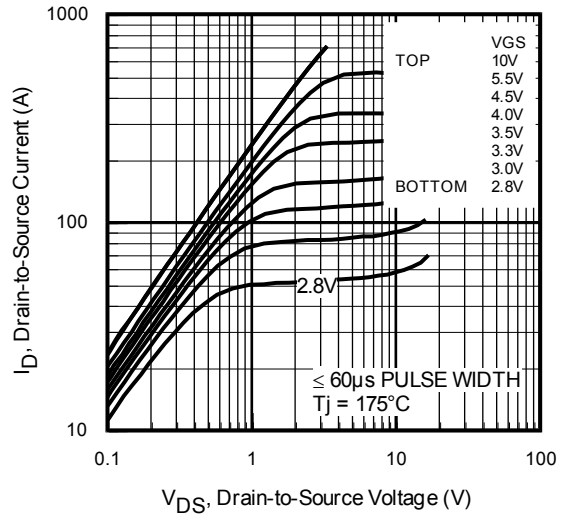
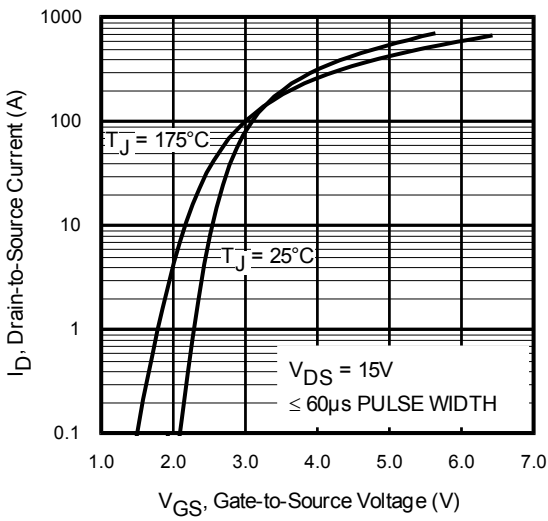
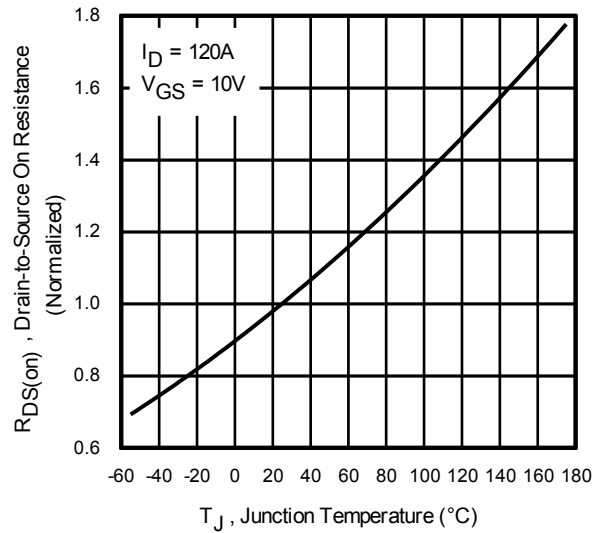
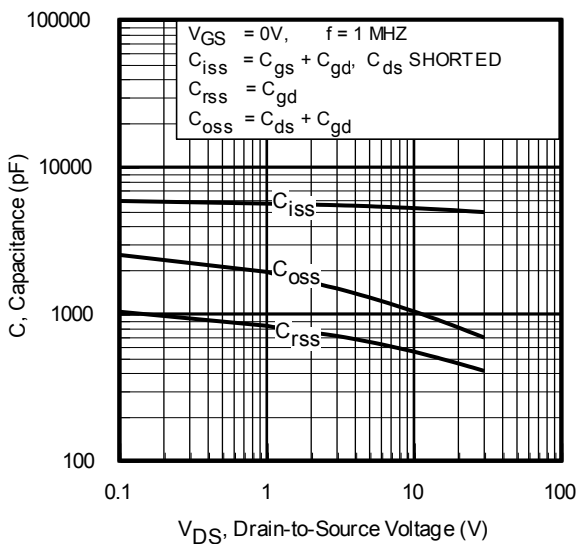
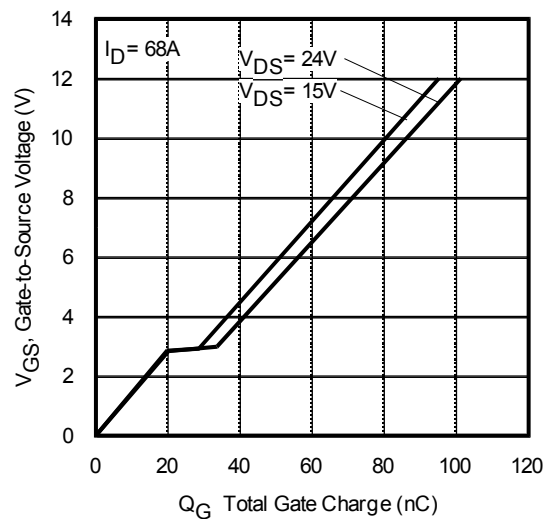
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	30	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	14	—	mV/°C	Reference to 25°C, I <sub>D</sub> = 1mA ①
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	1.9	2.4	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 68A ③
		—	2.6	3.2		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 68A ③
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.2	1.7	2.2	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 100μA
ΔV <sub>GS(th)</sub> /ΔT <sub>J</sub>	Gate Threshold Voltage Coefficient	—	-7.0	—	mV/°C	
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	1.0	μA	V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V
		—	—	150		V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V
g <sub>fs</sub>	Forward Transconductance	307	—	—	S	V <sub>DS</sub> = 15V, I <sub>D</sub> = 68A
Q <sub>g</sub>	Total Gate Charge	—	40	60	nC	V <sub>DS</sub> = 15V V <sub>GS</sub> = 4.5V I <sub>D</sub> = 68A
Q <sub>gs1</sub>	Pre-V <sub>th</sub> Gate-to-Source Charge	—	6.8	—		
Q <sub>gs2</sub>	Post-V <sub>th</sub> Gate-to-Source Charge	—	13	—		
Q <sub>gd</sub>	Gate-to-Drain Charge	—	8.7	—		
Q <sub>godr</sub>	Gate Charge Overdrive	—	11.5	—		
Q <sub>sw</sub>	Switch Charge (Q <sub>gs2</sub> + Q <sub>gd</sub> )	—	21.7	—		
R <sub>G</sub>	Gate Resistance	—	1.7	—	Ω	
t <sub>d(on)</sub>	Turn-On Delay Time	—	19	—	ns	V <sub>DD</sub> = 15V I <sub>D</sub> = 68A R <sub>G</sub> = 1.8Ω V <sub>GS</sub> = 4.5V ③
t <sub>r</sub>	Rise Time	—	142	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	32	—		
t <sub>f</sub>	Fall Time	—	72	—		
C <sub>iss</sub>	Input Capacitance	—	5050	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 15V f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	890	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	500	—		

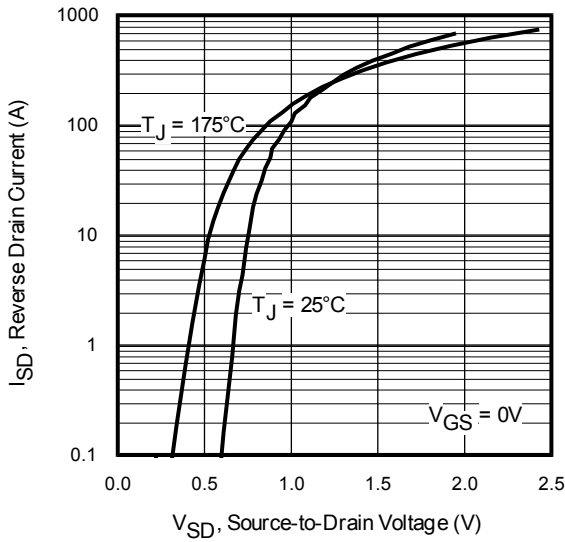
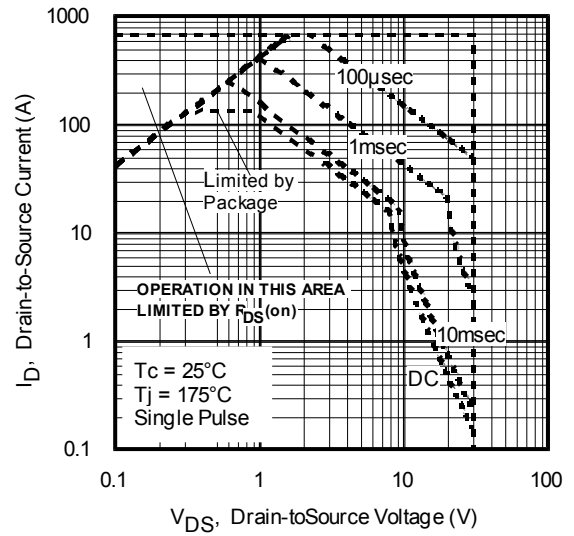
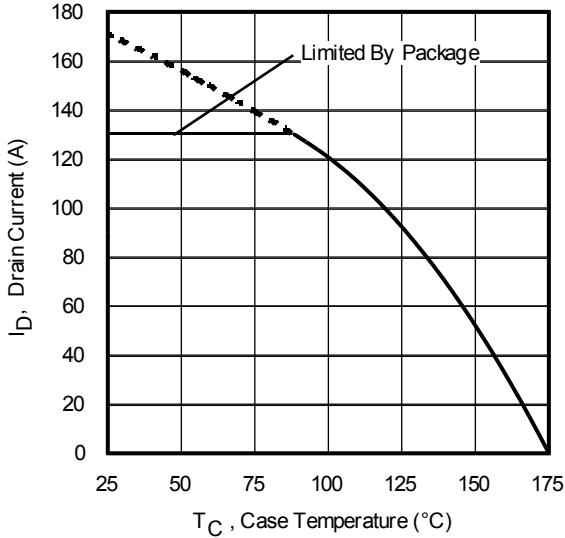
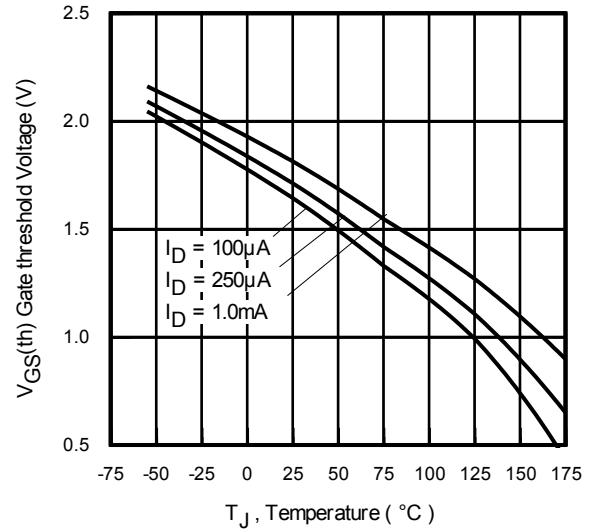
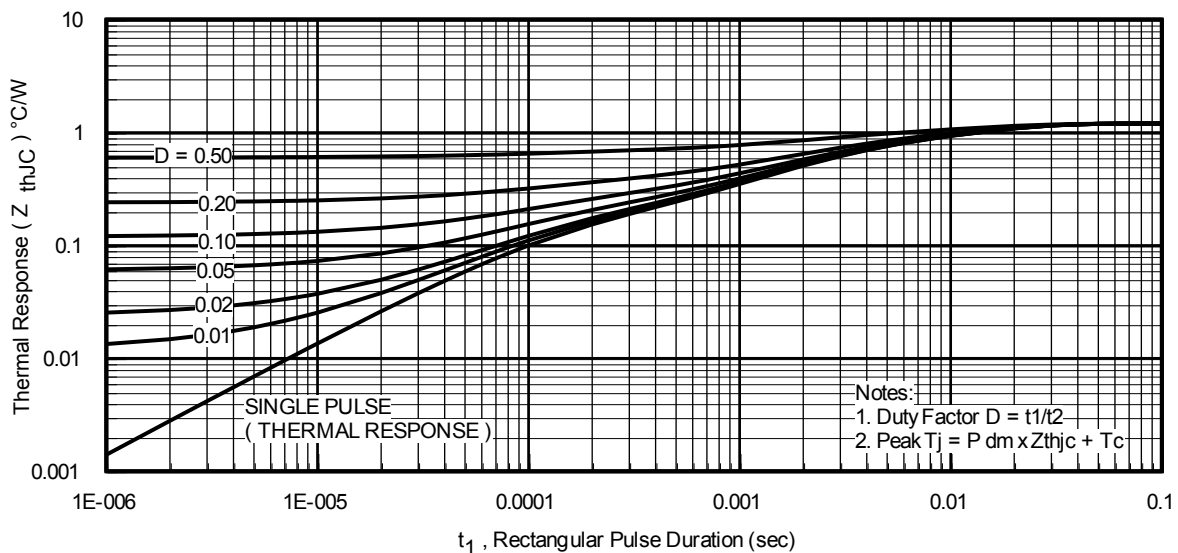
**Avalanche Characteristics**

E <sub>AS</sub> (Thermally limited)	Single Pulse Avalanche Energy ②	180	mJ
E <sub>AS</sub> (tested)	Single Pulse Avalanche Energy Tested Value ⑤	900	
I <sub>AR</sub>	Avalanche Current ①	68	A
E <sub>AR</sub>	Repetitive Avalanche Energy ①	12.5	mJ

**Diode Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode) ①	—	—	171 ⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	664		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.0	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 68A, V <sub>GS</sub> = 0V ③
t <sub>rr</sub>	Reverse Recovery Time	—	21	31	ns	T <sub>J</sub> = 25°C I <sub>F</sub> = 68A, V <sub>DD</sub> = 15V
Q <sub>rr</sub>	Reverse Recovery Charge	—	54	81	nC	di/dt = 430A/μs ③


**Fig 1. Typical Output Characteristics**

**Fig 2. Typical Output Characteristics**

**Fig 3. Typical Transfer Characteristics**

**Fig 4. Normalized On-Resistance vs. Temperature**

**Fig 5. Typical Capacitance vs. Drain-to-Source Voltage**

**Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage**


**Fig 7. Typical Source-Drain Diode Forward Voltage**

**Fig 8. Maximum Safe Operating Area**

**Fig 9. Maximum Drain Current vs. Case Temperature**

**Fig 10. Threshold Voltage vs. Temperature**

**Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case**

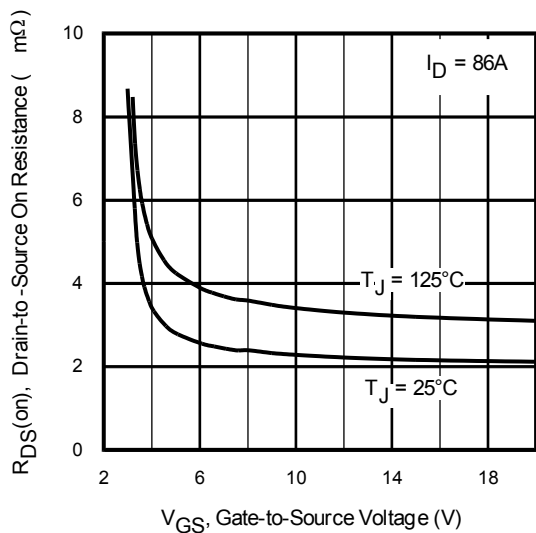


Fig 12. Typical On-Resistance vs. Gate Voltage

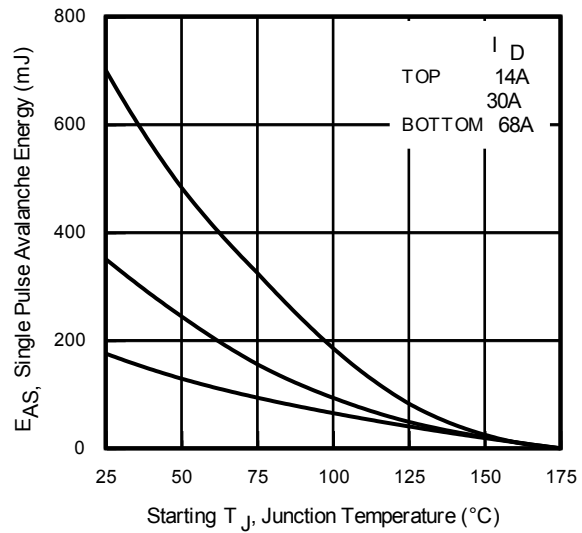
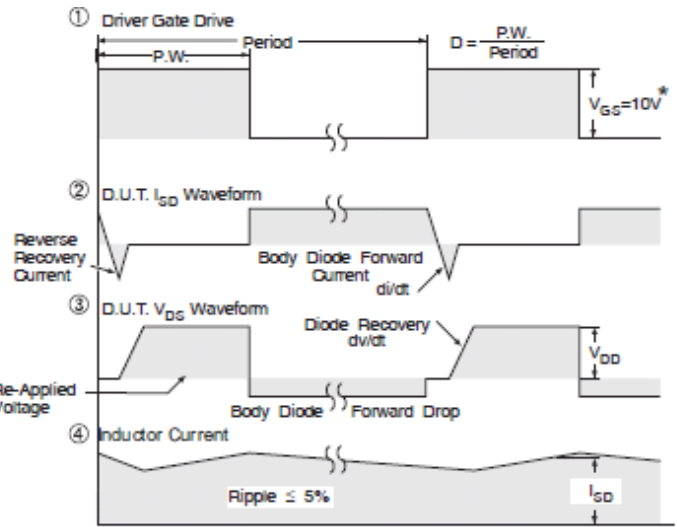
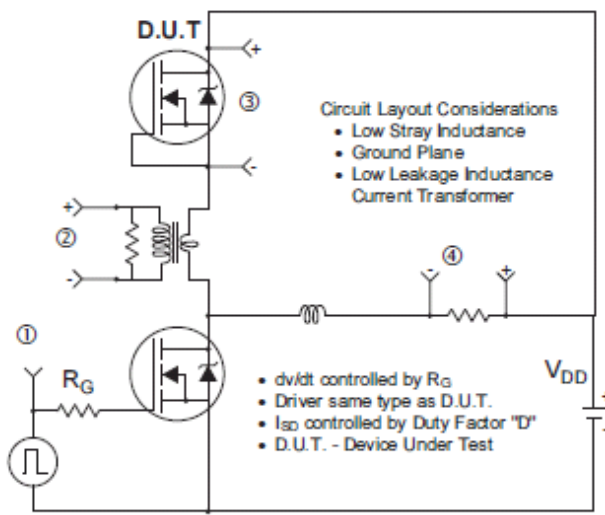
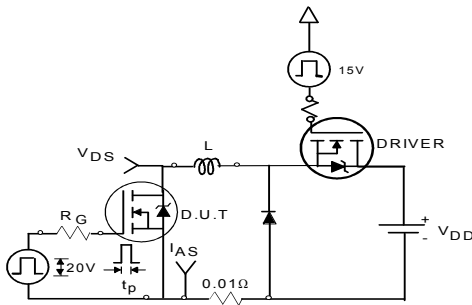


Fig 14. Maximum Avalanche Energy vs. Drain Current

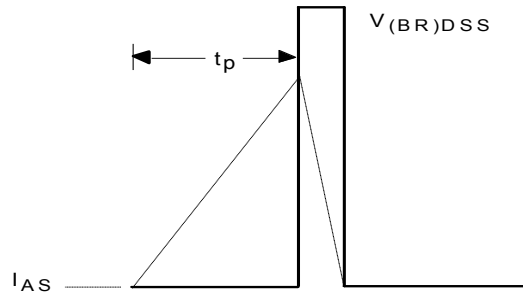


\*  $V_{GS} = 5V$  for Logic Level Devices

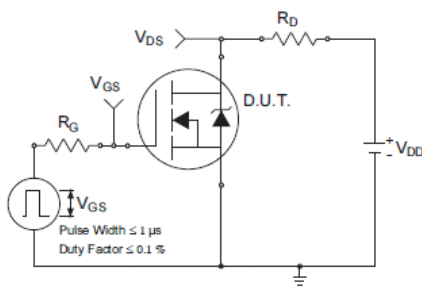
**Fig 18.** Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs



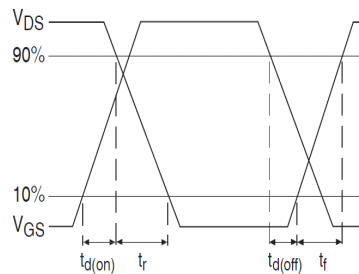
**Fig 19a.** Unclamped Inductive Test Circuit



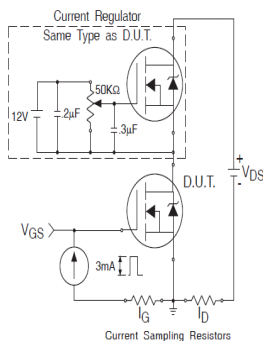
**Fig 19b.** Unclamped Inductive Waveforms



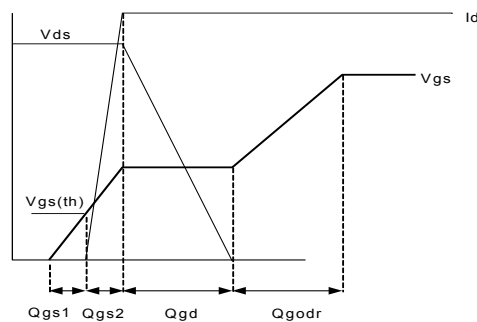
**Fig 20a.** Switching Time Test Circuit



**Fig 20b.** Switching Time Waveforms

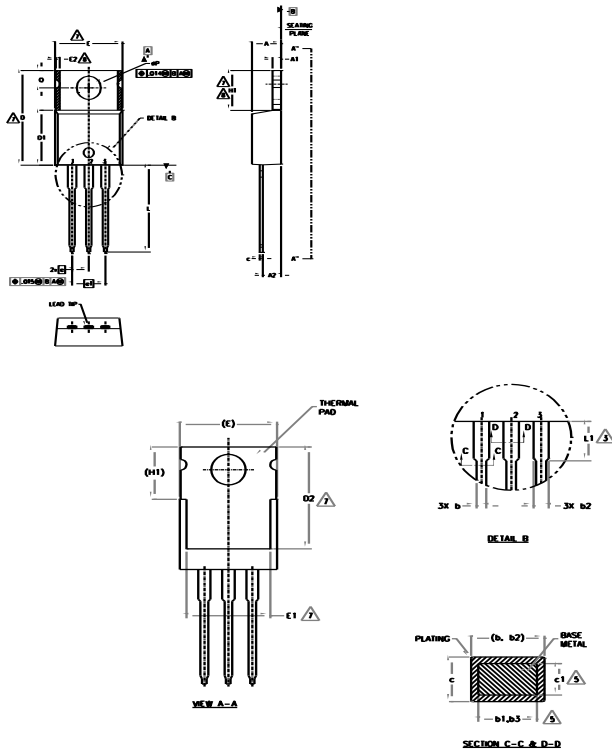


**Fig 21a.** Gate Charge Test Circuit



**Fig 21b.** Gate Charge Waveform

TO-220AB Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN LT.
- 4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- 6.- CONTROLLING DIMENSION : INCHES.
- 7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E1, D2 & E1
- 8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
- 9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

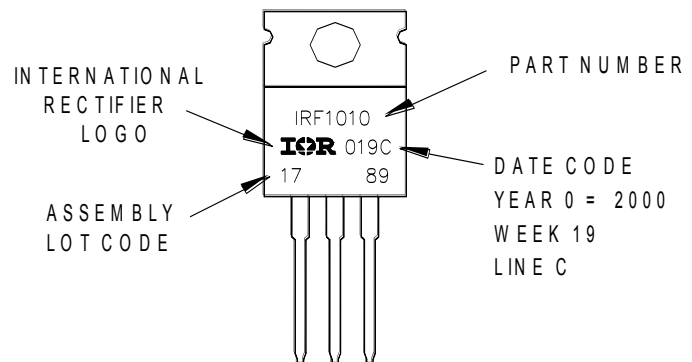
SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	-	0.76	-	.030	8
e	2.54 BSC		100 BSC		
e1	5.08 BSC		200 BSC		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
ØP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

- LEAD ASSIGNMENTS**
- HEAT SINK**
- 1.- GATE
  - 2.- BRANCH
  - 3.- SOURCE
- CRS. OPPOSITE**
- 1.- GATE
  - 2.- COLLECTOR
  - 3.- CONTROL
- WIREBOND**
- 1.- ANODE
  - 2.- CATHODE
  - 3.- ANODE

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 2000  
 IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"



TO-220AB packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>	Industrial (per JEDEC JESD47F) <sup>††</sup>	
<b>Moisture Sensitivity Level</b>	TO-220	N/A
<b>RoHS Compliant</b>	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

†† Applicable version of JEDEC standard at the time of product release.

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.067\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 68\text{A}$ ,  $V_{GS} = 10\text{V}$ .
- ③ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ④  $R_\theta$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .
- ⑤ This value determined from sample failure population, starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.5\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 60\text{A}$ ,  $V_{GS} = 10\text{V}$ .
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 130A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140).

International  
 Rectifier

**IR WORLD HEADQUARTERS:** 101N Sepulveda Blvd, El Segundo, California 90245, USA

To contact International Rectifier, please visit <http://www.irf.com/whoto-call/>