

1 W, VIPer01 evaluation board in buck topology

Data brief



- Self-supply to avoid auxiliary winding and bias component
- Delayed overload
- Max. duty cycle protection
- Thermal shutdown
- RoHS compliant

Description

The STEVAL-ISA178V1 uses the VIPER013XS, (drain current limitation $I_{DLIM} = 360$ mA and switching frequency $F_{OSC} = 30$ kHz, nominal values). The power supply is set in buck topology: $V_{OUT} = 5$ V; $I_{OUT} = 0.2$ A.

The input voltage range is 85 V_{AC} to 265 V_{AC} and the VIPer01 switching frequency is 60 kHz.

The FB pin of the VIPer01 is the inverting input of an error amplifier and is an accurate 1.2 V voltage reference with respect to the GND pin.

The IC is biased through a diode connected to V_{OUT} . Therefore, thanks to the low consumption of the internal blocks of the VIPer01, very low input power consumption under light or no load conditions is possible (less than 15 mW @ 230 V_{AC} under no load with an adequate design).

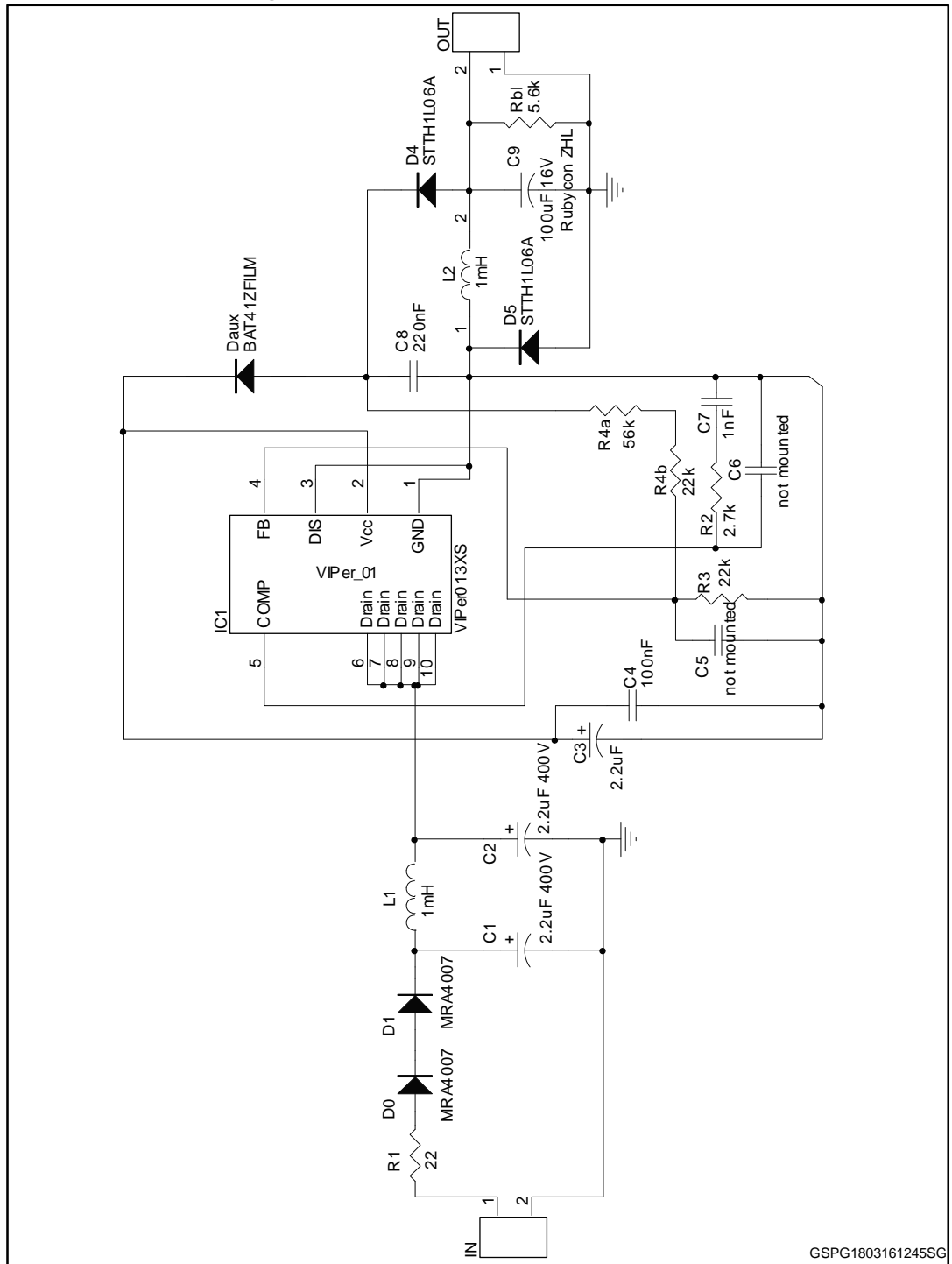
The VIPer01 is also equipped with a frequency reduction feature to limit excessive currents at startup, as well as overload/short-circuit and overtemperature management.

Features

- 800 V, avalanche rugged primary MOSFET
- Input power consumption in no load condition lower than 15 mW @ 230 V_{AC}
- Input power consumption in ZEROPOWER mode lower than 8 mW @ 230 V_{AC}
- On-board trans-conductance E/A with 1.2 V \pm 2% floating reference voltage
- Embedded HV startup
- Built-in soft-start
- Current mode PWM controller
- Frequency jittering to reduce the EMI filter cost
- Pulse skip mode to avoid flux-runaway during startup

1 Schematic diagram

Figure 1: STEVAL-ISA178V1 circuit schematic



GSPG1803161245SG

2 Revision history

Table 1: Document revision history

Date	Version	Changes
25-Mar-2016	1	Initial release.

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