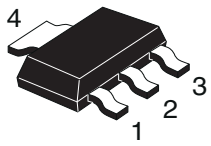
STN3P6F6

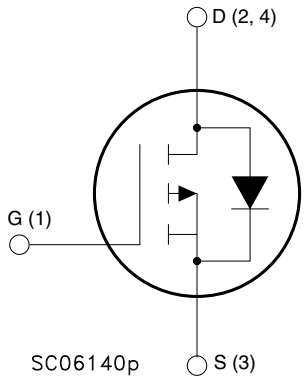
P-channel 60 V, 0.13 Ω typ., 3 A STripFET™ VI DeepGATE™ Power MOSFET in a SOT-223 package

Datasheet - production data



SOT-223

Figure 1. Internal schematic diagram



Features

Order code	V_{DSS}	$R_{DS(on)max}$	I_D
STN3P6F6	60 V	0.16 Ω @ 10 V	3 A

- $R_{DS(on)}$ * Qg industry benchmark
- Extremely low on-resistance $R_{DS(on)}$
- High avalanche ruggedness
- Low gate drive power losses

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the 6th generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest $R_{DS(on)}$ in all packages.

Table 1. Device summary

Order code	Marking	Package	Packaging
STN3P6F6	STN3P6F6	SOT-223	Tape and reel

Note: For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at T_{pcb} = 25 °C	3	A
I_D	Drain current (continuous) at T_{pcb} = 100 °C	2	A
I_{DM}	Drain current (pulsed)	12	A
P_{TOT} (1)	Total dissipation at T_{pcb} = 25 °C	2.6	W
T_j P_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

1. Pulse width is limited by safe operating area.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb max	57	°C/W

1. When mounted on FR-4 board of 15 mm^2, 2 Oz Cu, t<10 sec

Note: For the P-channel Power MOSFET actual polarity of voltages and current has to be reversed.

2 Electrical characteristics

(Tcase = 25 °C unless otherwise specified).

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS} = 0)	I_D = 250 µA	60			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 60 V V_{DS} = 60 V, T_C=125 °C			1 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 1.5 A		0.13	0.16	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 48 V, f = 1 MHz, V_{GS} = 0	-	340 40 20	-	pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 48 V, I_D = 3 A, V_{GS} = 10 V (see *Figure 14*)	-	6.4 1.7 1.7	-	nC nC nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 48 V, I_D = 1.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 13*)	-	6.4 5.3 14 3.7	-	ns ns ns ns

Note: For the P-channel Power MOSFET actual polarity of voltages and current has to be reversed.

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		3 12	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 3 A, V_{GS} = 0	-		1.1	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 5 A, di/dt = 100 A/µs V_{DD} = 16 V, T_j = 150 °C (see *Figure 15*)	-	20 17.8 1.8		ns nC A

1. Pulse width limited by safe operating area.
2. Pulse duration = 300 µs, duty cycle 1.5%

Note: For the P-channel Power MOSFET actual polarity of voltages and current has to be reversed.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

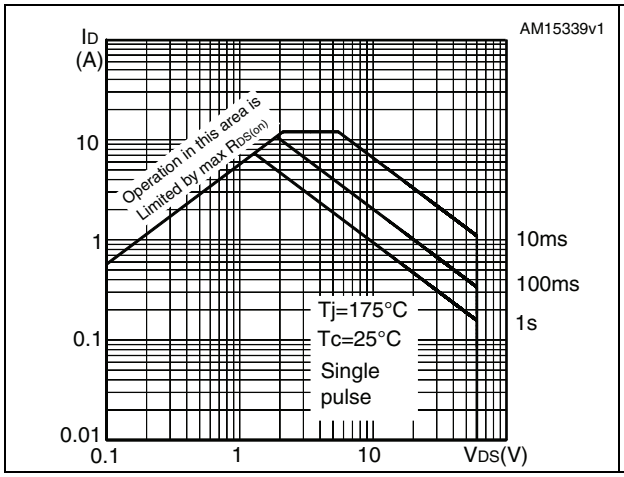


Figure 3. Thermal impedance

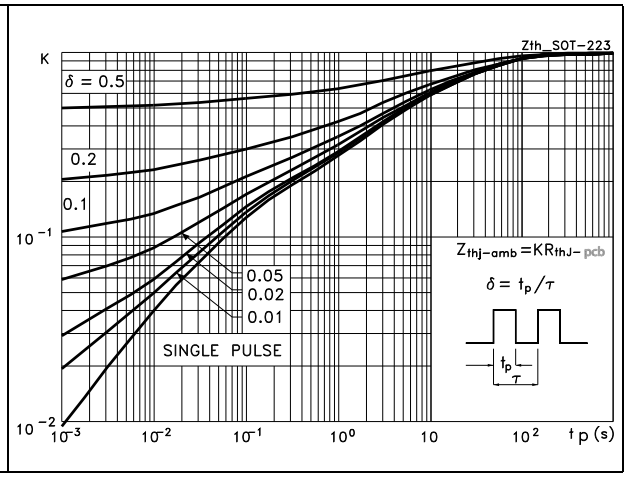


Figure 4. Output characteristics

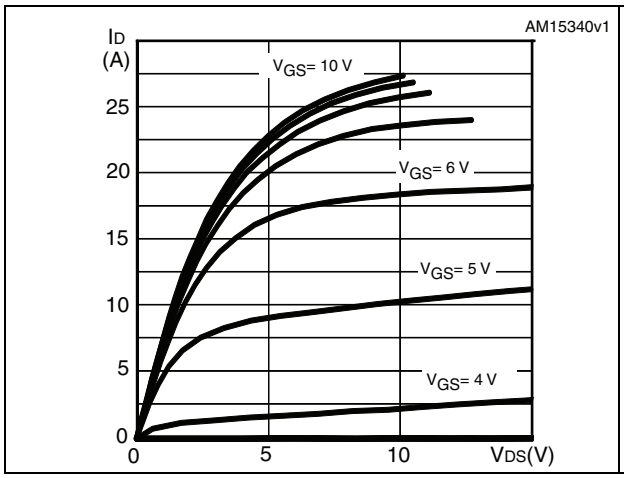


Figure 5. Transfer characteristics

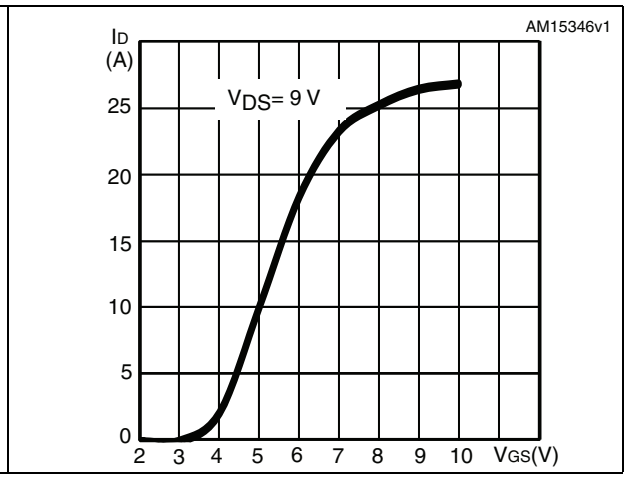


Figure 6. Gate charge vs gate-source voltage

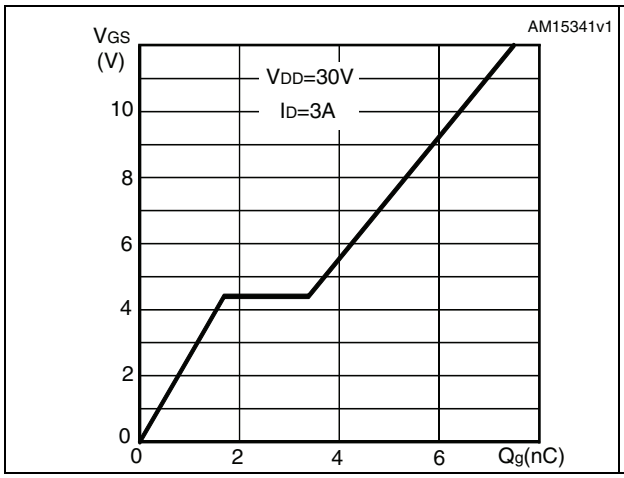


Figure 7. Static drain-source on-resistance

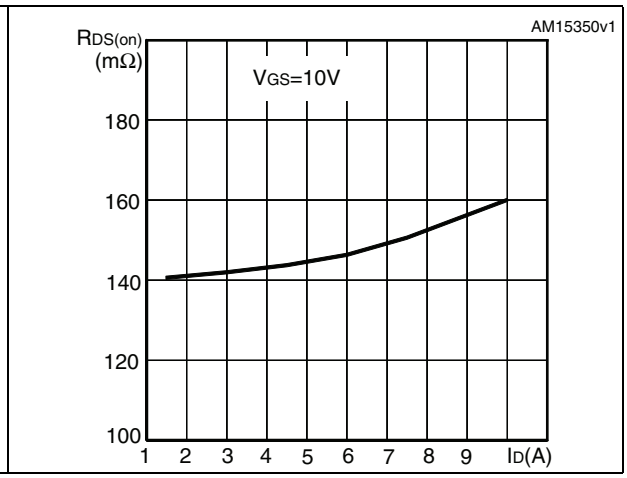


Figure 8. Capacitance variations

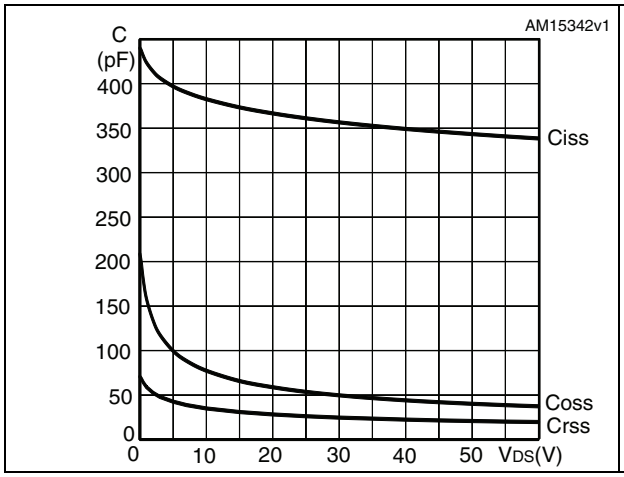


Figure 9. Normalized B_{VDSS} vs temperature

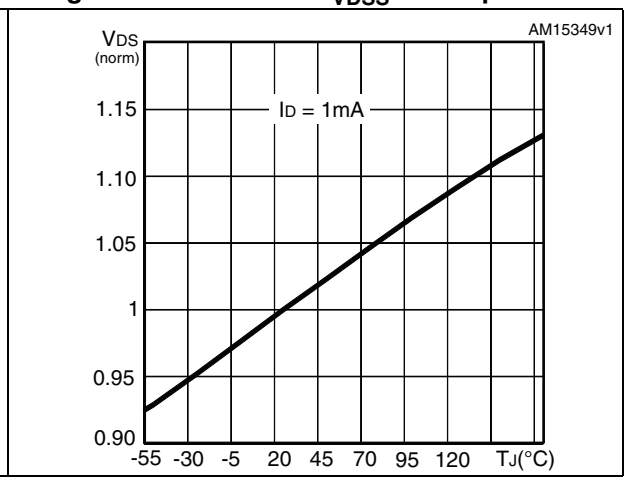


Figure 10. Normalized gate threshold voltage vs temperature

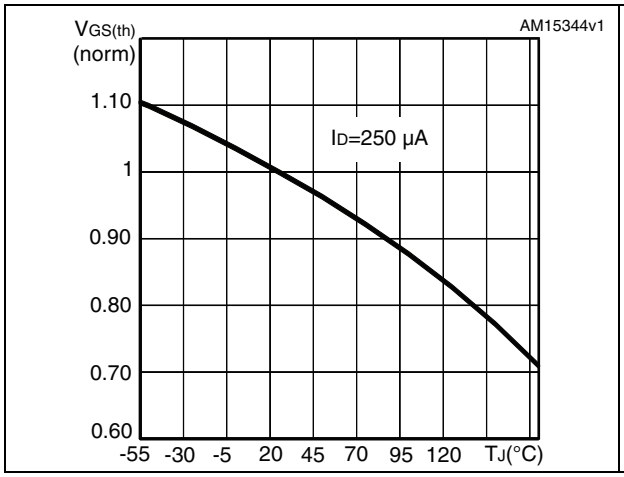


Figure 11. Normalized on-resistance vs temperature

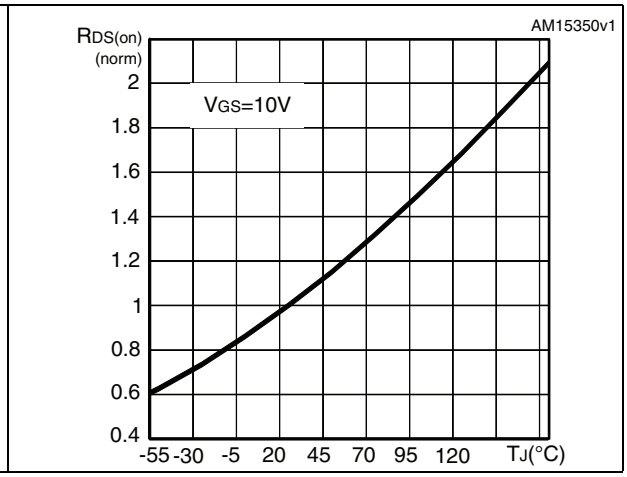
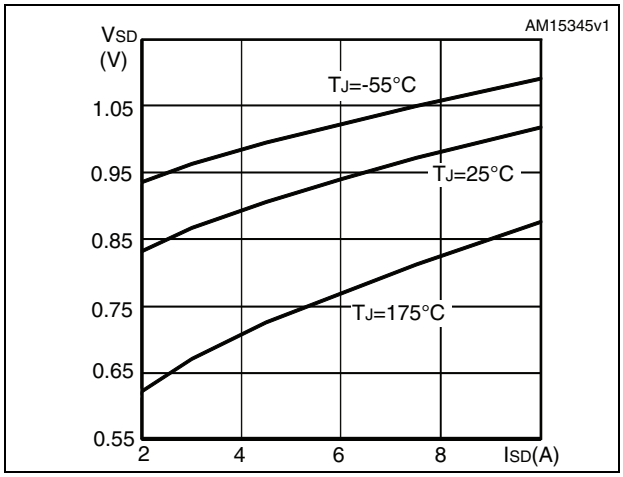


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

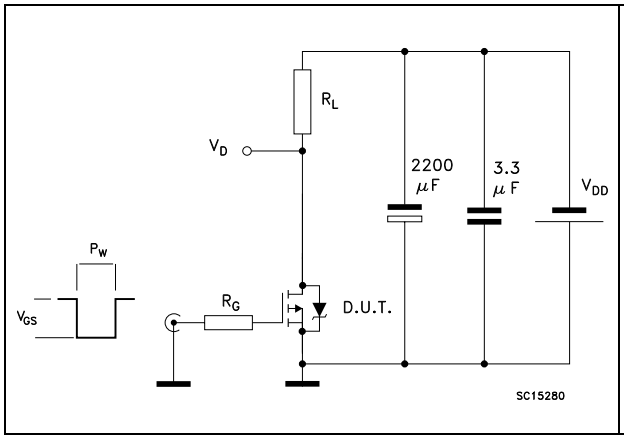


Figure 14. Gate charge test circuit

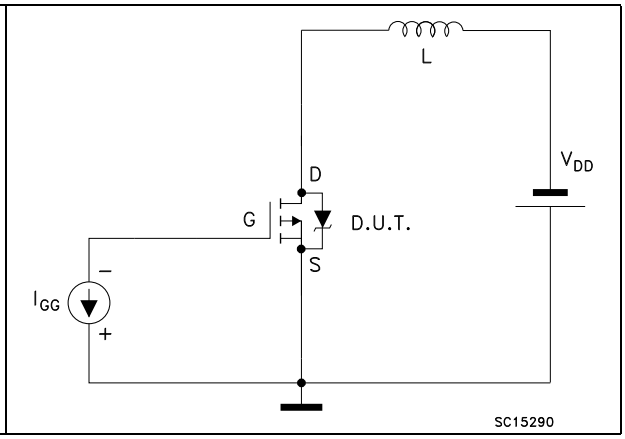
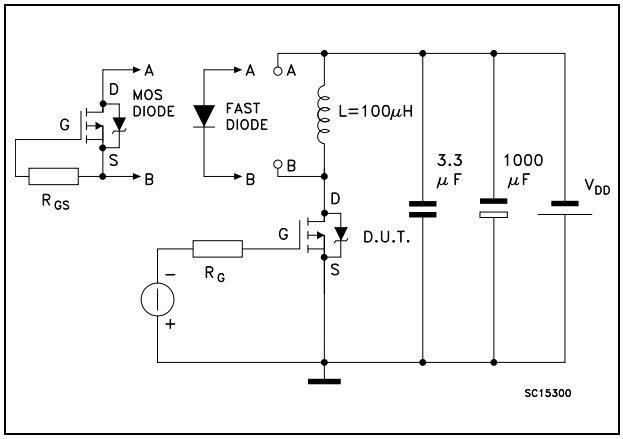


Figure 15. Test circuit for inductive load switching and diode recovery times



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
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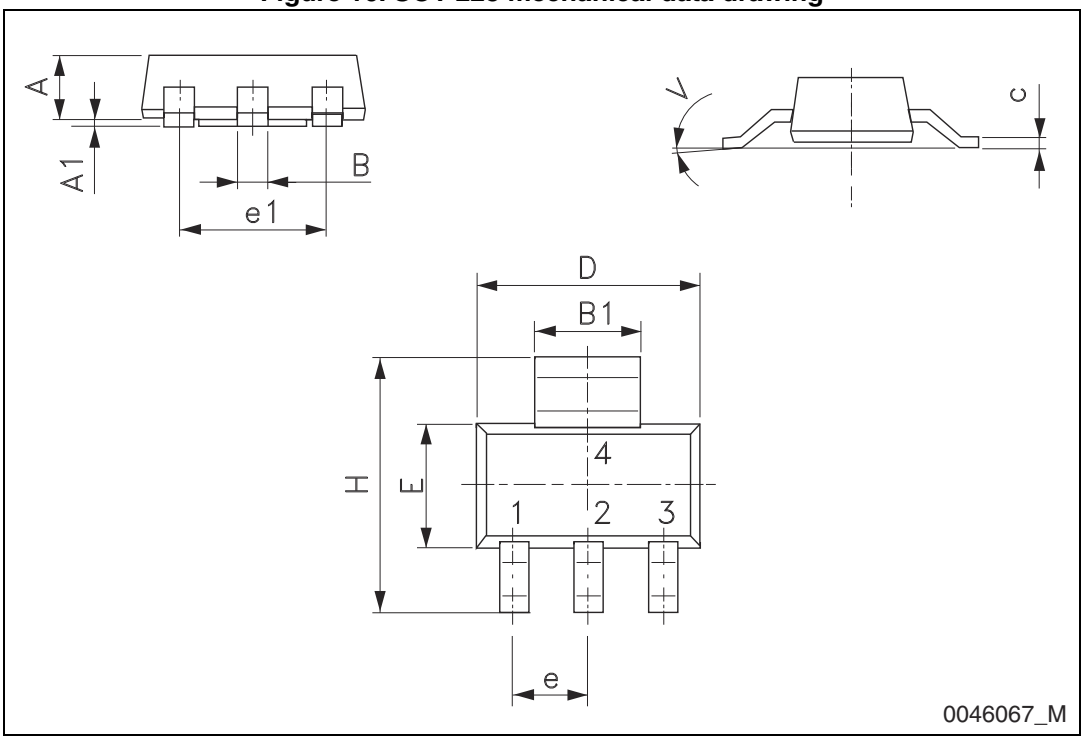
Table 8. SOT-223 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.80
A1	0.02		0.1
B	0.60	0.70	0.85
B1	2.90	3.00	3.15
c	0.24	0.26	0.35
D	6.30	6.50	6.70
e		2.30	
e1		4.60	
E	3.30	3.50	3.70
H	6.70	7.00	7.30
V			10°

Figure 16. SOT-223 mechanical data drawing



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
31-Oct-2012	1	First release.
09-Nov-2012	2	Modified: note *1* in *Table 3*
16-Jan-2013	3	Document status promoted from preliminary data to production data
14-Mar-2013	4	Modified: *Figure 1*, *3*, C_{iss}, C_{oss}, C_{rss} typical values in *Table 5*

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