



FDC5614P

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60V P-Channel Logic Level PowerTrench[®] MOSFET

General Description

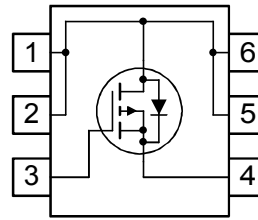
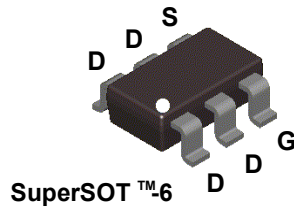
This 60V P-Channel MOSFET uses Fairchild's high voltage PowerTrench process. It has been optimized for power management applications.

Applications

- DC-DC converters
- Load switch
- Power management

Features

- -3 A, -60 V. $R_{DS(ON)} = 0.105 \Omega @ V_{GS} = -10 V$
 $R_{DS(ON)} = 0.135 \Omega @ V_{GS} = -4.5 V$
- Fast switching speed
- High performance trench technology for extremely low $R_{DS(ON)}$



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V _{DSS}	Drain-Source Voltage	-60	V
V _{GSS}	Gate-Source Voltage	±20	V
I _D	Drain Current – Continuous (Note 1a)	-3	A
	– Pulsed	-20	
P _D	Maximum Power Dissipation (Note 1a) (Note 1b)	1.6	W
		0.8	
T _J , T _{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	°C/W
R _{θJC}	Thermal Resistance, Junction-to-Case (Note 1)	30	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.564	FDC5614P	7"	8mm	3000 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, Referenced to 25°C		-49		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -48\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
I_{GSSF}	Gate–Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-1	-1.6	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, Referenced to 25°C		4		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = -10\text{ V}, I_D = -3\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -2.7\text{ A}$ $V_{GS} = -10\text{ V}, I_D = -3\text{ A}, T_J = 125^\circ\text{C}$		82 105 130	105 135 190	m Ω
$I_{D(on)}$	On–State Drain Current	$V_{GS} = -10\text{ V}, V_{DS} = -5\text{ V}$	-20			A
g_{FS}	Forward Transconductance	$V_{DS} = -5\text{ V}, I_D = -3\text{ A}$		8		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V},$		759		pF
C_{oss}	Output Capacitance	$f = 1.0\text{ MHz}$		90		pF
C_{riss}	Reverse Transfer Capacitance			39		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = -30\text{ V}, I_D = -1\text{ A},$		7	14	ns
t_r	Turn–On Rise Time	$V_{GS} = -10\text{ V}, R_{GEN} = 6\ \Omega$		10	20	ns
$t_{d(off)}$	Turn–Off Delay Time			19	34	ns
t_f	Turn–Off Fall Time			12	22	ns
Q_g	Total Gate Charge	$V_{DS} = -30\text{ V}, I_D = -3.0\text{ A},$		15	24	nC
Q_{gs}	Gate–Source Charge	$V_{GS} = -10\text{ V}$		2.5		nC
Q_{gd}	Gate–Drain Charge			3.0		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				-1.3	A
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -1.3\text{ A}$ (Note 2)		-0.8	-1.2	V

Notes:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
 - 78°C/W when mounted on a 1 in^2 pad of 2oz copper on FR-4 board.
 - 156°C/W when mounted on a minimum pad.
- Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$

Typical Characteristics

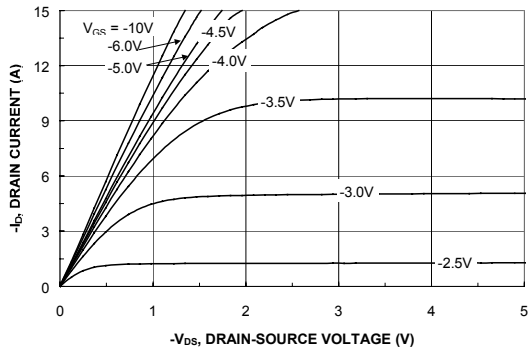


Figure 1. On-Region Characteristics.

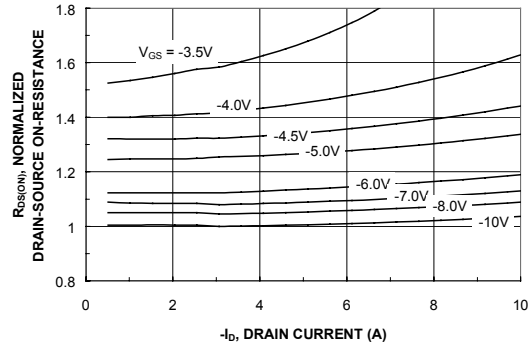


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

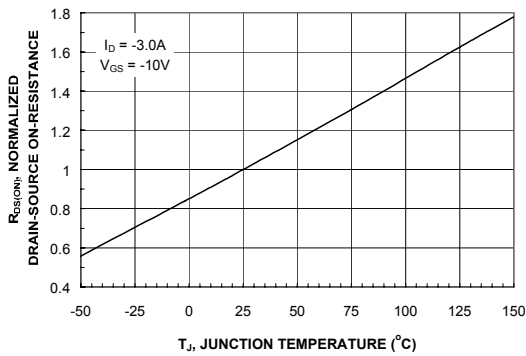


Figure 3. On-Resistance Variation with Temperature.

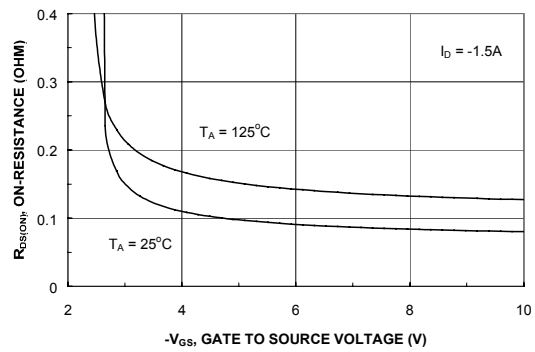


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

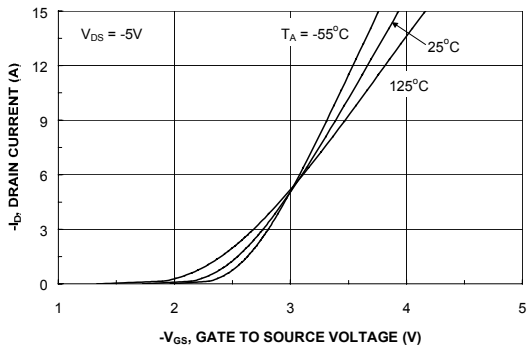


Figure 5. Transfer Characteristics.

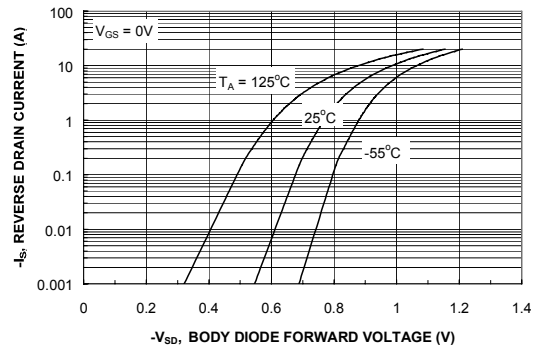


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

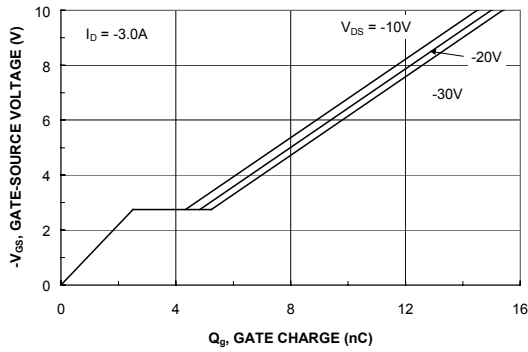


Figure 7. Gate Charge Characteristics.

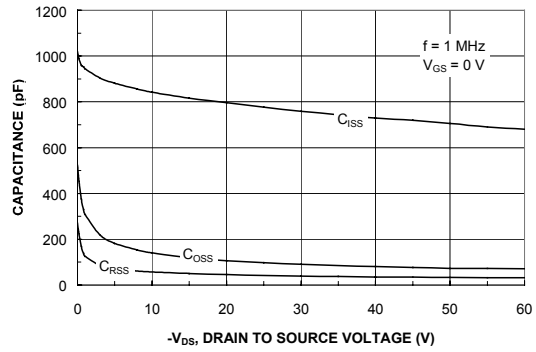


Figure 8. Capacitance Characteristics.

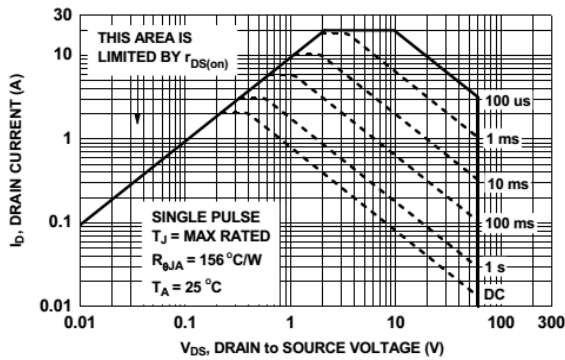


Figure 9. Maximum Safe Operating Area.

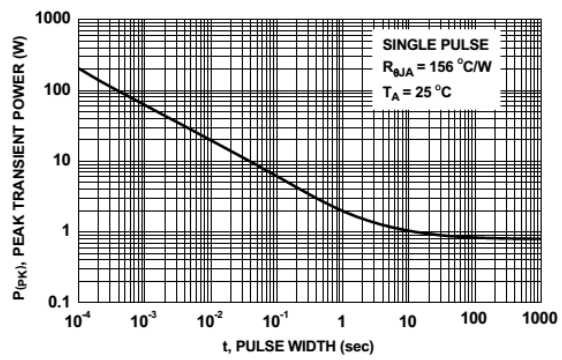
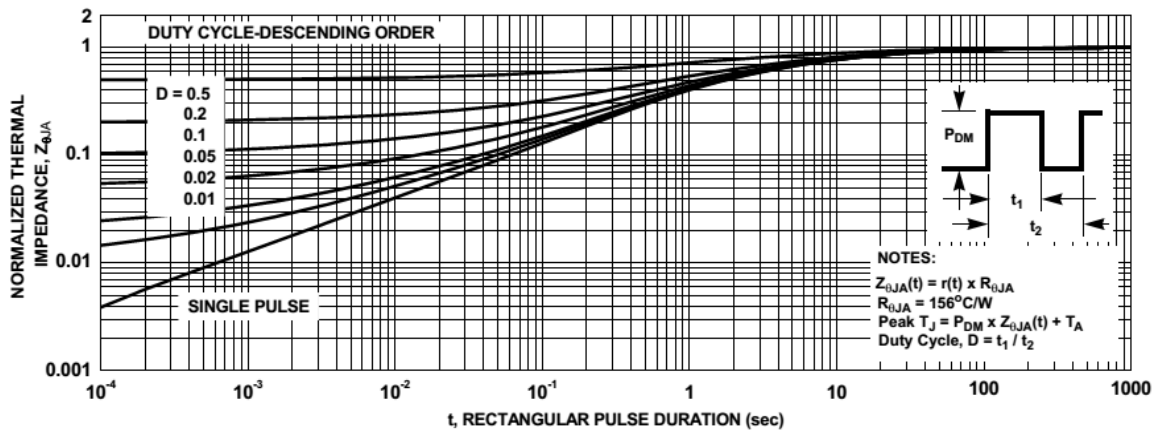
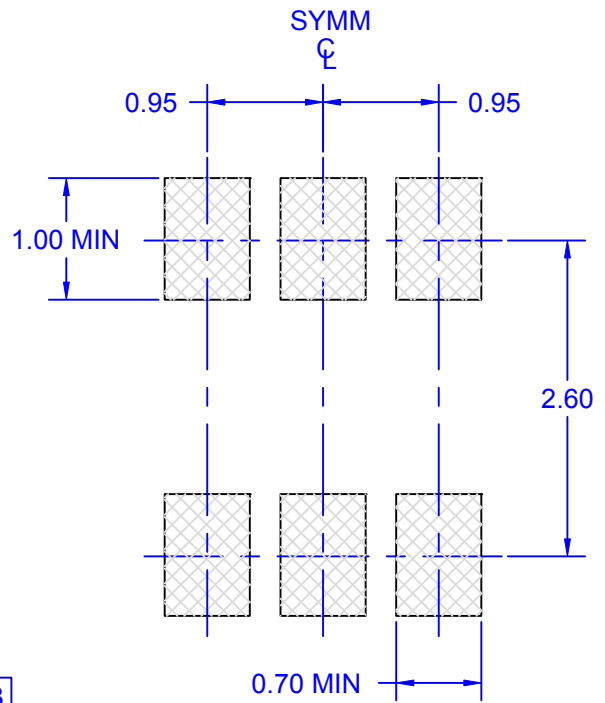
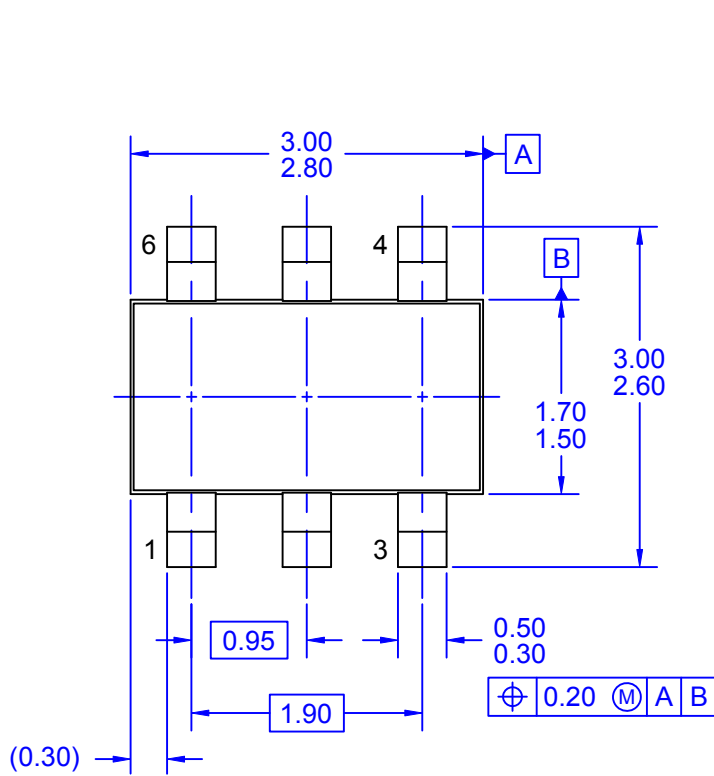


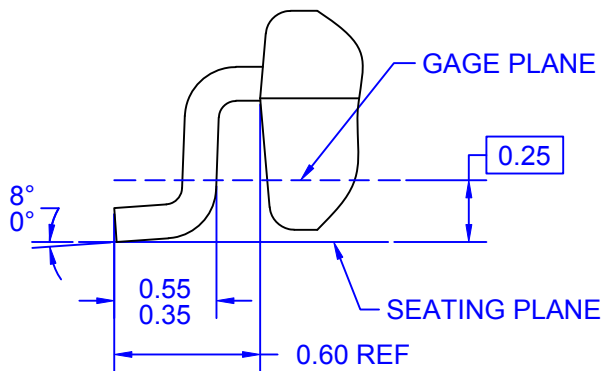
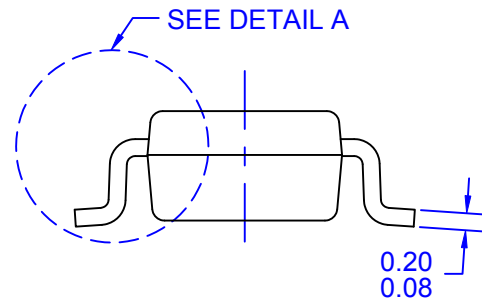
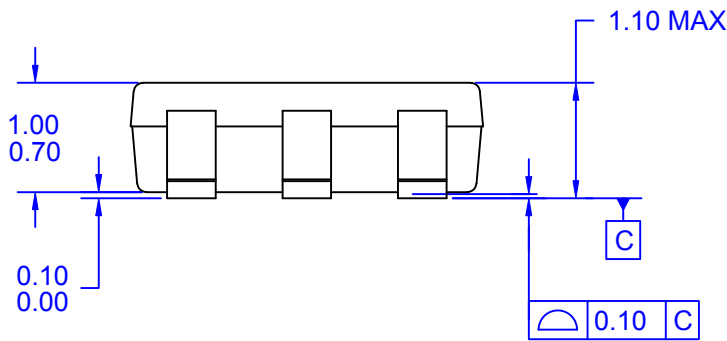
Figure 10. Single Pulse Maximum Power Dissipation.



Thermal characterization performed using the conditions described in Note 1b.
 Transient thermal response will change depending on the circuit board design.



LAND PATTERN RECOMMENDATION



DETAIL A
SCALE: 50X

- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC MO-193. VAR. AA, ISSUE C, DATED JANUARY 2000.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 2009.
 - D) DRAWING FILE NAME: MKT-MA06AREV5





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