# Avalanche Photodiode Bias Controller and Wide Range (5 nA to 5 mA) Current Monitor

# ADL5317

## FEATURES

- Accurately sets avalanche photodiode (APD) bias voltage
  - Wide bias range from 6 V to 75 V
- 3 V-compatible control interface
- Monitors photodiode current (5:1 ratio) over six decades
- Linearity 0.25% from 10 nA to 1 mA, 0.5% from 5 nA to 5 mA
- Overcurrent protection and overtemperature shutdown
- Miniature 16-lead chip scale package (LFCSP 3 mm × 3 mm)

## APPLICATIONS

- Optical power monitoring and biasing in APD systems
- Wide dynamic range voltage sourcing and current monitoring in high voltage systems

## FUNCTIONAL BLOCK DIAGRAM

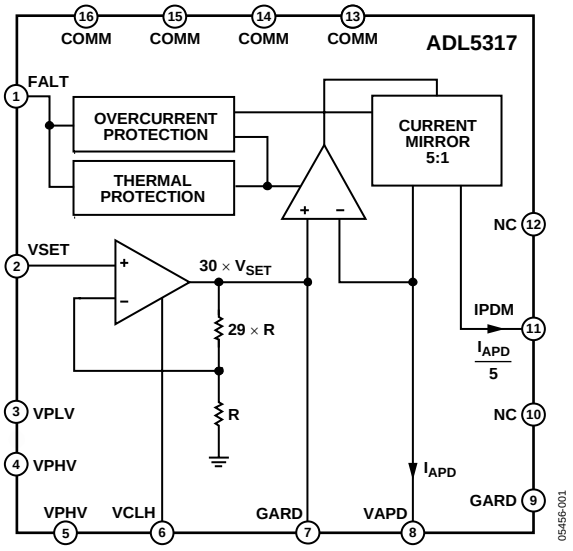


*Figure 1.*

## GENERAL DESCRIPTION

The ADL5317 is a high voltage, wide dynamic range, biasing and current monitoring device optimized for use with avalanche photodiodes. When used with a stable high voltage supply (up to 80 V), the bias voltage at the VAPD pin can be varied from 6 V to 75 V using the 3 V-compatible VSET pin. The current sourced from the VAPD pin over a range of 5 nA to 5 mA is accurately mirrored with an attenuation of 5 and sourced from the IPDM monitor output. In a typical application, the monitor output drives a current input logarithmic amplifier to produce an output representing the optical power incident upon the photodiode. The photodiode anode can be connected to a high speed transimpedance amplifier for the extraction of the data stream.

A signal of 0.2 V to 2.5 V with respect to ground applied at the VSET pin is amplified by a fixed gain of 30 to produce the 6 V to 75 V bias at Pin VAPD. The accuracy of the bias control interface of the ADL5317 allows for straightforward calibration, thereby maintaining a constant avalanche multiplication factor of the photodiode over temperature. The current monitor output, IPDM, maintains its high linearity vs. photodiode current over the full range of APD bias voltage. The current ratio of 5:1 remains constant as $V_{SET}$ and $V_{PHV}$ are varied.

The ADL5317 also offers a supply tracking mode compatible with adjustable high voltage supplies. The VAPD pin accurately follows 2.0 V below the VPHV supply pin when VSET is tied to a voltage from 3.0 V to 5.5 V (or higher with a current limiting resistor), and the VCLH pin is open.

Protection from excessive input current at VAPD as well as excessive die temperature is provided. The voltage at VAPD falls rapidly from its setpoint when the input current exceeds 18 mA nominally. A die temperature in excess of 140°C will cause the bias controller and monitor to shut down until the temperature falls below 120°C. Either overstress condition will trigger a logic low at the FALT pin, an open collector output loaded by an external pull-up to an appropriate logic supply (1 mA max).

The ADL5317 is available in a 16-lead LFCSP package and is specified for operation from −40°C to +85°C.

**Rev. 0**



One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

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- CN0057

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- Optical and High Speed Networking ICs

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## REVISION HISTORY

**7/05—Revision 0: Initial Version**

# SPECIFICATIONS

$V_{PHV}$ = 78 V, $V_{PLV}$ = 5 V, $V_{APD}$ = 60 V, $I_{APD}$ = 5 µA, $T_A$ = 25°C, unless otherwise noted.

**Table 1.**

| Parameter | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|
| CURRENT MONITOR OUTPUT | | | | | IPDM (Pin 11 ) |
| Current Gain from VAPD to IPDM | 0.198 | 0.200 | 0.202 | A/A | $T_A$ = 25°C |
| | 0.193 | | 0.207 | | −40°C < $T_A$ < +85°C |
| Nonlinearity | | 0.25 | 1.6 | % | 10 nA < $I_{APD}$ < 1 mA |
| | | 0.5 | 3.0 | % | 5 nA < $I_{APD}$ < 5 mA |
| Small-Signal Bandwidth | | 2 | | kHz | $I_{APD}$ = 5 nA, $V_{PHV}$ = 60 V, $V_{APD}$ = 30 V |
| | | 2 | | MHz | $I_{APD}$ = 5 µA, $V_{PHV}$ = 60 V, $V_{APD}$ = 30 V |
| Wideband Noise at IPDM | | 10 | | nA | $I_{APD}$ = 5 µA, $C_{GRD}$ = 2 nF, BW = 10 MHz, $V_{PHV}$ = 40 V, $V_{APD}$ = 30 V |
| Output Voltage Range | 0 | | $V_{PLV}$ | V | $V_{APD}$ > 3 × $V_{PLV}$ |
| | 0 | | $V_{APD}$ / 3 | V | $V_{APD}$ < 3 × $V_{PLV}$ |
| APD BIAS CONTROL | | | | | VSET (Pin 2), VAPD (Pin 8) |
| Specified $V_{APD}$ Voltage Operating Range | 6 | | $V_{PHV}$ − 1.5 | V | 10 V < $V_{PHV}$ < 41 V |
| | $V_{PHV}$ − 35 | | $V_{PHV}$ − 1.5 | V | 41 V < $V_{PHV}$ < 76.5 V |
| | $V_{PHV}$ − 35 | | 75 | V | 76.5 V < $V_{PHV}$ < 80 V |
| VAPD to GARD Offset | | 3 | | mV | |
| Specified Input Current Range, $I_{APD}$ | 5n | | 5m | A | Flows from VAPD pin |
| VSET to VAPD Incremental Gain | 29.7 | 30 | 30.3 | V/V | 0.2 V < $V_{SET}$ < 2.5 V[1] |
| VSET Input Referred Offset, 1σ | | 0.5 | | mV | |
| VSET Voltage Range | 0.2 | | 5.5 | V | |
| Incremental Input Resistance at VSET | | 100 | | MΩ | $V_{SET}$ = 2.0 V |
| Input Bias Current at VSET | | 0.3 | | µA | $V_{SET}$ = 2.0 V, flows from VSET pin |
| $V_{APD}$ Settling Time, 5% | | 20 | | µsec | $V_{SET}$ = 1.6 V to 2.4 V, $C_{GRD}$ = 2 nF, $V_{PHV}$ = 60 V, $V_{APD}$ = 30 V |
| | | 100 | | µsec | $V_{SET}$ = 2.4 V to 1.6 V, $C_{GRD}$ = 2 nF, $V_{PHV}$ = 60 V, $V_{APD}$ = 30 V |
| $V_{APD}$ Supply Tracking Offset (Below $V_{PHV}$) | 1.90 | 2.0 | 2.15 | V | $V_{SET}$ = 5.0 V, 10 V < $V_{PHV}$ < 77 V |
| OVERSTRESS PROTECTION | | | | | FALT (Pin 1) |
| VAPD Current Compliance Limit | 14 | 18 | 21 | mA | $V_{SET}$ = 2.0 V, $V_{APD}$ deviation of 500 mV |
| Thermal Shutdown Trip Point | | 140 | | °C | Die temperature rising |
| Thermal Hysteresis | | 20 | | °C | |
| FALT Output Low Voltage | | | 0.8 | V | Fault condition, load current < 1 mA |
| POWER SUPPLIES | | | | | VPHV (Pin 4, Pin 5), VPLV (Pin 3) |
| Low Voltage Supply | 4 | | 6 | V | VPLV |
| Quiescent Current | | 0.7 | 0.84 | mA | Independent of $I_{APD}$ |
| High Voltage Supply | 10 | | 80 | V | VPHV |
| Quiescent Current | | 2.3 | 2.9 | mA | $I_{APD}$ = 5 µA, $V_{APD}$ = 60 V |
| | | 3.6 | 4.5 | mA | $I_{APD}$ = 1 mA, $V_{APD}$ = 60 V |

[1] Tested 1.5 V < $V_{SET}$ < 2.5 V, guaranteed operation 0.2 V < $V_{SET}$ < 2.5 V.

# ABSOLUTE MAXIMUM RATINGS

**Table 2.**

| Parameter | Rating |
|---|---|
| Supply Voltage | 80 V |
| Input Current at VAPD | 25 mA |
| Internal Power Dissipation | 615 mW |
| $\theta_{JA}$ (Soldered Exposed Paddle) | 65°C/W |
| Maximum Junction Temperature | 125°C |
| Operating Temperature Range | −40°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature Range (Soldering 60 sec) | 300°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

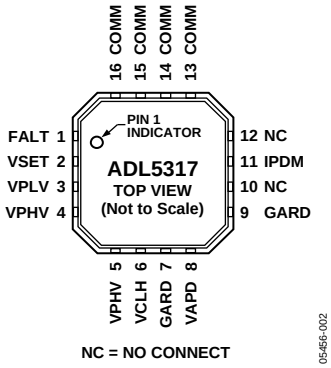



*Figure 2. Pin Configuration*

**Table 3. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | FALT | Open Collector (Active Low) Logic Output. Indicates an overcurrent or overtemperature condition. |
| 2 | VSET | APD Bias Voltage Setting Input. Short to VPLV for supply tracking mode. |
| 3 | VPLV | Low Voltage Supply, 4 V to 6 V. |
| 4, 5 | VPHV | High Voltage Supply, 10 V to 80 V. |
| 6 | VCLH | Can be shorted to VPHV for extended linear operating range. No connect for supply tracking mode. |
| 7, 9 | GARD | Guard pin tracks VAPD pin and filters setpoint buffer noise (with External Capacitor $C_{GRD}$ to COMM). Optional shielding of VAPD trace. Capacitive load only. |
| 8 | VAPD | APD Bias Voltage Output and Current Input. Sources current only. |
| 10, 12 | NC | Optional shielding of IPDM trace. No connection to die. |
| 11 | IPDM | Photodiode Monitor Current Output. Sources current only. Current at this node is equal to $I_{APD}/5$. |
| 13 to 16 | COMM | Analog Ground. |

# TYPICAL PERFORMANCE CHARACTERISTICS

$V_{PHV}$ = 78 V, $V_{PLV}$ = 5 V, $V_{APD}$ = 60 V, $I_{APD}$ = 5 µA, $T_A$ = 25°C, unless otherwise noted.

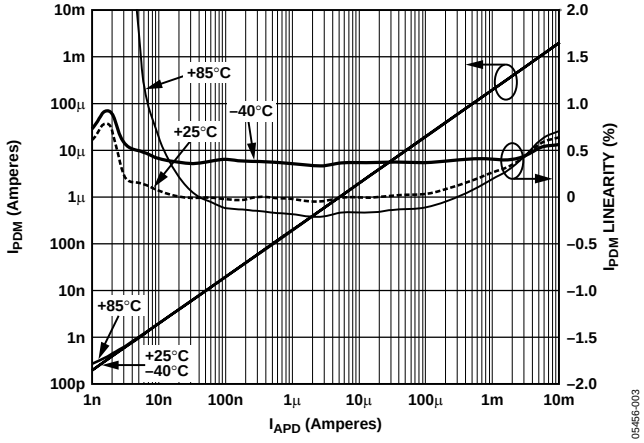



Figure 3. $I_{PDM}$ Linearity for Multiple Temperatures, Normalized to $I_{APD}$ = 5 µA, 25°C

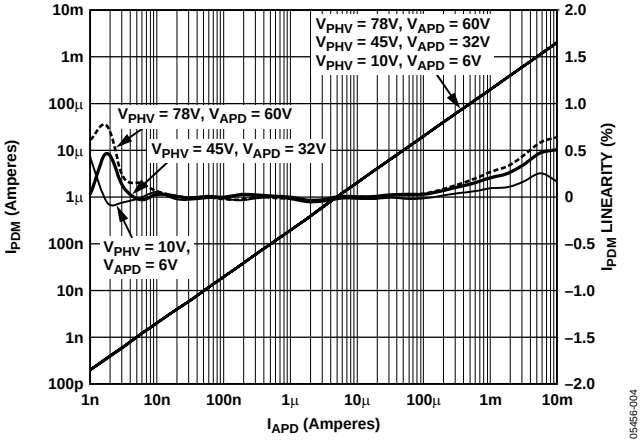



Figure 6. $I_{PDM}$ Linearity for Multiple Values of $V_{APD}$ and $V_{PHV}$, Normalized to $I_{APD}$ = 5 µA, $V_{PHV}$ = 78 V, $V_{APD}$ = 60 V

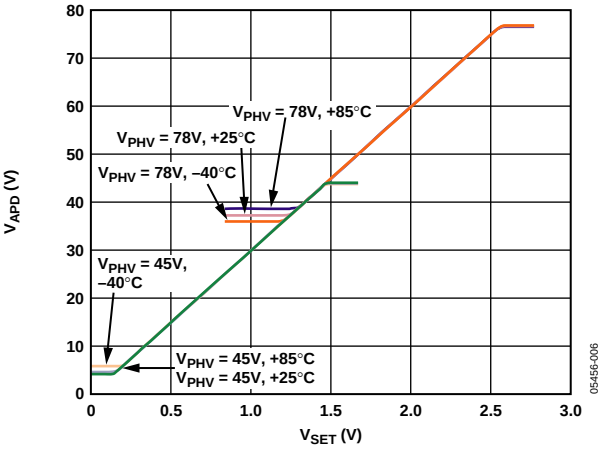



Figure 4. $V_{APD}$ vs. $V_{SET}$ for Multiple Temperatures, $V_{PHV}$ = 78 V and $V_{PHV}$ = 45 V, $I_{APD}$ = 5 µA

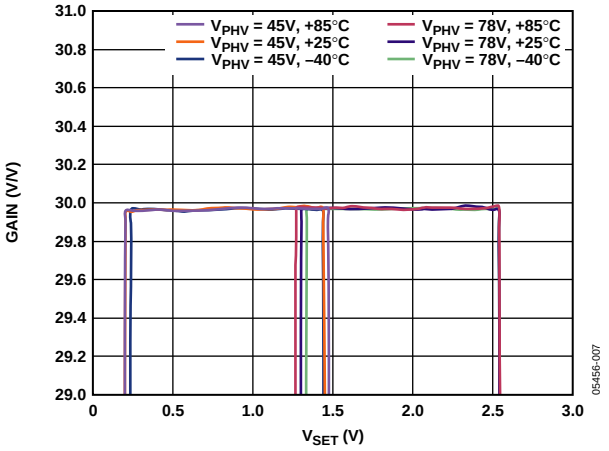



Figure 7. Incremental Gain from $V_{SET}$ to $V_{APD}$ vs. $V_{SET}$ for Multiple Temperatures, $I_{APD}$ = 5 µA, $V_{PHV}$ = 78 V and 45 V

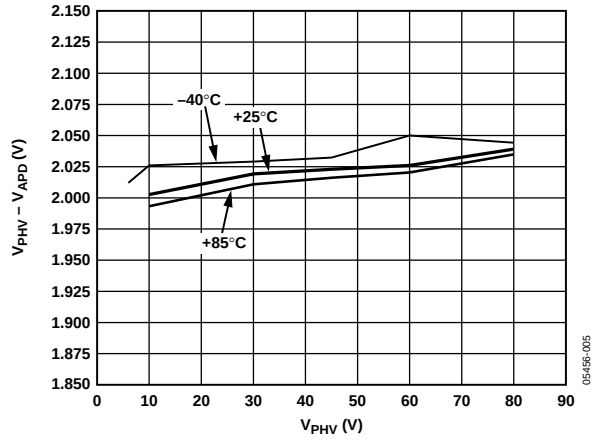



Figure 5. $V_{APD}$ Supply Tracking Offset vs. $V_{PHV}$ for Multiple Temperatures

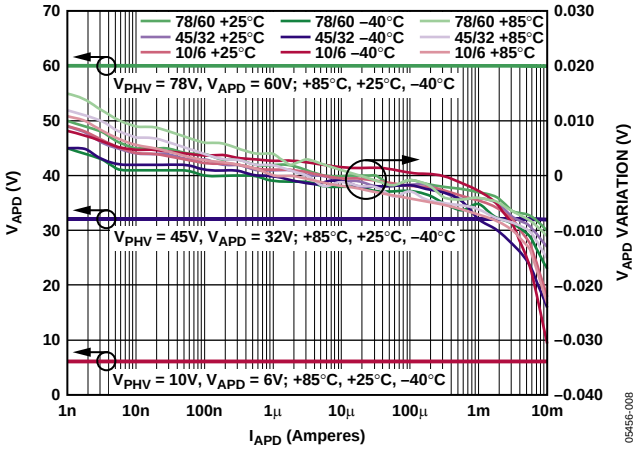



Figure 8. $V_{APD}$ vs. $I_{APD}$ for Multiple Temperatures and Values of $V_{PHV}$ and $V_{APD}$

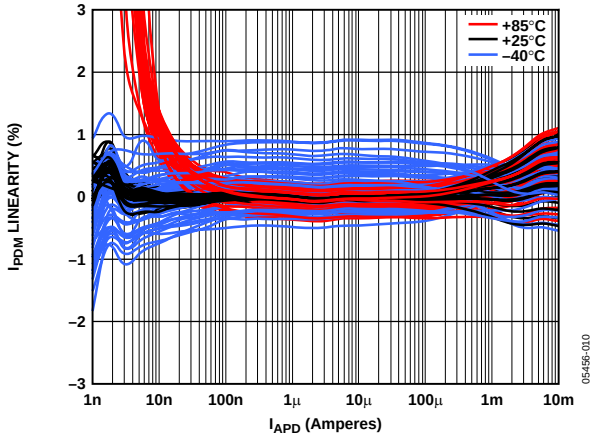



Figure 9. $I_{PDM}$ Linearity for Multiple Temperatures and Devices $V_{PHV}$ =75 V, $V_{APD}$ = 60 V, Normalized to $I_{APD}$ = 5 µA, 25°C

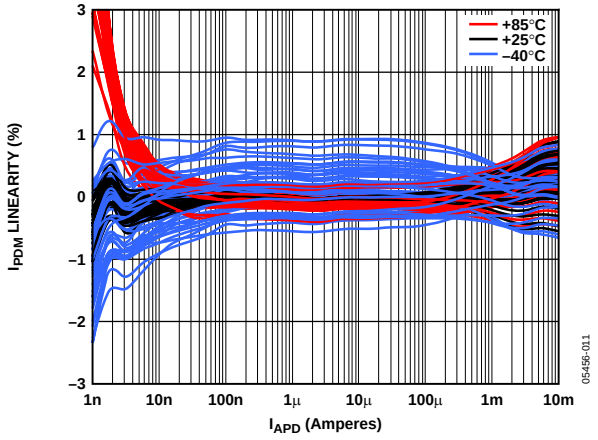



Figure 12. $I_{PDM}$ Linearity for Multiple Temperatures and Devices $V_{PHV}$ = 45 V, $V_{APD}$ = 32 V, Normalized to $I_{APD}$ = 5 µA, 25°C

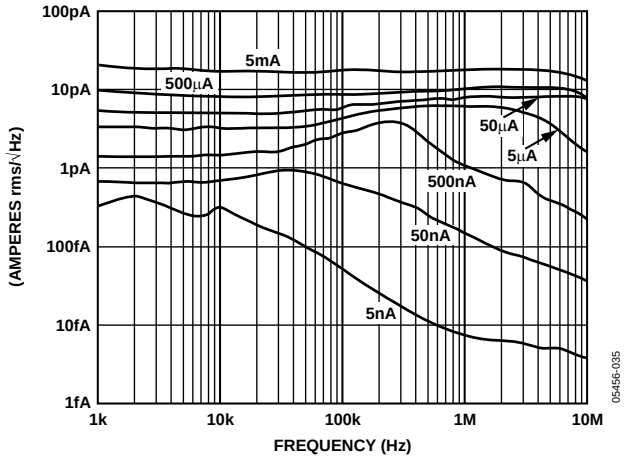



Figure 10. Output Current Noise Density vs. Frequency for Multiple Values of $I_{APD}$, $C_{GARD}$ = 2 nF, $V_{PHV}$ = 40 V, $V_{APD}$ = 30 V

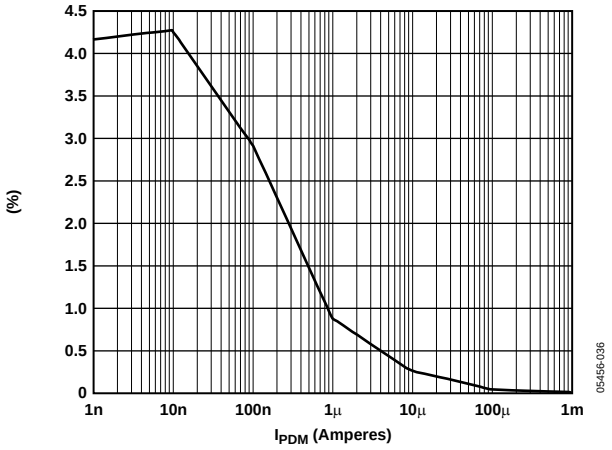



Figure 13. Output Wideband Current Noise as a Percentage of $I_{PDM}$ vs. $I_{PDM}$, $C_{GARD}$ = 2 nF, $V_{PHV}$ = 40 V, $V_{APD}$ = 30 V, BW = 10 MHz

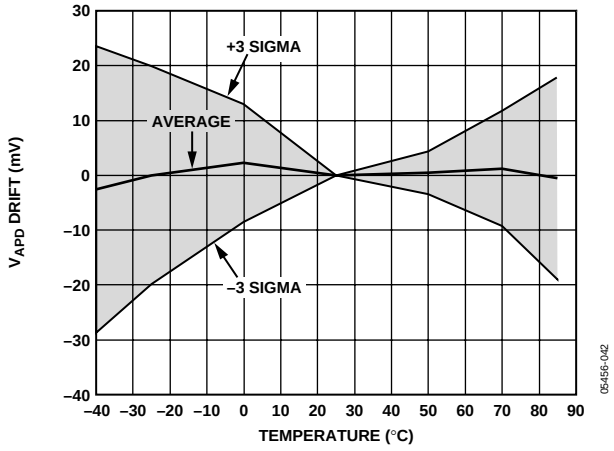



Figure 11. Temperature Drift of $V_{APD}$, 3 σ to Either Side of Mean

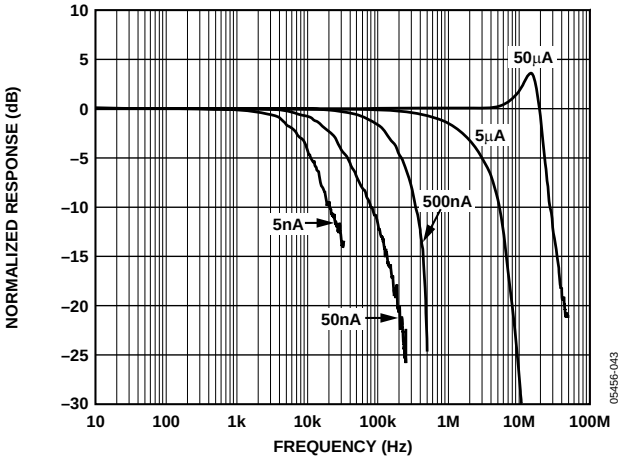



Figure 14. Small Signal AC Response from $I_{APD}$ to $I_{PDM}$, for $I_{APD}$ in Decades from 5 nA to 50 µA, $V_{PHV}$ = 60 V, $V_{APD}$ = 30 V

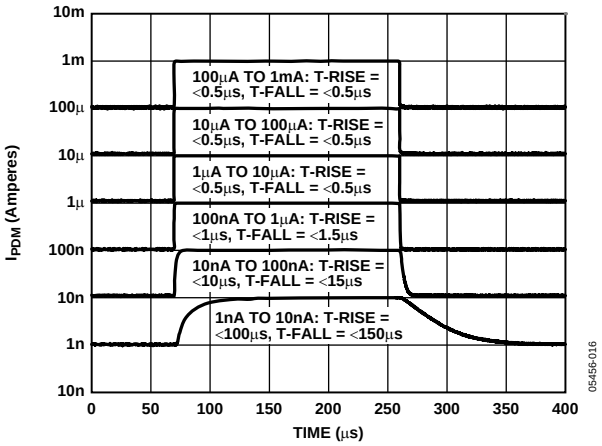



*Figure 15. Pulse Response from $I_{APD}$ to $I_{PDM}$ for $I_{APD}$ in Decades from 5 nA to 5 mA, $V_{PHV}$ = 60 V, $V_{APD}$ = 30 V*

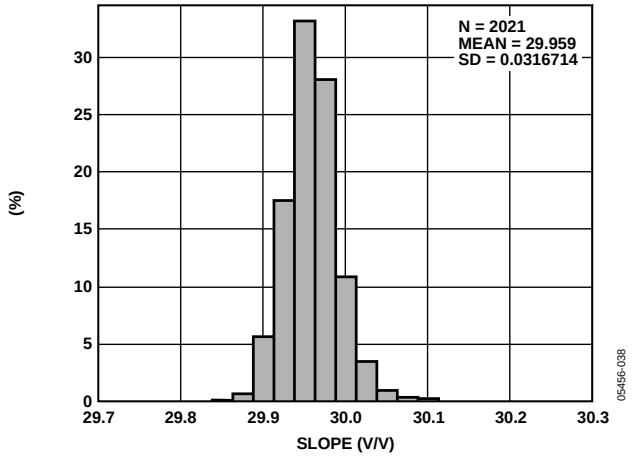



*Figure 16. Distribution of Incremental Gain from $V_{SET}$ to $V_{APD}$ for $V_{SET}$ from 1.5 V to 2.4 V, $I_{APD}$ = 5 µA*

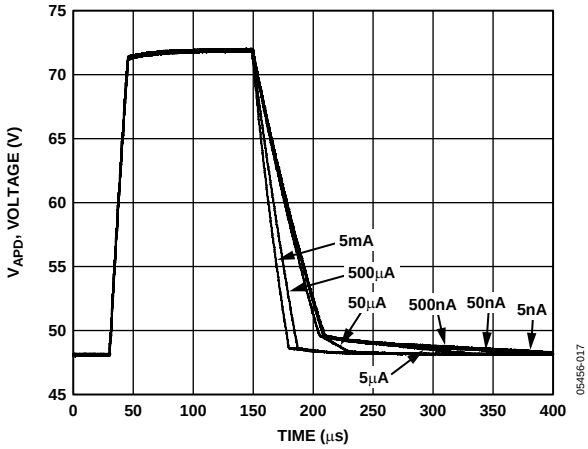



*Figure 17. Pulse Response from $V_{SET}$ to $V_{APD}$ ($V_{SET}$ Pulsed 1.6 V to 2.4 V) for $I_{APD}$ in Decades from 5 nA to 5 mA, $C_{GARD}$ = 2 nF, $V_{PHV}$ = 60 V, $V_{APD}$ = 30 V*

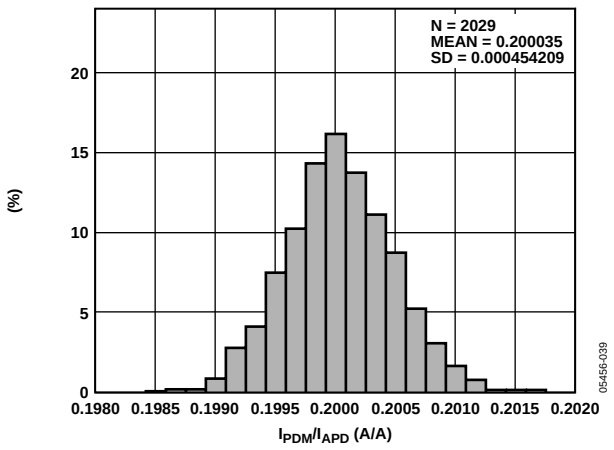



*Figure 18. Distribution of $I_{PDM}/I_{APD}$ at $V_{PHV}$ = 60 V, $V_{SET}$ = 1.0 V, $I_{APD}$ = 50 µA*

# THEORY OF OPERATION

The ADL5317 is designed to address the need for high voltage bias control and precision optical power monitoring in optical systems using avalanche photodiodes. It is optimized for use with the Analog Devices, Inc. family of translinear logarithmic amplifiers that take advantage of the wide input current range of the ADL5317. This arrangement allows the anode of the photodiode to connect directly to a transimpedance amplifier for the extraction of the data stream without need for a separate optical power monitoring tap. Figure 19 shows the basic connections for the ADL5317.

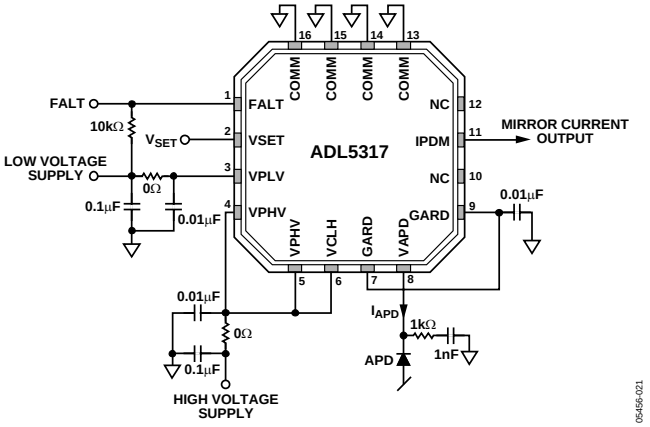



*Figure 19. Basic Connections*

At the heart of the ADL5317 is a precision attenuating current mirror with a voltage following characteristic that provides precision biasing at the monitor input. This architecture uses a JFET-input amplifier to drive the bipolar mirror and maintain stable $V_{APD}$ voltage, while offering very low leakage current at the VAPD pin. The mirror attenuates the current sourced through VAPD by a factor of 5 to limit power dissipation under high voltage operation and delivers the mirrored current to the IPDM monitor output pin. Proprietary mirroring and cascoding techniques maintain the linearity vs. the input current and stability of the mirror ratio over a very wide range of supply and $V_{APD}$ voltages.

## BIAS CONTROL INTERFACE

In the linear operating mode, the voltage at VAPD is referenced to ground, and follows the simplified equation

$$V_{APD} = 30 \times V_{SET}$$

GARD is driven to the same potential as VAPD for use in shielding the highly sensitive VAPD pin from leakage currents. The GARD and VAPD pins are clamped to within approximately 40 V below the VPHV supply to prevent internal device breakdowns, and VAPD is clamped to within a volt of GARD.

The VAPD adjustment range for a given high voltage supply, VPHV, is limited to approximately 33 V (or less, for $V_{PHV}$ < 41 V). For example, VAPD is specified from 40 V to 73.5 V for a 75 V supply, and 6 V (the minimum allowed) to 28.5 V for a 30 V supply. When VAPD is driven to its lower clamp voltage via the VSET pin, the mirror can continue to operate, but the VAPD bias voltage no longer responds to incremental changes in $V_{SET}$.

## GARD INTERFACE

The GARD pins primarily shield the VAPD trace from leakage currents and filter noise from the bias control interface. GARD is driven by the $V_{SET}$ amplifier through a 20 kΩ resistor. This resistor forms an RC network with an external capacitor from GARD to ground that filters the thermal noise of the amplifier's feedback network and provides additional power supply rejection. The series components, $R_{COMP}$ and $C_{COMP}$, shown in Figure 20, are necessary to ensure essential high frequency compensation at the VAPD input pin over the full operating range of the ADL5317.

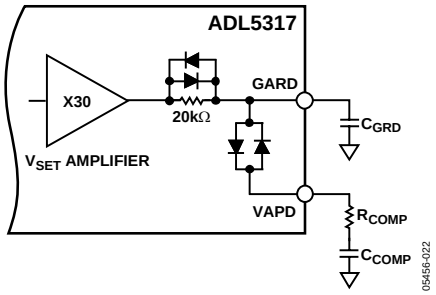



*Figure 20. Filtering VAPD Using the GARD Interface*

The cutoff frequency of the GARD interface for small signals and noise is defined by

$$F_{3dB} = \frac{1}{2\pi \times 20\,\text{k}\Omega \times C_{GRD}}$$

where:

$F_{3dB}$ is the cutoff frequency of the low-pass filter formed by the on-board 20 kΩ and $C_{GRD}$.
$C_{GRD}$ is the filter capacitor installed from GARD to ground.

A larger value for $C_{GRD}$ (up to approximately 0.01 µF) provides superior noise performance at the lowest input current levels, but also slows the response time to changes in $V_{SET}$.

The pull-up of the $V_{SET}$ amplifier is limited to approximately 2.5 mA, resulting in a slew limited region for large signals, followed by an RC decay for the final 700 mV. This decay corresponds to the above single-pole equation. The pull-down of the $V_{SET}$ amplifier is largely resistive, equivalent to approximately 90 kΩ in parallel with 70 µA to ground.

For small input currents, this pull-down must discharge not only $C_{GRD}$ but also $C_{COMP}$ at the VAPD pin (through the GARD and VAPD diodes). The final 700 mV of settling for lower input currents is dominated by the input current discharge of $C_{COMP}$. For larger input currents, the $V_{SET}$ amplifier pull-down discharges only $C_{GRD}$, since $I_{APD}$ is capable of discharging $C_{COMP}$ quickly (see Figure 17).

Any dc load on GARD alters the gain from VSET to VAPD due to the 20 kΩ source impedance. Note that the load presented by a multimeter or oscilloscope probe is sufficient to alter the VSET to VAPD gain, and must be taken into account.

The GARD pin is internally clamped to approximately 40 V below VPHV to prevent device breakdown, and VAPD is clamped to within 1 V of GARD. For this reason, any short-circuit to ground from GARD or VAPD must be avoided for VPHV voltages above 36 V, or device damage results.

## VCLH INTERFACE

The voltage clamp high-side pin (VCLH) is typically connected to VPHV for linear operation of the VSET interface and left open for supply tracking mode (see the Supply Tracking Mode section for more details). The voltage at VCLH represents a high-side clamp above which the $V_{SET}$ amplifier output (and $V_{APD}$) is not allowed to rise. The voltage is internally set to a temperature stable 2.0 V below $V_{PHV}$ through a 25 kΩ resistor.

When $V_{SET}$ is pulled up to 3 V or higher and VCLH is open, VAPD follows 2.0 V below VPHV as VPHV is varied. This bypasses the linear VSET interface for applications where an adjustable high voltage supply is preferred (see the Applications section). The 25 kΩ source resistance allows VCLH to be shorted to VPHV, removing the 2.0 V high-side clamp for extended linear operating range (up to $V_{PHV}$ − 1.5 V) in linear mode. VCLH can be left open in linear mode if a fixed clamp point is desired.

## NOISE PERFORMANCE

The noise performance for the ADL5317, defined as the rms noise current as a fraction of the output dc current, improves with increasing signal current. This partially results from the relationship between quiescent collector current and shot noise in bipolar transistors. At lower signal current levels, the noise contribution from the $V_{SET}$ amplifier and other noise sources appearing at VAPD dominate the noise behavior. Filtering the VSET interface noise through an external capacitor from GARD to ground, as well as selecting optimal external compensation components on VAPD, minimizes the amount of voltage noise at VAPD that is converted to current noise at IPDM.

## RESPONSE TIME

The response time for changes in signal current is fundamentally a function of signal current, with small-signal bandwidth increasing roughly in proportion to signal current. The value of the external compensating capacitor on VAPD strongly affects response time, although the value must be chosen to maintain stability and prevent noise peaking. Response time for changes in $V_{SET}$ voltage is primarily a function of the filter capacitance at the GARD pin. See the GARD Interface section for further details.

Figure 15 and Figure 17 show the response of the ADL5317 to pulsed input current and $V_{SET}$ voltage, respectively.

## DEVICE PROTECTION

Thermal and overcurrent protection are provided with fault detection. The FALT pin is an open collector logic output (active low) designed to assert when an overtemperature or overcurrent condition is detected. A pull-up resistor to an appropriate logic supply is required, and its value should be chosen such that no more than 1 mA output current is used when active.

When the die temperature of the ADL5317 exceeds 140°C (typical), the current mirror shuts down, causing the bias voltage at VAPD to be pulled down, and FALT asserts. FALT remains asserted until the temperature falls below the trigger temperature minus the thermal hysteresis (20°C typical), after which the mirror and biaser again power up. The cycle may repeat until the cause of the fault is removed.

When the input current, $I_{APD}$, exceeds 18 mA (typical), the current mirror and biaser attempt to maintain the threshold current by allowing the $V_{APD}$ voltage to fall to a point of equilibrium. In other words, the threshold current represents the compliance of the bias voltage; in this case, the current at which $V_{APD}$ falls 500 mV below its midrange current value. FALT asserts, but is not guaranteed to remain asserted, as VAPD is pulled down toward ground. If $V_{APD}$ falls below ~3 V, as in the case of a momentary short-circuit or being driven by a programmable current source exceeding the threshold current, bias current generators critical to device operation become saturated. This causes FALT to deassert and the mirror to shut down. The mirror does not power up until the input current falls below the current limit of the $V_{SET}$ amplifier (approximately 2.5 mA), allowing VAPD to be pulled up to its normal operating level. The FALT pin can be grounded if the logic signal is not used.

# APPLICATIONS

The ADL5317 is primarily designed for wide dynamic range applications simplifying APD bias circuit architecture. Accurate control of the bias voltage across the APD becomes critical to maintain the proper avalanche multiplication factor as the temperature and input power vary. Figure 21 shows how to use the ADL5317 with an external temperature sensor to monitor the ambient temperature of the APD. Using a look-up table and DAC to drive VSET, it is possible to apply the correct $V_{APD}$ for the conditions. Note that Pin 9, Pin 10, and Pin 12 to Pin 15 were removed for simplification.

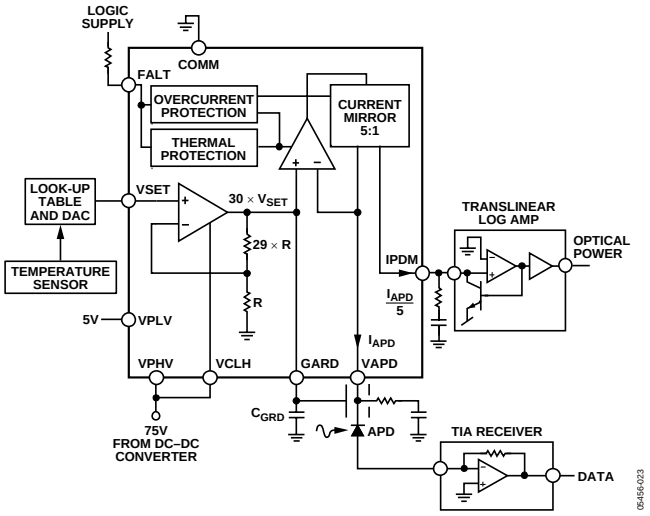



*Figure 21. Typical APD Biasing Application Using the ADL5317*

In this application, the ADL5317 is operating in linear mode. The bias voltage to the APD, delivered at Pin VAPD, is controlled by the voltage ($V_{SET}$) at Pin VSET. The bias voltage at VAPD is equal to 30 × $V_{SET}$.

The range of voltages available at VAPD for a given high voltage supply is limited to approximately 33 V (or less, for $V_{APD}$ < 41 V). This is because the GARD and VAPD pins are clamped to within ~40 V below VPHV, preventing internal device breakdowns.

The input current, $I_{APD}$, is divided down by a factor of 5 and precisely mirrored to Pin IPDM. This interface is optimized for use with any of the Analog Devices translinear logarithmic amplifiers (for example, the AD8304 or AD8305) to offer a precise, wide dynamic range measurement of the optical power incident upon the APD.

If a voltage output is preferred at IPDM, a single external resistor to ground is all that is necessary to perform the conversion. Voltage compliance at IPDM is limited to $V_{PLV}$ or $V_{APD}/3$, whichever is lower.

## SUPPLY TRACKING MODE

Some applications for the ADL5317 require a variable dc-to-dc converter or alternative variable biasing sources to supply VPHV. For these applications, it is necessary to configure the ADL5317 for supply tracking mode, shown in Figure 22. In this mode, the VSET interface is bypassed. However, the full functionality of the precision current mirror remains available.

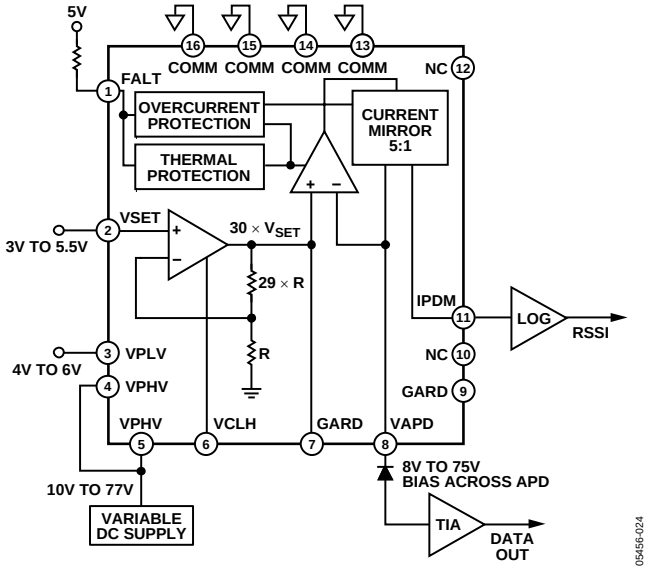



*Figure 22. Supply Tracking Mode*

In supply tracking mode, the $V_{SET}$ amplifier is pulled up beyond its linear operating range and effectively placed into a controlled saturation. This is done by applying 3.0 V to 5.5 V at the VSET pin. It is also necessary to remove the connection from VCLH, which defines the saturation point, to VPHV. Once the ADL5317 is placed into supply tracking mode, $V_{APD}$ is clamped to 2.0 V below $V_{PHV}$.

For those designs where it is desirable to drive VSET from the VPLV supply, it is necessary to place a 100 kΩ resistor between VSET and VPLV for $V_{PLV}$ > 5.5 V. This is due to input current limitations on the VSET pin.

## TRANSLINEAR LOG AMP INTERFACING

The monitor current output, IPDM, of the ADL5317 is designed to interface directly to an Analog Devices translinear logarithmic amplifier, such as the AD8304, AD8305, or ADL5306. Figure 23 shows the basic connections necessary for interfacing the ADL5317 to the AD8305. In this configuration, the designer is can use the full current mirror range of the ADL5317 for high accuracy power monitoring.

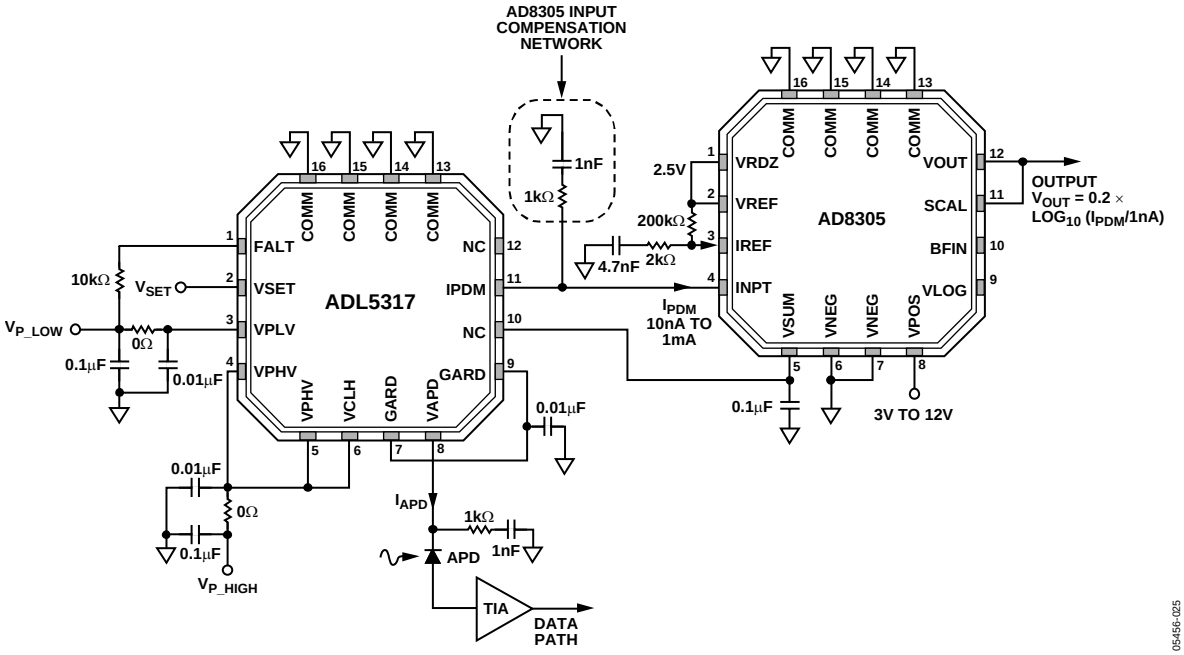



*Figure 23. Interfacing the ADL5317 to the AD8305 for High Accuracy APD Power Monitoring*

Measured rms noise voltage at the output of the AD8305 vs. input current is shown in Figure 24 for the AD8305 by itself and in cascade with the ADL5317. The relatively low noise produced by the ADL5317, combined with the additional noise filtering inherent in the frequency response characteristics of the AD8305, result in minimal degradation to the noise performance of the AD8305.

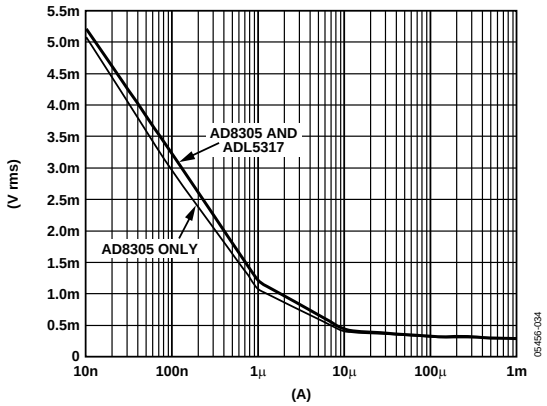



*Figure 24. Measured RMS Noise of AD8305 vs. AD8305 Cascaded with ADL5317*

## CHARACTERIZATION METHODS

During characterization, the ADL5317 was treated as a high voltage 5:1 precision current mirror. To make accurate measurements throughout the entire current range, calibrated Keithley 236 current sources were used to create and measure the test currents. Measurements at low current and high voltage are very susceptible to leakage to the ground plane.

To minimize leakage on the characterization board, the guard pins are connected to traces that buffer VAPD and IPDM from ground. The triax guard connector is also connected to the GARD pin of the device to provide buffering along the cabling.

Figure 25 shows the primary characterization setup. The data gathered is used directly, or with calculation, for all the static measurements, including mirror error between IAPD and IPDM , supply tracking offset, incremental gain, and VAPD vs. IAPD. Component selection is very similar to that of the evaluation board, except that triax connectors are used in place of the SMA connectors. To measure the pulse response, output noise, and bandwidth measurements, more specialized test setups are used.

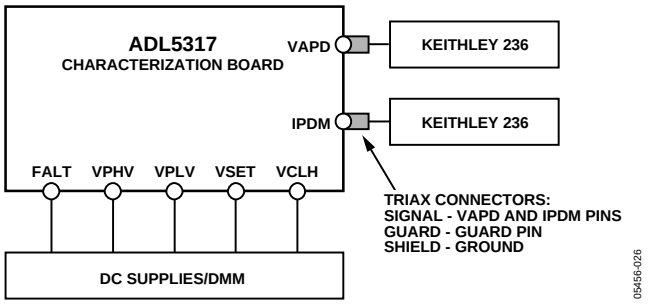



*Figure 25. Primary Characterization Setup*

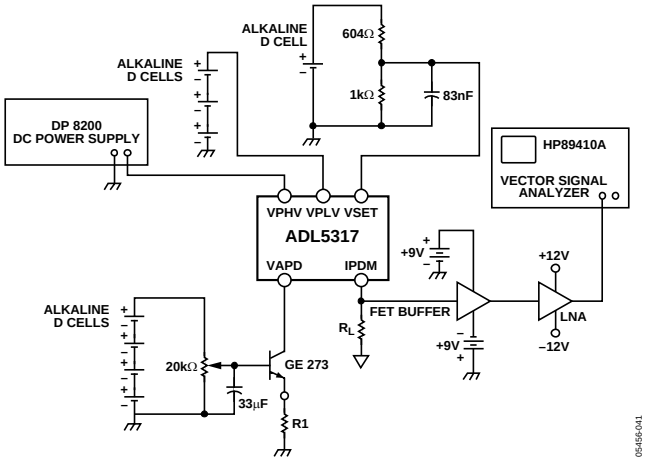



Figure 26. Configuration for Noise Spectral Density and Wideband Current Noise

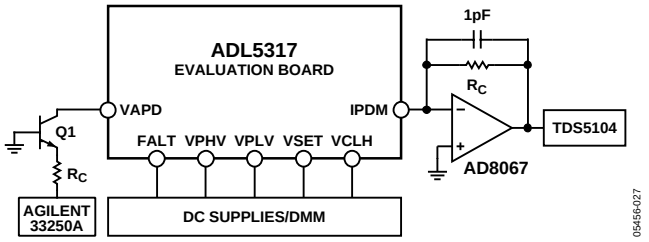



Figure 27. Configuration for Pulse Response from $I_{APD}$ to $I_{PDM}$

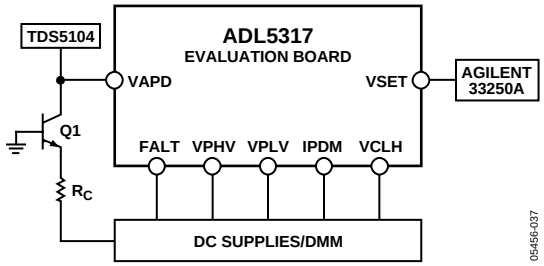



Figure 28. Configuration for Pulse Response from $V_{SET}$ to $V_{APD}$

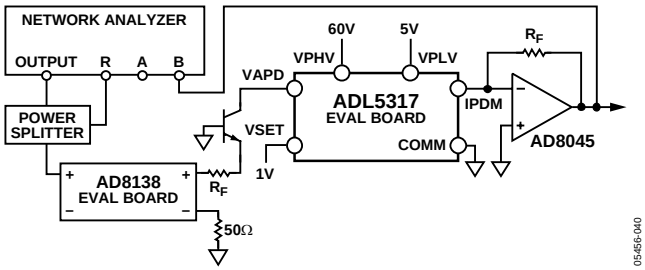



Figure 29. Configuration for Small Signal AC Response

The setup in Figure 26 is used to measure the output current noise of the ADL5317. Batteries are used in numerous places to minimize introduced noise and remove the uncertainty resulting from the use of multiple dc supplies. In application, properly bypassed dc supplies provide similar results. The load resistor is chosen for each current to maximize signal-to-noise ratio while maintaining measurement system bandwidth (when combined with the low capacitance JFET buffer). The custom LNA is used to overcome noise floor limitations in the HP89410A signal analyzer.

Figure 27 shows the configuration used to measure the $I_{APD}$ pulse response. To create the test current pulse, Q1 is used in a common base configuration with the Agilent 33250A, generating a negative biased square wave with an amplitude that results in a one decade current step on IPDM.

$R_C$ is chosen according to what current range is desired. Only one cable is used between the Agilent 33250A and $R_C$, while everything else is connected with SMA connectors. A FET scope probe connects the output of the AD8067 to the TDS5104 input.

The configuration in Figure 28 is used to measure $V_{APD}$ while $V_{SET}$ is pulsed. Q1 and $R_C$ are used to generate the operating current on the VAPD pin. An Agilent 33250A pulse generator is used on the VSET pin to create a 1.6 V to 2.4 V square wave. The capacitance on the GARD pin is 2 nF for this test.

The setup in Figure 29 is used to measure the frequency response from $I_{APD}$ to $I_{PDM}$. The AD8138 differential op amp delivers a −1.250 V dc offset to bias the NPN transistor and to have a 500 mV drop across $R_F$. This voltage is modulated to a depth of 5% of full scale over frequency. The voltage across $R_F$ sets the dc operating point of $I_{APD}$. $R_F$ values are chosen to result in decade changes in $I_{APD}$. The output current at the IPDM pin is fed into an AD8045 op amp configured to operate as a transimpedance amplifier. The Feedback Resistor, $R_F$, is the same value as that on the output of the AD8138. Note that any noise at the VSET input is amplified by the ADL5317 with a gain of 30. This noise shows up on VAPD and causes errors when measuring nanoamp current levels. This noise can be filtered by use of the GARD pin. See the GARD Interface section for more details.

# EVALUATION BOARD

**Table 4. Evaluation Board Configuration Options**

| Component | Function | Default Condition |
|---|---|---|
| VPHV, VPLV, GND | High and Low Voltage Supply and Ground Pins. | Not Applicable |
| VSET | APD Bias Voltage Setting Pin. The dc voltage applied to VSET determines the APD bias voltage at VAPD. $V_{APD} = 30 \times V_{SET}$. | Not Applicable |
| R11, C8 | APD Input Compensation. Provides essential high frequency compensation at the VAPD input pin. | C8 = 1 nF (size 0603)<br>R11 = 1 kΩ (size 0603) |
| VAPD, L1, C9 | Input Interface. The evaluation board is configured to accept an input current at the SMA connector labeled VAPD. Filtering of this current can be done using L1 and C9. | L1 = 0 Ω (size 0805)<br>C9 = open (size 0805) |
| IPDM, R1 | Mirror Interface. The output current at the SMA connector labeled IPDM is 1/5 the value at VAPD. R1 allows a resistor to be installed for applications where a scaled voltage referenced to $I_{APD}$ instead of a current is desirable. | R1 = open (size 1206) |
| R7, R8, R9, R10, C6, C7, C10 | Guard Options. By populating R9 and/or R10, the shell of the VAPD SMA connector is set to the GARD potential. R7 and R8 are installed so that the guard potential can be driven by an external source, such as the VSUM potential of the Analog Devices optical log amps. C7 filters noise from the VSET interface and provides a high frequency ac path to ground. Additional filtering is possible by installing a capacitor at C10. C10 should equal C7. | R7 = R8 = 0 Ω (size 0402)<br>R9 = R10 = open (size 0402)<br>C7 = 0.01 µF (size 0805)<br>C6 = C10 = open (size 0402) |
| VPLV, W1, W2, R3 | Optional Supply Tracking Mode. Connecting Jumper W2 and opening Jumper W1 places the ADL5317 into supply tracking mode. In this mode, the voltage at VAPD is typically 2 V below $V_{PHV}$. R3 = 100 kΩ for $V_{PLV} > 5.5$ V. | R3 = 0 Ω (size 0402)<br>W1 = open<br>W2 = closed |
| VCLH, W1, C4, R6 | Extended Linear Operating Range. Closing W1 connects Pin VPHV and Pin VCLH. This allows for an extended linear control range of $V_{APD}$ using $V_{SET}$. | W1 = closed<br>C4 = open (size 0805)<br>R6 = 0 Ω (size 0402) |
| FALT, R2 | FALT Interface. R2 is a resistive pull-up that is used to create the logic signal at FALT. | R2 = 10 kΩ (size 0603) |
| C1, C2, C3, C5, R4, R5 | Supply Filtering/Decoupling. | C1 = C2 = 0.01 µF (size 0402)<br>C3 = 0.1 µF (size 0603)<br>C5 = 0.1 µF (size 1206)<br>R4 = R5 = 0 Ω (size 0402) |

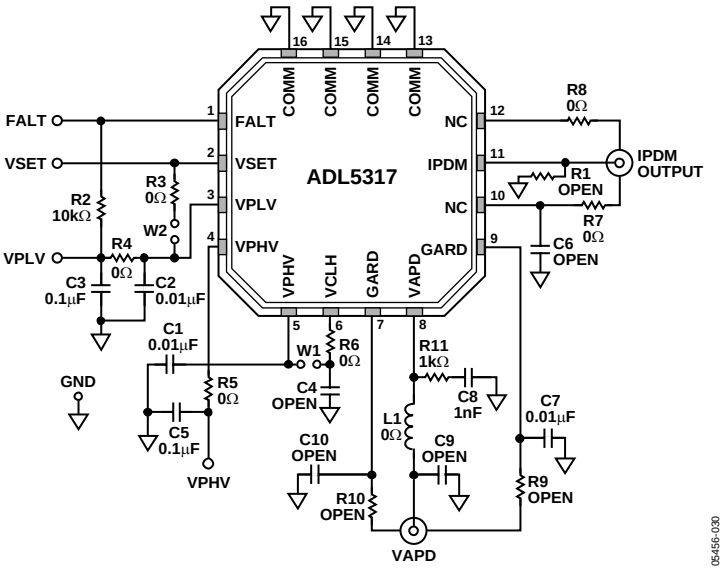



*Figure 30. ADL5317 Evaluation Board Schematic*

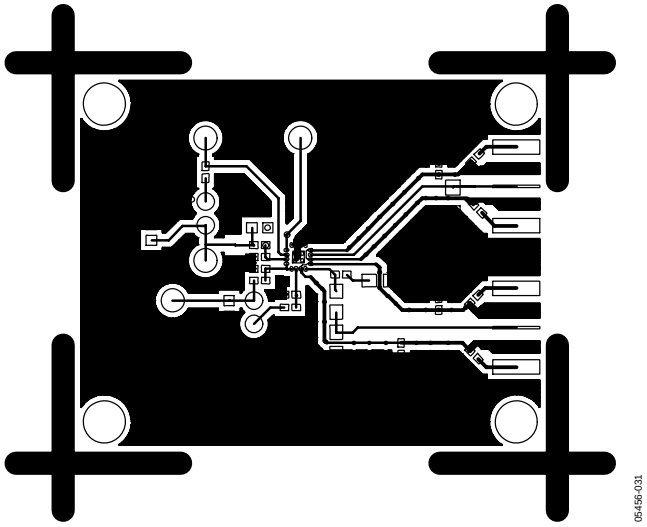



*Figure 31. ADL5317 Evaluation Board Layout*

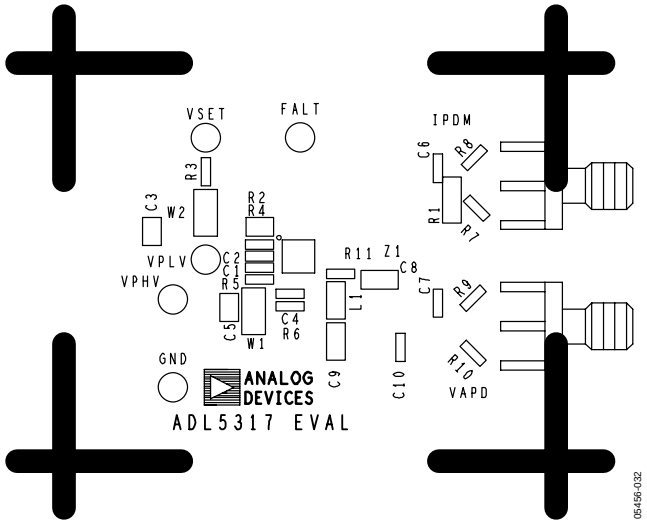
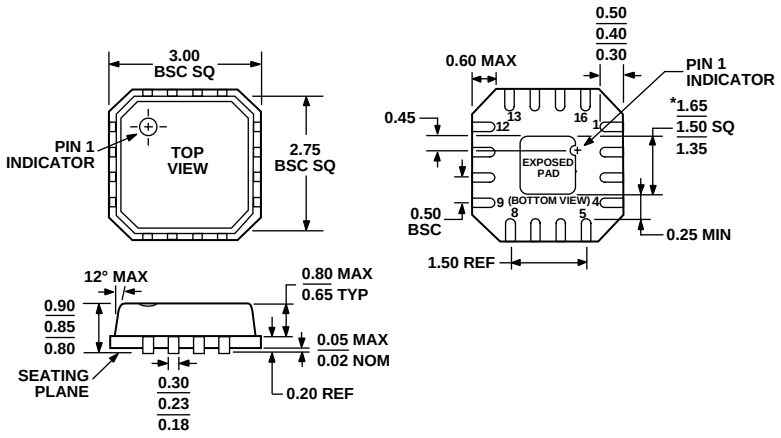



*Figure 32. ADL5317 Evaluation Board Silkscreen*

# OUTLINE DIMENSIONS




*COMPLIANT TO JEDEC STANDARDS MO-220-VEED-2
EXCEPT FOR EXPOSED PAD DIMENSION.

*Figure 33. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]*
*3 mm x 3 mm Body, Very Thin Quad*
*(CP-16-3)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option | Branding |
|---|---|---|---|---|
| ADL5317ACPZ-REEL7[1] | –40°C to +85°C | 16-Lead Lead Frame Chip Scale Package (LFCSP_VQ) | CP-16-3 | R00 |
| ADL5317ACPZ-WP[1] | –40°C to +85°C | 16-Lead Lead Frame Chip Scale Package (LFCSP_VQ) | CP-16-3 | R00 |
| ADL5317-EVAL | | Evaluation Board | | R00 |

[1] Z = Pb-free part.


D05456-0-7/05(0)