Dual-Loop, 50 Mbps to 2.7 Gbps Laser Diode Driver

Data Sheet

ADN2841

FEATURES

- 50 Mbps to 2.7 Gbps operation
- Typical rise/fall time: 80 ps
- Bias current range: 2 mA to 100 mA
- Modulation current range: 5 mA to 80 mA
- Monitor photodiode current: 50 µA to 1200 µA
- Closed-loop control of power and extinction ratio
- Laser fail and laser degrade alarms
- Automatic laser shutdown (ALS)
- Dual MPD functionality for DWDM
- Optional clocked data
- Full current parameter monitoring
- 5 V operation
- 48-lead LFCSP
- 32-lead LFCSP (reduced functionality)

APPLICATIONS

- DWDM dual MPD wavelength fixing
- SONET OC-1/3/12/48
- SDH STM-1/4/16
- Fibre Channel
- Gigabit Ethernet

GENERAL DESCRIPTION

The ADN2841 uses a unique control algorithm to control both the average power and extinction ratio of the laser diode (LD) after initial factory setup. Because power and extinction ratio control are fully integrated, external component count is low and PCB area is small. Programmable alarms are provided for laser fail (end of life) and laser degrade (impending fail).

The ADN2841 has circuitry for a second monitor photodiode, which enables DWDM wavelength control.

FUNCTIONAL BLOCK DIAGRAM

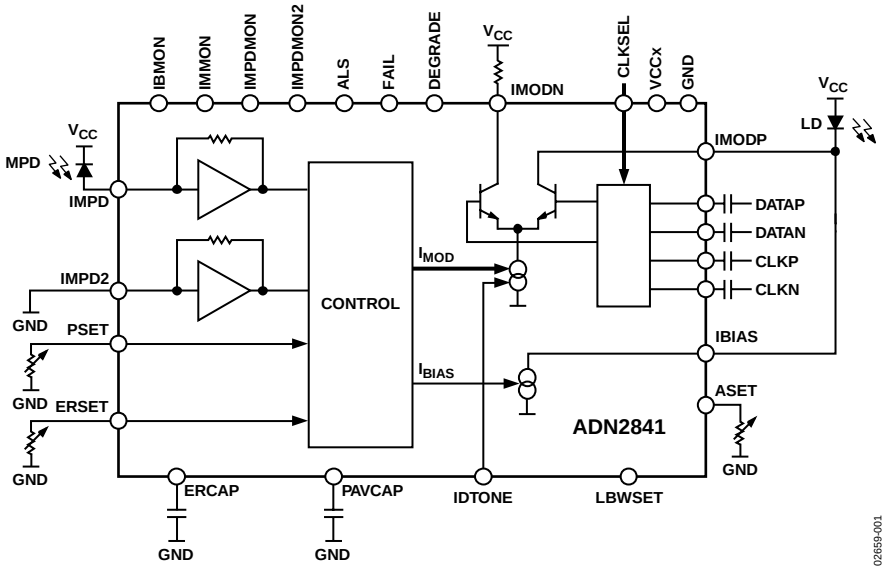

Figure 1.

Document Feedback

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Tel: 781.329.4700
Technical Support www.analog.com

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Last Content Update: 08/30/2016

Comparable Parts

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Evaluation Kits

- ADN2841 Evaluation Board

Documentation

Application Notes

- AN-629: ADN2841 Evaluation Kit
- AN-630: ADN2841 Optical Evaluation Kit
- AN-631: ADN2841/ADN2847 DC-Coupled Optical Evaluation Kit
- AN-658: Optical Channel Identification on the ADN284x Laser Drivers (Part I)

Data Sheet

- ADN2841: Dual-Loop, 50 Mbps to 2.7 Gbps Laser Diode Driver Data Sheet

Reference Materials

Analog Dialogue

- Single-Chip Digitally Controlled Data-Acquisition as Core of Reliable DWDM Communication Systems

Informational

- Optical and High Speed Networking ICs

Technical Articles

- Dual-Loop Laser Drivers Bring Robustness To Optical Networks

Design Resources

- ADN2841 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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9/13—Rev. A to Rev. B

Updated Format ... Universal
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Added Typical Performance Characteristics Section; moved Figure 5 and Figure 6 ... 8
Updated Outline Dimensions ... 15
Changes to Ordering Guide ... 16

8/02—Rev. 0 to Rev. A

Replaced Figure 8 ... 10
Updated Outline Dimensions ... 11

10/01—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 5 V ± 10%. All specifications T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are specified at 25°C.

Table 1.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
LASER BIAS (BIAS)					
Current, I_{BIAS}	2		100	mA	
Compliance Voltage	1.2		V_{CC}	V	
I_{BIAS} During ALS			0.1	mA	
ALS Response Time		10		µs	
CCBIAS Compliance Voltage		1.2		V	
MODULATION CURRENT (IMODP, IMODN)					
Output Current, I_{MOD}	5		80	mA	
Compliance Voltage	1.8		V_{CC}	V	
I_{MOD} During ALS			0.1	mA	
Rise Time		80	120	ps	
Fall Time		80	120	ps	
Jitter			20	ps p-p	
Pulse Width Distortion		18		ps	
MONITOR PD (MPD, MPD2)					
Input Current	50		1200	µA	Average current
Voltage			1.6	V	
POWER SET INPUT (PSET PIN)					
Capacitance			80	pF	
Input Current	50		1200	µA	Average current
Voltage	1.15	1.23	1.35	V	
EXTINCTION RATIO SET INPUT (ERSET PIN)					
Allowable Resistance Range	1.2		25	kΩ	
Voltage	1.15	1.23	1.35	V	
ALARM SET (ASET PIN)					
Allowable Resistance Range	1.2		25	kΩ	
Voltage	1.15	1.23	1.35	V	
Hysteresis		5		%	
CONTROL LOOP					
Time Constant		0.22		sec	LBWSET = GND
		2.25		sec	LBWSET = V_{CC}
DATA INPUTS (DATAP, DATAN, CLKP, CLKN PINS)					
AC-Coupled[2]					
V p-p (Single-Ended Peak-to-Peak)	100		500	mV	
Input Impedance		50		Ω	
t_{SETUP}[3]	150	95		ps	
t_{HOLD}[3]	0	–70		ps	
LOGIC INPUTS (ALS, LBWSET, CLKSEL PINS)					
V_{IH}	2.4			V	
V_{IL}			0.8	V	
ALARM OUTPUTS					Internal 30 kΩ pull-up
V_{OH}	2.4			V	
V_{OL}			0.8	V	
IDTONE PIN					User to supply current sink in the range of 50 µA to 4 mA
Compliance Voltage			V_{CC} – 1.5	V	
I_{OUT}/I_{IN} Ratio		2			
f_{IN}[4]	0.01		1	MHz	

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
IBMON, IMMON, IMPDMON, IMPDMON2 PINS					
IBMON, IMMON Division Ratio		100		A/A	I_{BIAS} current/I_{MOD} current
IMPDMON, IMPDMON2 Division Ratio		1		A/A	I_{MPD} current/I_{MPD2} current
IMPDMON to IMPDMON2 Matching			1	%	I_{MPD} = 1200 µA
Compliance Voltage	0		V_{CC} − 1.2	V	
SUPPLY					
I_{CC}[5]		0.05		A	I_{BIAS} = I_{MOD} = 0 A
V_{CC}[6]	4.5	5.0	5.5	V	

[1] Temperature range: −40°C to +85°C.
[2] When the voltage on DATAP is greater than the voltage on DATAN, the modulation current flows in the IMODP pin.
[3] Guaranteed by design and characterization. Not production tested.
[4] IDTONE may cause eye distortion.
[5] I_{CC} for power calculation is the typical I_{CC} given.
[6] All VCCx pins should be shorted together.

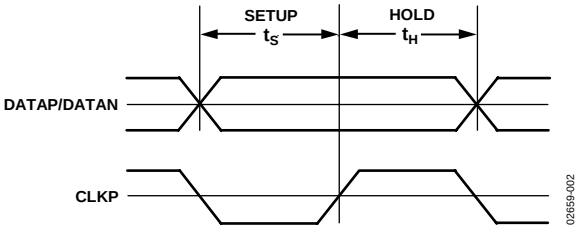


Figure 2. Setup and Hold Time

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter[1]	Rating
V_{CC} to GND	7 V
Operating Temperature Range	
Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature ($T_{J\,MAX}$)	150°C
Power Dissipation	$(T_{J\,MAX} - T_A)/\theta_{JA}$ mW

[1] Transient currents of up to 100 mA will not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered onto a 4-layer circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
48-Lead LFCSP	25	°C/W
32-Lead LFCSP	32	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

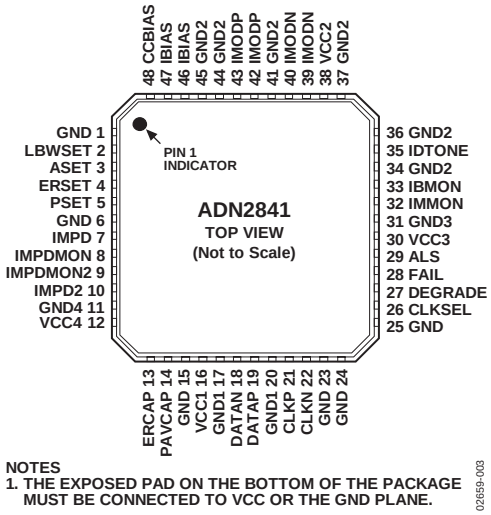


Figure 3. Pin Configuration, 48-Lead LFCSP

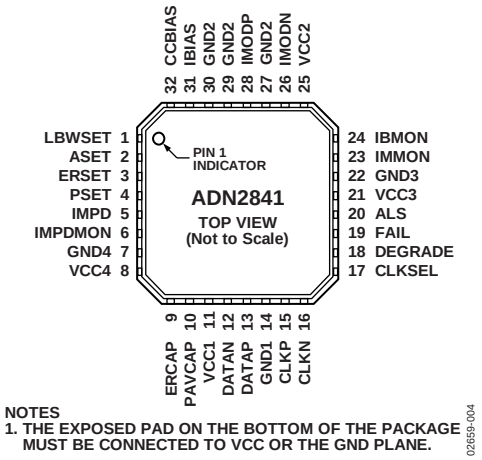


Figure 4. Pin Configuration, 32-Lead LFCSP

Table 4. Pin Function Descriptions

Pin No.			
48-Lead LFCSP	**32-Lead LFCSP**	**Mnemonic**	**Description**
1		GND	Supply Ground.
2	1	LBWSET	Select Low Loop Bandwidth (Active = V_{CC}).
3	2	ASET	Alarm Current Threshold Set Pin.
4	3	ERSET	Extinction Ratio Set Pin.
5	4	PSET	Average Optical Power Set Pin.
6		GND	Ground.
7	5	IMPD	Monitor Photodiode Input.
8	6	IMPDMON	Mirrored Current from Monitor Photodiode.
9		IMPDMON2	Mirrored Current from Monitor Photodiode 2. For use with two MPDs.
10		IMPD2	Monitor Photodiode Input 2. For use with two MPDs.
11	7	GND4	Supply Ground.
12	8	VCC4	Supply Voltage.
13	9	ERCAP	Extinction Ratio Loop Capacitor.
14	10	PAVCAP	Average Power Loop Capacitor.
15		GND	Ground.
16	11	VCC1	Supply Voltage.
17		GND1	Supply Ground.
18	12	DATAN	Data, Negative Differential Terminal.
19	13	DATAP	Data, Positive Differential Terminal.
20	14	GND1	Supply Ground.
21	15	CLKP	Data Clock, Positive Differential Terminal. Used if CLKSEL = V_{CC}.
22	16	CLKN	Data Clock, Negative Differential Terminal. Used if CLKSEL = V_{CC}.
23		GND	Ground.
24		GND	Ground.
25		GND	Ground.
26	17	CLKSEL	Clock Select (Active = V_{CC}). Used if data is clocked into the chip.
27	18	DEGRADE	Degrade Alarm Output.
28	19	FAIL	Fail Alarm Output.
29	20	ALS	Automatic Laser Shutdown.
30	21	VCC3	Supply Voltage.

Pin No.			
48-Lead LFCSP	32-Lead LFCSP	Mnemonic	Description
31	22	GND3	Supply Ground.
32	23	IMMON	Modulation Current Mirror Output.
33	24	IBMON	Bias Current Mirror Output.
34		GND2	Supply Ground.
35		IDTONE	IDTONE. Requires external current sink to ground.
36		GND2	Supply Ground.
37		GND2	Supply Ground.
38	25	VCC2	Supply Voltage.
39	26	IMODN	Modulation Current Negative Output. Connect to 25 Ω.
40		IMODN	Modulation Current Negative Output. Connect to 25 Ω.
41	27	GND2	Supply Ground.
42	28	IMODP	Modulation Current Positive Output. Connect to laser diode.
43		IMODP	Modulation Current Positive Output. Connect to laser diode.
44	29	GND2	Supply Ground.
45	30	GND2	Supply Ground.
46	31	IBIAS	Laser Diode Bias Current.
47		IBIAS	Laser Diode Bias Current.
48	32	CCBIAS	Extra Laser Diode Bias When AC-Coupled.
EP	EP	Exposed Pad	The exposed pad on the bottom of the package must be connected to VCC or the GND plane.

TYPICAL PERFORMANCE CHARACTERISTICS

Average power = −3 dBm, extinction ratio = 9.5 dB; eye diagrams obtained using a Mitsubishi FU-445SDF.

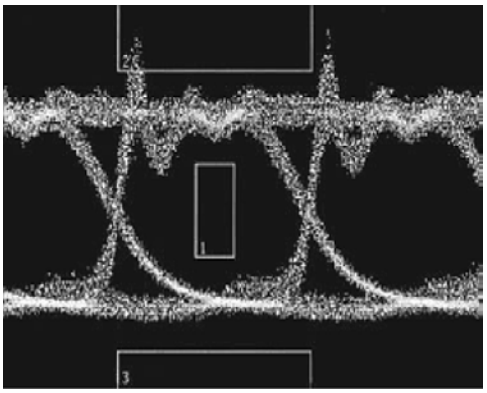


Figure 5. Unfiltered 2.5 Gbps Optical Eye

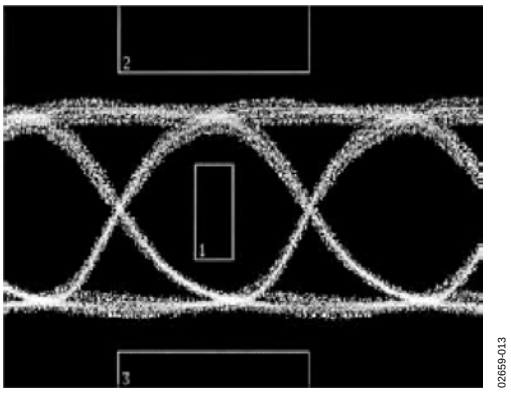


Figure 6. Filtered 2.5 Gbps Optical Eye

THEORY OF OPERATION

Laser diodes have current-in to light-out transfer functions as shown in Figure 7. Two key characteristics of this transfer function are the threshold current, I_{TH}, and the slope in the linear region beyond the threshold current, referred to as slope efficiency, LI.

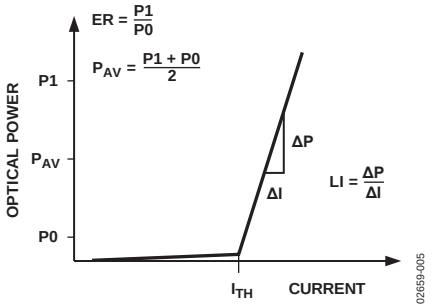


Figure 7. Laser Transfer Function

CONTROL

A monitor photodiode (MPD) is required to control the LD. The MPD current is fed into the ADN2841 to control the optical power and extinction ratio, continuously adjusting the bias current and modulation current in response to the laser's changing threshold current and light-to-current (LI) slope (slope efficiency).

The ADN2841 uses automatic power control (APC) to maintain a constant power over time and temperature.

The ADN2841 uses closed-loop extinction ratio control to allow optimum setting of extinction ratio for every device. Therefore, SONET/SDH interface standards can be met over device variation, temperature, and time. Closed-loop modulation control eliminates the need to overmodulate the LD or to include external components for temperature compensation. This reduces research and development time and second-sourcing issues caused by characterizing LDs.

Average power and extinction ratio are set using the PSET and ERSET pins, respectively. Potentiometers are connected between these pins and ground. The potentiometer R_{PSET} is used to change the average power. The potentiometer R_{ERSET} is used to adjust the extinction ratio. Both PSET and ERSET are kept 1.23 V above GND.

R_{PSET} and R_{ERSET} can be calculated using the following formulas:

$$R_{PSET} = \frac{1.23\ \text{V}}{I_{AV}}$$

where I_{AV} is the average MPD current.

$$R_{ERSET} = \frac{1.23\ \text{V}}{\frac{I_{MPD\_CW}}{P_{CW}} \times \frac{ER-1}{ER+1} \times 0.2 \times P_{AV}}$$

where

I_{MPD_CW} is the MPD current at the specified P_{CW}.

P_{CW} is the dc optical power specified on the laser data sheet.

P_{AV} is the required average power.

Note that I_{ERSET} and I_{PSET} change from device to device. However, the control loops determine the actual values. It is not required to know the exact values for LI or MPD optical coupling.

LOOP BANDWIDTH SELECTION

For anyrate operation, the user should hardwire the LBWSET pin high and use 1 µF capacitors to set the actual loop bandwidth. These capacitors are placed between the PAVCAP and ERCAP pins and ground. It is important that these capacitors be low leakage multilayer ceramics with an insulation resistance greater than 100 GΩ or a time constant of 1000 sec, whichever is less. The ADN2841 can be optimized for 2.7 Gbps operation by keeping the LBWSET pin low. This results in a much shorter loop time constant (a 10× reduction). The value of the PAVCAP and ERCAP capacitors required for 2.7 Gbps operation is 22 nF.

ALARMS

The ADN2841 alarms are designed to allow interface compliance to ITU-T G.958 (11/94), Section 10.3.1.1.2 (transmit fail) and Section 10.3.1.1.3 (transmit degrade). The ADN2841 has two active high alarms, DEGRADE and FAIL. A resistor between ground and the ASET pin is used to set the current at which these alarms are raised. The current through the ASET resistor is a ratio of 100:1 to the FAIL alarm threshold. The DEGRADE alarm will be raised at 90% of this level.

Example:

$$I_{FAIL} = 50\ \text{mA} \therefore I_{DEGRADE} = 45\ \text{mA}$$

$$I_{ASET} = \frac{I_{BIASTRIP}}{100} = \frac{50\ \text{mA}}{100} = 500\ \mu\text{A}$$

$$R_{ASET} = \frac{1.23\ \text{V}}{I_{ASET}} = \frac{1.23\ \text{V}}{500\ \mu\text{A}} = 2.46\ \text{k}\Omega$$

Note that the smallest value for R_{ASET} is 1.2 kΩ, because this value corresponds to the I_{BIAS} maximum of 100 mA.

The laser degrade alarm, DEGRADE, gives a warning of imminent laser failure if the laser diode degrades further or if environmental conditions—for example, increasing temperature—continue to stress the LD.

The laser fail alarm, FAIL, is activated when the transmitter can no longer be guaranteed to be SONET/SDH compliant. This occurs when one of the following conditions arises:

- The ASET threshold is reached.
- The ALS pin is set high. This shuts off the modulation and bias currents to the LD, resulting in the MPD current dropping to 0. This gives closed-loop feedback to the system in which ALS has been enabled.

The DEGRADE pin goes high only when the bias current exceeds 90% of the ASET current.

MONITOR CURRENTS

IBMON, IMMON, IMPDMON, and IMPDMON2 are current controlled current sources from V_{CC}. They mirror the bias, modulation, and MPD current for increased monitoring functionality. An external resistor to GND gives a voltage proportional to the current monitored.

DUAL MPD DWDM FUNCTION (48-LEAD LFCSP ONLY)

The ADN2841 has circuitry for an optional second monitor photodiode, MPD2. The second photodiode current is mirrored to IMPDMON2 for wavelength control purposes and is summed internally for the power control loop. For single MPD circuits, the IMPD2 pin is tied to GND.

The second monitor photodiode enables the system designer to use the two currents to control the wavelength of the laser diode using various optical filtering techniques inside the laser module.

If the monitor current functions IMPDMON and IMPDMON2 are not required, the IMPD and IMPD2 pins can be grounded, and the monitor photodiode output can be connected directly to PSET.

IDTONE (48-LEAD LFCSP ONLY)

The IDTONE pin is supplied for fiber identification/supervisory channels or control purposes in WDM. This pin modulates the Optical 1 level over a possible range of 2% of minimum I_{MOD} to 10% of maximum I_{MOD}. The level of modulation is set by connecting an external current sink between the IDTONE pin and ground. There is a gain of 2 from this pin to the I_{MOD} current.

Figure 8 shows how an AD9850/AD9851 DDS can be used with the ADN2841 to allow fiber identification.

Note that using IDTONE during transmission may cause optical eye degradation.

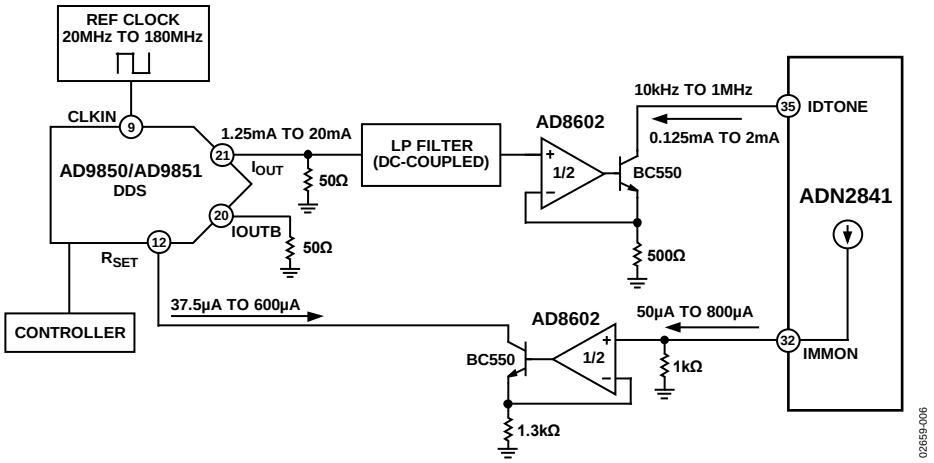


Figure 8. Circuitry to Allow Fiber Identification

DATA AND CLOCK INPUTS

Data and clock inputs are ac-coupled (10 nF recommended) and terminated via a 100 Ω internal resistor between the DATAP and DATAN pins and also between the CLKP and CLKN pins. A high impedance circuit sets the common-mode voltage that is designed to change over temperature. It is recommended that ac coupling be used to eliminate the need for matching between common-mode voltages.

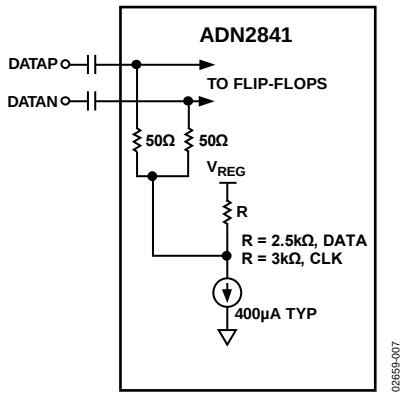


Figure 9. AC Coupling of Data Inputs

CCBIAS

CCBIAS should be connected to the IBIAS pin if the laser diode is connected to the ADN2841 using a capacitor. CCBIAS is a current sink to GND.

AUTOMATIC LASER SHUTDOWN

The ADN2841 ALS pin allows compliance with ITU-T G.958 (11/94), Section 9.7. When ALS is logic high, both bias and modulation currents are turned off.

Correct operation of ALS can be confirmed by the FAIL alarm being raised when ALS is asserted. Note that this is the only time that DEGRADE will be low while FAIL is high.

ALARM INTERFACES

A 30 kΩ internal pull-up resistor is used to pull the digital high value of the alarm outputs to V_{CC}. However, the ADN2841 has a feature that allows the user to externally wire resistors in parallel with the 30 kΩ pull-up resistors, thus enabling the user to interface to non-V_{CC} levels. Non-V_{CC} alarm output levels must be below the V_{CC} used for the ADN2841.

POWER CONSUMPTION

The ADN2841 die temperature must be kept below 125°C. The θ_{JA} is 25°C/W for the 48-lead LFCSP and 32°C/W for the 32-lead LFCSP when soldered on a 4-layer board. Both LFCSP packages have an exposed pad and, therefore, must be soldered to the PCB to achieve this thermal performance.

$$T_{DIE} = T_{AMBIENT} + (\theta_{JA} \times P)$$

$$I_{CC} = I_{CCMIN} + (0.3 \times I_{MOD})$$

$$P = V_{CC} \times I_{CC} + (I_{BIAS} \times V_{IBIAS}) + (I_{MOD} \times V_{IMODx})$$

Thus, the maximum combination of I_{BIAS} + I_{MOD} must be calculated.

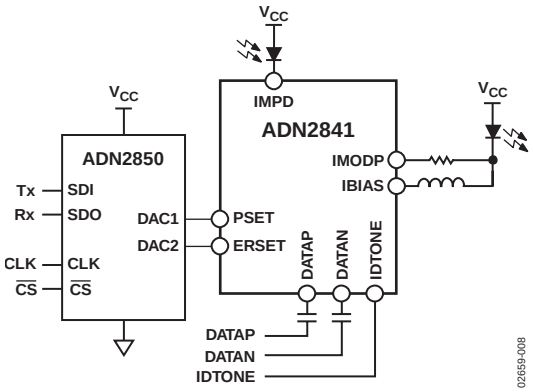
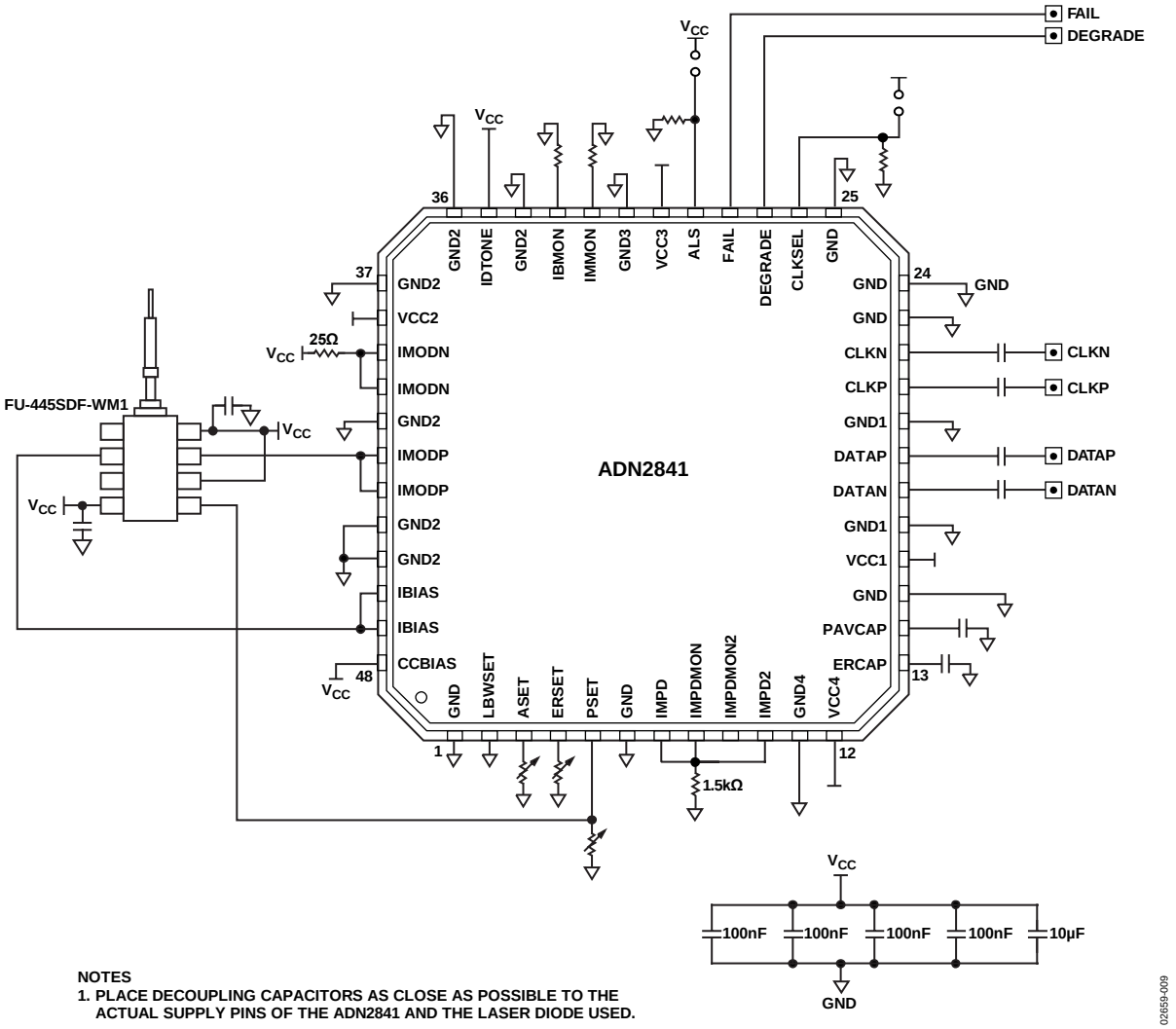


Figure 10. Application Using Optical Supervisor ADN2850 as a Dual, 10-Bit Digital Potentiometer Using Thin Film Resistor Technology to Give Very Low Temperature Coefficients

APPLICATION CIRCUITS



NOTES
1. PLACE DECOUPLING CAPACITORS AS CLOSE AS POSSIBLE TO THE ACTUAL SUPPLY PINS OF THE ADN2841 AND THE LASER DIODE USED.

Figure 11. 2.7 Gbps Test Circuit, DC-Coupled, Data Not Clocked, Fast Loop Time Constant Selected

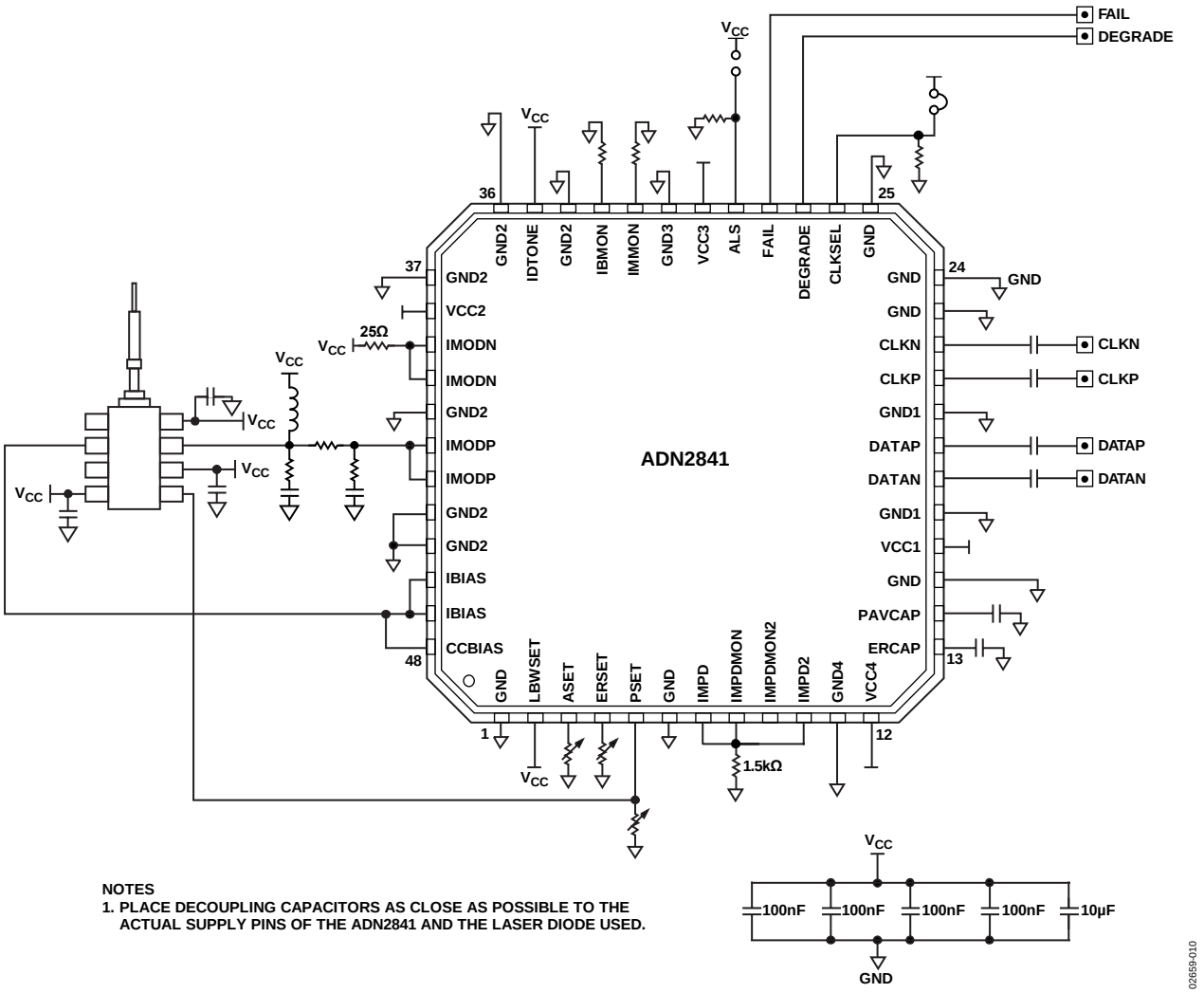
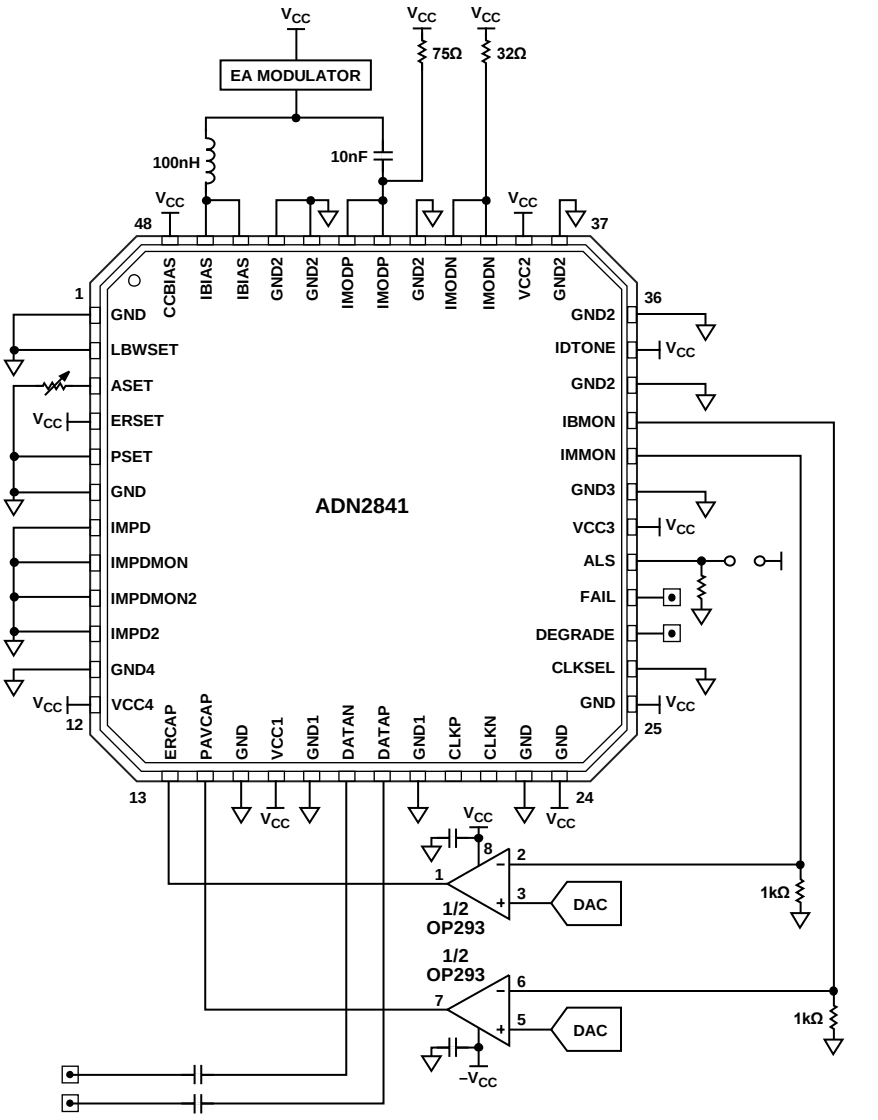


Figure 12. Anyrate Test Circuit, Capacitively Coupled, Data Clocked, Slow Loop Time Constant Selected

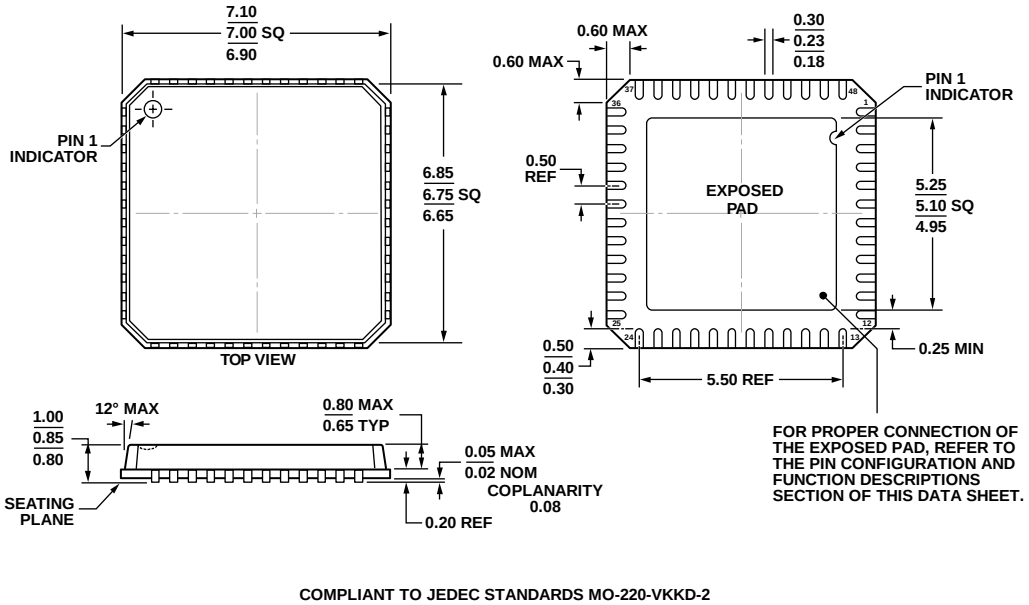


NOTES
1. PLACE DECOUPLING CAPACITORS AS CLOSE AS POSSIBLE TO THE ACTUAL SUPPLY PINS OF THE ADN2841 AND THE LASER DIODE USED.
2. THE OP293 HAS BEEN SELECTED BECAUSE OF ITS GAIN BANDWIDTH PRODUCT AND SHOULD BE USED IN THIS APPLICATION.

02659-011

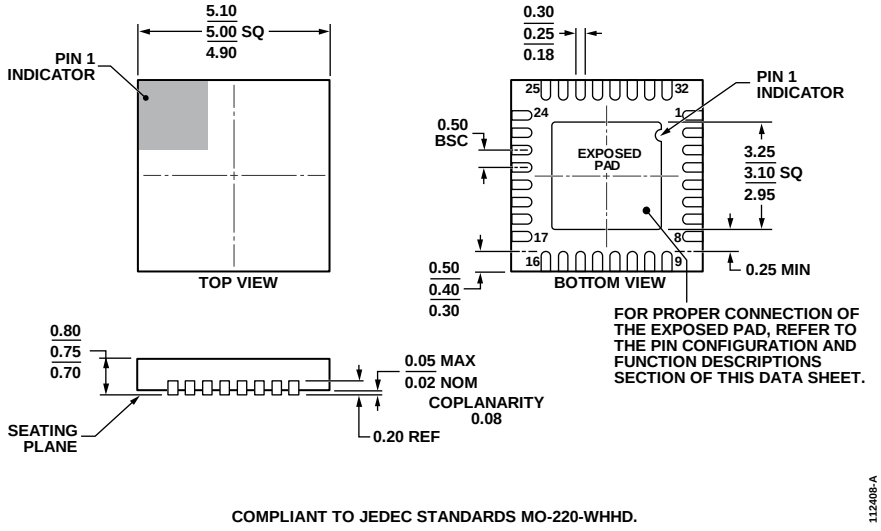
Figure 13. Applications Circuit

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VKKD-2

Figure 14. 48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
7 mm × 7 mm Body, Very Thin Quad
(CP-48-1)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD.

Figure 15. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Very Thin Quad
(CP-32-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADN2841ACPZ-32	−40°C to +85°C	32-Lead LFCSP_WQ	CP-32-7
ADN2841ACPZ-32-RL	−40°C to +85°C	32-Lead LFCSP_WQ	CP-32-7
ADN2841ACPZ-32-RL7	−40°C to +85°C	32-Lead LFCSP_WQ	CP-32-7
ADN2841ACPZ-48	−40°C to +85°C	48-Lead LFCSP_VQ	CP-48-1
ADN2841ACPZ-48-RL	−40°C to +85°C	48-Lead LFCSP_VQ	CP-48-1

[1] Z = RoHS Compliant Part.

D02659–0–9/13(B)