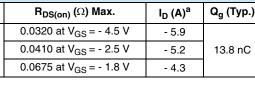
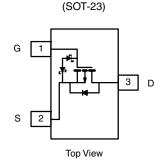




P-Channel 20 V (D-S) MOSFET

| PRODUCT SUMMARY | | | | | |
|---------------------|---|---------------------------------|-----------------------|--|--|
| V _{DS} (V) | $R_{DS(on)}\left(\Omega\right)$ Max. | I _D (A) ^a | Q _g (Typ.) | | |
| | 0.0320 at V _{GS} = - 4.5 V | - 5.9 | | | |
| - 20 | 0.0410 at V _{GS} = - 2.5 V | - 5.2 | 13.8 nC | | |
| | $0.0675 \text{ at V}_{GS} = -1.8 \text{ V}$ | - 4.3 | | | |





TO-236

Si2365EDS (H5)* * Marking Code

Ordering Information:

Si2365EDS-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

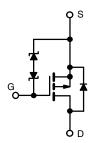
- TrenchFET® Power MOSFET
- 100 % R_g Tested
- Built-in ESD Protection
 - Typical ESD Performance 3000 V
- Material categorization: For definitions of compliance please see www.vishav.com/doc?99912



HALOGEN FREE

APPLICATIONS

- Power Management for Portable and Consumer
 - Load Switches
 - DC/DC Converters



P-Channel MOSFET

| Parameter | Symbol | Limit | Unit | | |
|--|-----------------------------------|----------------|-----------------------|----|--|
| Drain-Source Voltage | V_{DS} | - 20 | V | | |
| Gate-Source Voltage | V_{GS} | ± 8 | 1 V | | |
| | T _C = 25 °C | | - 5.9 | | |
| Continuous Drain Current (T. 150 °C) | T _C = 70 °C | | - 4.7 | | |
| Continuous Drain Current (T _J = 150 °C) | T _A = 25 °C | I _D | - 4.5 ^{b, c} | | |
| | T _A = 70 °C | | - 3.6 ^{b, c} | Α | |
| Pulsed Drain Current (t = 300 μs) | I _{DM} | - 20 | | | |
| Continuous Source-Drain Diode Current | T _C = 25 °C | | - 1.4 | | |
| Continuous Source-Drain Diode Current | T _A = 25 °C | ls – | - 1 ^{b, c} | | |
| | T _C = 25 °C | | 1.7 | | |
| Maximum Dawar Dissination | T _C = 70 °C | | 1.1 | W | |
| Maximum Power Dissipation | T _A = 25 °C | P _D | 1 ^{b, c} | VV | |
| | T _A = 70 °C | | 0.6 ^{b, c} | | |
| Operating Junction and Storage Temperature Ra | T _J , T _{stg} | - 55 to 150 | °C | | |
| Soldering Recommendations (Peak Temperature | | 260 | -0 | | |

| THERMAL RESISTANCE RATINGS | | | | | | |
|---|--------------|-------------------|---------|---------|---------|--|
| Parameter | | Symbol | Typical | Maximum | Unit | |
| Maximum Junction-to-Ambient ^{b, d} | t ≤ 5 s | R _{thJA} | 100 | 130 | °C/W | |
| Maximum Junction-to-Foot (Drain) | Steady State | R_{thJF} | 60 | 75 | - 'C/VV | |

Notes:

- a. $T_C = 25$ °C.
- b. Surface mounted on 1" x 1" FR4 board.
- d. Maximum under steady state conditions is 175 °C/W.

Si2365EDS

Vishay Siliconix



| Parameter | Symbol | Test Conditions | Min. | Тур. | Max. | Unit | |
|---|-------------------------|--|-------|--------|--------|-------|--|
| Static | | | | | | | |
| Drain-Source Breakdown Voltage | V_{DS} | $V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$ | - 20 | | | V | |
| V _{DS} Temperature Coefficient | $\Delta V_{DS}/T_{J}$ | I _D = - 250 μA | | - 14 | | mV/°C | |
| V _{GS(th)} Temperature Coefficient | $\Delta V_{GS(th)}/T_J$ | 1 _D = - 230 μΑ | | 2.5 | | | |
| Gate-Source Threshold Voltage | V _{GS(th)} | $V_{DS} = V_{GS}, I_{D} = -250 \mu A$ | - 0.4 | | - 1 | V | |
| Gate-Source Leakage | I _{GSS} | $V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$ | | | ± 10 | | |
| date-Source Leakage | | $V_{DS} = 0 \text{ V}, V_{GS} = \pm 4.5 \text{ V}$ | | | ± 1 | Δ | |
| Zero Gate Voltage Drain Current | lana | V _{DS} = - 20 V, V _{GS} = 0 V | | | - 1 | μΑ | |
| Zero Gate voltage Diam Guirent | I _{DSS} | $V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 \text{ °C}$ | | | - 10 | 7 | |
| On-State Drain Current ^a | I _{D(on)} | $V_{DS} \le -5 \text{ V}, V_{GS} = -4.5 \text{ V}$ | - 15 | | | Α | |
| | | V _{GS} = - 4.5 V, I _D = - 4 A | | 0.0265 | 0.0320 | | |
| Drain-Source On-State Resistance ^a | R _{DS(on)} | V _{GS} = - 2.5 V, I _D = - 4 A | | 0.0340 | 0.0410 | Ω | |
| | | V _{GS} = - 1.8 V, I _D = - 2 A | | 0.0465 | 0.0675 | 1 | |
| Dynamic ^b | | | | | | | |
| Total Cata Charge | 0 | $V_{DS} = -10 \text{ V}, V_{GS} = -8 \text{ V}, I_{D} = -4.5 \text{ A}$ | | 23.8 | 36 | nC | |
| Total Gate Charge | Qg | V _{DS} = - 10 V, V _{GS} = - 4.5 V, I _D = - 4.5 A | | 13.8 | 21 | | |
| Gate-Source Charge | Q_{gs} | | | 1.9 | | | |
| Gate-Drain Charge | Q_{gd} | | | 3 | | | |
| Gate Resistance | R_g | f = 1 MHz | 2.2 | 11 | 22 | Ω | |
| Turn-On Delay Time | t _{d(on)} | | | 22 | 33 | | |
| Rise Time | t _r | $V_{DD} = -10 \text{ V}, R_L = 2.8 \Omega$ $I_D \cong -3.6 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_g = 1 \Omega$ | | 21 | 32 | | |
| Turn-Off Delay Time | | | | 62 | 93 | | |
| Fall Time | t _f | | | 14 | 21 | no | |
| Turn-On Delay Time | t _{d(on)} | | | 9 | 18 | ns | |
| Rise Time | t _r | V_{DD} = - 10 V, R_L = 2.8 Ω | | 6 | 12 | | |
| Turn-Off Delay Time | t _{d(off)} | $I_D \cong$ - 3.6 A, V_{GEN} = - 8 V, R_g = 1 Ω | | 65 | 98 | | |
| Fall Time | t _f | | | 15 | 23 | | |
| Drain-Source Body Diode Characterist | ics | | | | | | |
| Continuous Source-Drain Diode Current | I _S | $T_C = 25 ^{\circ}C$ | | | - 1.4 | Α | |
| Pulse Diode Forward Current | I _{SM} | | | | - 20 | ^ | |
| Body Diode Voltage | V_{SD} | I _S = - 3.6 A, V _{GS} = 0 V | | - 0.8 | - 1.2 | V | |
| Body Diode Reverse Recovery Time | t _{rr} | | | 13 | 20 | ns | |
| Body Diode Reverse Recovery Charge | Q _{rr} | I _F = - 3.6 A, dl/dt = 100 A/μs, T _{.I} = 25 °C | | 5 | 10 | nC | |
| Reverse Recovery Fall Time | t _a | $_{1F} = -3.0 \text{ A}, \text{ ul/ul} = 100 \text{ A/}\mu\text{s}, \text{ IJ} = 25 ^{\circ}\text{C}$ | | 8 | | ns | |
| Reverse Recovery Rise Time | t _b | | | 5 | | | |

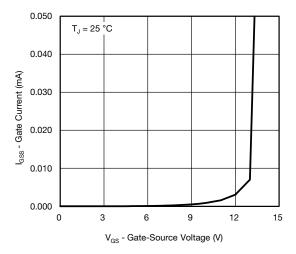
Notes:

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

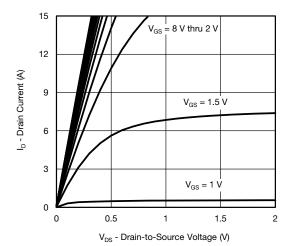
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



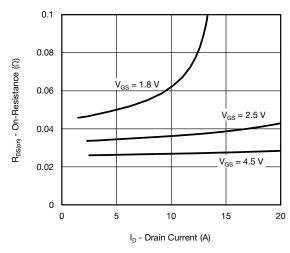
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



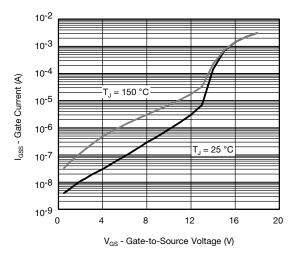
Gate Current vs. Gate-Source Voltage



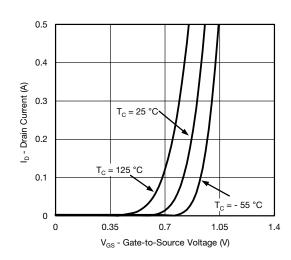
Output Characteristics



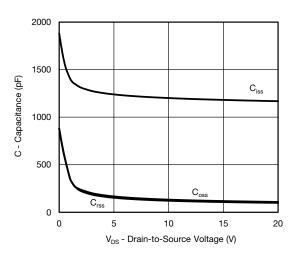
On-Resistance vs. Drain Current



Gate Current vs. Gate-Source Voltage



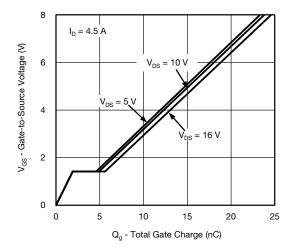
Transfer Characteristics



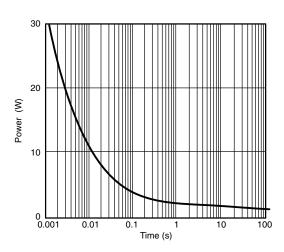
Capacitance

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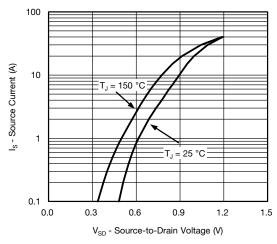
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



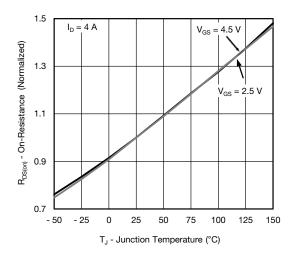
Gate Charge



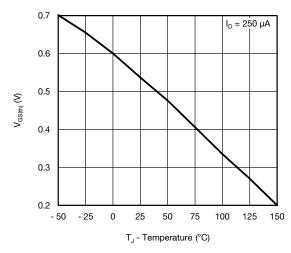
Single Pulse Power, Junction-to-Ambient



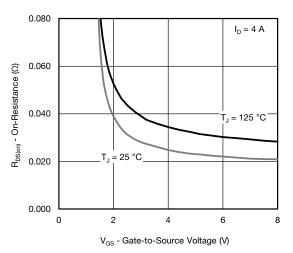
Soure-Drain Diode Forward Voltage



On-Resistance vs. Junction Temperature



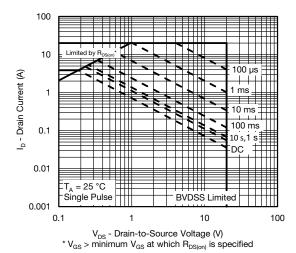
Threshold Voltage



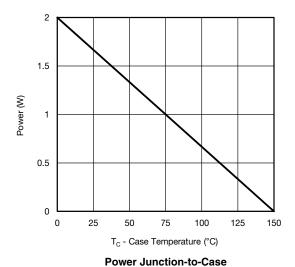
On-Resistance vs. Gate-to-Source Voltage

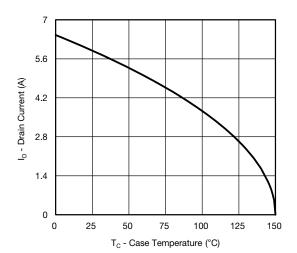


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

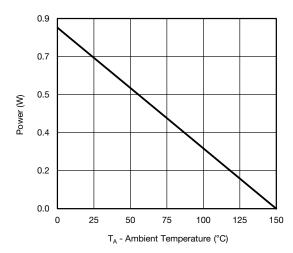


Safe Operating Area, Junction-to-Ambient





Current Derating*

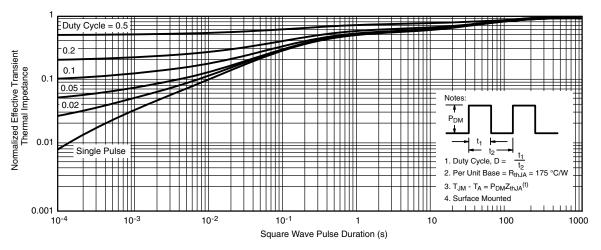


Power Junction-to-Ambient

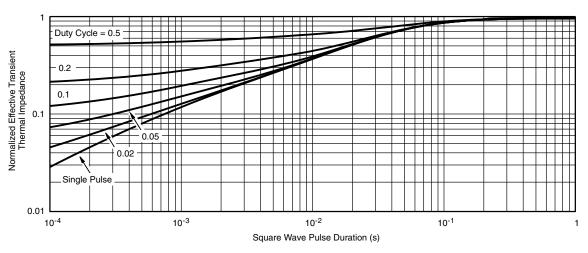
 $^{^{\}star}$ The power dissipation P_D is based on $T_{J(max.)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63199.

Vishay Siliconix

SOT-23 (TO-236): 3-LEAD







| Dim | MILLIMETERS | | INCHES | | |
|------------------------|-------------|----------|-----------|-----------|--|
| | Min | Max | Min | Max | |
| Α | 0.89 | 1.12 | 0.035 | 0.044 | |
| A ₁ | 0.01 | 0.10 | 0.0004 | 0.004 | |
| A ₂ | 0.88 | 1.02 | 0.0346 | 0.040 | |
| b | 0.35 | 0.50 | 0.014 | 0.020 | |
| С | 0.085 | 0.18 | 0.003 | 0.007 | |
| D | 2.80 | 3.04 | 0.110 | 0.120 | |
| E | 2.10 | 2.64 | 0.083 | 0.104 | |
| E ₁ | 1.20 | 1.40 | 0.047 | 0.055 | |
| е | 0.9 | 5 BSC | 0.037 | 4 Ref | |
| e ₁ | 1.9 | 0 BSC | 0.074 | 48 Ref | |
| L | 0.40 | 0.60 | 0.016 | 0.024 | |
| L ₁ | 0.6 | 0.64 Ref | | 0.025 Ref | |
| S | 0.5 | 50 Ref | 0.020 Ref | | |
| q | 3° | 8° | 3° | 8° | |
| FCN: S-03946-Rev K 09- | lul-01 | • | | | |

ECN: S-03946-Rev. K, 09-Jul-01

DWG: 5479

Document Number: 71196 www.vishay.com 09-Jul-01





Mounting LITTLE FOOT® SOT-23 Power MOSFETs

Wharton McDaniel

Surface-mounted LITTLE FOOT power MOSFETs use integrated circuit and small-signal packages which have been been modified to provide the heat transfer capabilities required by power devices. Leadframe materials and design, molding compounds, and die attach materials have been changed, while the footprint of the packages remains the same.

See Application Note 826, Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs, (http://www.vishay.com/doc?72286), for the basis of the pad design for a LITTLE FOOT SOT-23 power MOSFET footprint. In converting this footprint to the pad set for a power device, designers must make two connections: an electrical connection and a thermal connection, to draw heat away from the package.

The electrical connections for the SOT-23 are very simple. Pin 1 is the gate, pin 2 is the source, and pin 3 is the drain. As in the other LITTLE FOOT packages, the drain pin serves the additional function of providing the thermal connection from the package to the PC board. The total cross section of a copper trace connected to the drain may be adequate to carry the current required for the application, but it may be inadequate thermally. Also, heat spreads in a circular fashion from the heat source. In this case the drain pin is the heat source when looking at heat spread on the PC board.

Figure 1 shows the footprint with copper spreading for the SOT-23 package. This pattern shows the starting point for utilizing the board area available for the heat spreading copper. To create this pattern, a plane of copper overlies the drain pin and provides planar copper to draw heat from the drain lead and start the process of spreading the heat so it can be dissipated into the ambient air. This pattern uses all the available area underneath the body for this purpose.



FIGURE 1. Footprint With Copper Spreading

Since surface-mounted packages are small, and reflow soldering is the most common way in which these are affixed to the PC board, "thermal" connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low-impedance path for heat to move away from the device.

Document Number: 70739

26-Nov-03



RECOMMENDED MINIMUM PADS FOR SOT-23



Recommended Minimum Pads Dimensions in Inches/(mm)

Return to Index

APPLICATION NOTE



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