

FEATURES

44 V supply maximum ratings
V_{SS} to V_{DD} analog signal range
Low on resistance: <35 Ω
Ultralow power dissipation: < 35 μW
Fast transition time: 160 ns maximum
Break-before-make switching action
Plug-in replacement for DG419

APPLICATIONS

Precision test equipment
Precision instrumentation
Battery-powered systems
Sample hold systems

GENERAL DESCRIPTION

The ADG419 is a monolithic CMOS SPDT switch. This switch is designed on an enhanced LC²MOS process that provides low power dissipation yet gives high switching speed, low on resistance, and low leakage currents.

The on resistance profile of the ADG419 is very flat over the full analog input range, ensuring excellent linearity and low distortion. The part also exhibits high switching speed and high signal bandwidth. CMOS construction ensures ultralow power dissipation, making the parts ideally suited for portable and battery-powered instruments.

Each switch of the ADG419 conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked. The ADG419 exhibits break-before-make switching action.

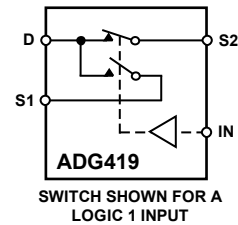
FUNCTIONAL BLOCK DIAGRAM

Figure 1.

PRODUCT HIGHLIGHTS

1. Extended Signal Range.
The ADG419 is fabricated on an enhanced LC²MOS process, giving an increased signal range that extends to the supply rails.
2. Ultralow Power Dissipation.
3. Low R_{ON}.
4. Single-Supply Operation.
For applications where the analog signal is unipolar, the ADG419 can be operated from a single rail power supply. The part is fully specified with a single 12 V power supply and remains functional with single supplies as low as 5 V.

Rev. B

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

ADG419* Product Page Quick Links

Last Content Update: 08/30/2016

Comparable Parts

View a parametric search of comparable parts

Evaluation Kits

- Evaluation Board for 8 lead MSOP Devices in the Switch/Mux Portfolio

Documentation

Data Sheet

- ADG419-DSCC: Military Data Sheet
- ADG419-EP: Enhanced Product Data Sheet
- ADG419: LC²MOS Precision Mini-DIP Analog Switch Data Sheet

User Guides

- UG-893: Evaluating the 8-Lead MSOP Devices in the Switch/Mux Portfolio

Reference Materials

Product Selection Guide

- Switches and Multiplexers Product Selection Guide

Technical Articles

- CMOS Switches Offer High Performance in Low Power, Wideband Applications
- Data-acquisition system uses fault protection
- Enhanced Multiplexing for MEMS Optical Cross Connects
- Temperature monitor measures three thermal zones

Design Resources

- ADG419 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

Discussions

View all ADG419 EngineerZone Discussions

Sample and Buy

Visit the product page to see pricing options

Technical Support

Submit a technical question or find your regional support number

TABLE OF CONTENTS

| | | | |
|--------------------------------|---|--|----|
| Features | 1 | Absolute Maximum Ratings | 5 |
| Applications..... | 1 | ESD Caution..... | 5 |
| Functional Block Diagram | 1 | Pin Configuration and Function Descriptions..... | 6 |
| General Description | 1 | Typical Performance Characteristics | 7 |
| Product Highlights | 1 | Test Circuits..... | 9 |
| Revision History | 2 | Terminology | 11 |
| Specifications..... | 3 | Outline Dimensions | 12 |
| Dual Supply | 3 | Ordering Guide | 13 |
| Single Supply | 4 | | |

REVISION HISTORY

8/09—Rev. B to Rev. C

| | |
|----------------------------------|-----------|
| Updated Format..... | Universal |
| Changes to Table 1..... | 3 |
| Changes to Table 2..... | 4 |
| Updated Outline Dimensions | 12 |
| Changes to Ordering Guide | 13 |

SPECIFICATIONS

DUAL SUPPLY

$V_{DD} = 15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, $V_L = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.

Table 1.

| Parameter ¹ | B Version | | | T Version | | Unit | Test Conditions/Comments |
|---|---------------------------------------|--------------------------|--------------------------|---------------------------------------|--------------------------|--|---|
| | +25°C | -40°C to +85°C | -40°C to +125°C | +25°C | -55°C to +125°C | | |
| ANALOG SWITCH | | | | | | | |
| Analog Signal Range | | | V_{SS} to V_{DD} | | V_{SS} to V_{DD} | | |
| R_{ON} | 25 35 | 45 | 45 | 25 35 | 45 | Ω typ Ω max | $V_D = \pm 12.5\text{ V}$, $I_S = -10\text{ mA}$ $V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$ |
| LEAKAGE CURRENTS | | | | | | | |
| Source Off Leakage, I_S (Off) | ± 0.1 | | | ± 0.1 | | nA typ | $V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$ $V_D = \pm 15.5\text{ V}$, $V_S = \mp 15.5\text{ V}$; see Figure 12 |
| Drain Off Leakage, I_D (Off) | ± 0.25 ± 0.1 | ± 5 | ± 15 | ± 0.25 ± 0.1 | ± 15 | nA max nA typ | $V_D = \pm 15.5\text{ V}$, $V_S = \mp 15.5\text{ V}$; see Figure 12 |
| Channel On Leakage, I_D , I_S (On) | ± 0.75 ± 0.4 ± 0.75 | ± 5 | ± 30 | ± 0.75 ± 0.4 ± 0.75 | ± 30 | nA max nA typ nA max | $V_S = V_D = \pm 15.5\text{ V}$; see Figure 13 |
| DIGITAL INPUTS | | | | | | | |
| Input High Voltage, V_{INH} | | 2.4 | 2.4 | | 2.4 | V min | |
| Input Low Voltage, V_{INL} | | 0.8 | 0.8 | | 0.8 | V max | |
| Input Current I_{INL} or I_{INH} | | ± 0.005 ± 0.5 | ± 0.005 ± 0.5 | | ± 0.005 ± 0.5 | μA typ μA max | $V_{IN} = V_{INL}$ or V_{INH} |
| DYNAMIC CHARACTERISTICS ² | | | | | | | |
| $t_{TRANSITION}$ | 160 | 200 | 200 | 145 | 200 | ns max | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_{S1} = \pm 10\text{ V}$, $V_{S2} = \mp 10\text{ V}$; see Figure 14 |
| Break-Before-Make Time Delay, t_D | 30 | | | 30 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_{S1} = V_{S2} = \pm 10\text{ V}$; see Figure 15 |
| Off Isolation | 5 | | | 5 | | ns min | |
| Channel-to-Channel Crosstalk | 80 | | | 80 | | dB typ | $R_L = 50\ \Omega$, $f = 1\text{ MHz}$; see Figure 16 |
| C_S (Off) | 90 | | | 70 | | dB typ | $R_L = 50\ \Omega$, $f = 1\text{ MHz}$; see Figure 17 |
| C_S (On) | 6 | | | 6 | | pF typ | $f = 1\text{ MHz}$ |
| C_D , C_S (On) | 55 | | | 55 | | pF typ | $f = 1\text{ MHz}$ |
| POWER REQUIREMENTS | | | | | | | |
| I_{DD} | 0.0001 | | | 0.0001 | | μA typ | $V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$ $V_{IN} = 0\text{ V}$ or 5 V |
| | 1 | 2.5 | 2.5 | 1 | 2.5 | μA max | |
| I_{SS} | 0.0001 | | | 0.0001 | | μA typ | |
| | 1 | 2.5 | 2.5 | 1 | 2.5 | μA max | |
| I_L | 0.0001 | | | 0.0001 | | μA typ | $V_L = 5.5\text{ V}$ |
| | 1 | 2.5 | 2.5 | 1 | 2.5 | μA max | |

¹ Temperature ranges are as follows: B Version: -40°C to $+125^\circ\text{C}$; T Version: -55°C to $+125^\circ\text{C}$.

² Guaranteed by design, not subject to production test.

ADG419

SINGLE SUPPLY

$V_{DD} = 12\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $V_L = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.

Table 2.

| Parameter ¹ | B Version | | | T Version | | Unit | Test Conditions/Comments |
|--|---------------------------------------|--------------------------|--------------------------|---------------------------------------|--------------------------|--|---|
| | +25°C | -40°C to +85°C | -40°C to +125°C | +25°C | -55°C to +125°C | | |
| ANALOG SWITCH | | | | | | | |
| Analogue Signal Range | | | 0 to V_{DD} | | | V | |
| R_{ON} | 40 | | | 40 | | Ω typ | $V_D = 3\text{ V}$, 8.5 V , $I_S = -10\text{ mA}$ |
| | | 60 | 70 | | 70 | Ω max | $V_{DD} = 10.8\text{ V}$ |
| LEAKAGE CURRENT | | | | | | | |
| Source OFF Leakage, I_S (Off) | ± 0.1 | | | ± 0.1 | | nA typ | $V_{DD} = 13.2\text{ V}$ $V_D = 12.2\text{ V}/1\text{ V}$, $V_S = 1\text{ V}/12.2\text{ V}$; see Figure 12 |
| Drain OFF Leakage, I_D (Off) | ± 0.25 ± 0.1 | ± 5 | ± 15 | ± 0.25 ± 0.1 | ± 15 | nA max nA typ | $V_D = 12.2\text{ V}/1\text{ V}$, $V_S = 1\text{ V}/12.2\text{ V}$; see Figure 12 |
| Channel ON Leakage, I_D , I_S (On) | ± 0.75 ± 0.4 ± 0.75 | ± 5 | ± 30 | ± 0.75 ± 0.4 ± 0.75 | ± 30 | nA max nA typ nA max | $V_S = V_D = 12.2\text{ V}/1\text{ V}$; see Figure 13 |
| DIGITAL INPUTS | | | | | | | |
| Input High Voltage, V_{INH} | | 2.4 | 2.4 | | 2.4 | V min | |
| Input Low Voltage, V_{INL} | | 0.8 | 0.8 | | 0.8 | V max | |
| Input Current I_{INL} or I_{INH} | | ± 0.005 ± 0.5 | ± 0.005 ± 0.5 | | ± 0.005 ± 0.5 | μA typ μA max | $V_{IN} = V_{INL}$ or V_{INH} |
| DYNAMIC CHARACTERISTICS² | | | | | | | |
| $t_{TRANSITION}$ | 180 | 250 | 250 | 170 | 250 | ns max | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_{S1} = 0\text{ V}/8\text{ V}$, $V_{S2} = 8\text{ V}/0\text{ V}$; see Figure 14 |
| Break-Before-Make Time Delay, t_D | 60 | | | 60 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_{S1} = V_{S2} = 8\text{ V}$; see Figure 15 |
| Off Isolation | 80 | | | 80 | | dB typ | $R_L = 50\ \Omega$, $f = 1\text{ MHz}$; see Figure 16 |
| Channel-to-Channel Crosstalk | 90 | | | 70 | | dB typ | $R_L = 50\ \Omega$, $f = 1\text{ MHz}$; see Figure 17 |
| C_S (Off) | 13 | | | 13 | | pF typ | $f = 1\text{ MHz}$ |
| C_D , C_S (On) | 65 | | | 65 | | pF typ | $f = 1\text{ MHz}$ |
| POWER REQUIREMENTS | | | | | | | |
| I_{DD} | 0.0001 | | | 0.0001 | | μA typ | $V_{DD} = 13.2\text{ V}$ $V_{IN} = 0\text{ V}$ or 5 V |
| | 1 | 2.5 | 2.5 | 1 | 2.5 | μA max | |
| I_L | 0.0001 | | | 0.0001 | | μA typ | $V_L = 5.5\text{ V}$ |
| | 1 | 2.5 | 2.5 | 1 | 2.5 | μA max | |

¹ Temperature ranges are as follows: B Version: -40°C to $+125^\circ\text{C}$; T Version: -55°C to $+125^\circ\text{C}$.

² Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise noted.

Table 3.

| Parameter | Rating |
|--|--|
| V_{DD} to V_{SS} | 44 V |
| V_{DD} to GND | -0.3 V to +25 V |
| V_{SS} to GND | +0.3 V to -25 V |
| V_L to GND | -0.3 V to $V_{DD} + 0.3$ V |
| Analog, Digital Inputs ¹ | $V_{SS} - 2$ V to $V_{DD} + 2$ V or 30 mA, whichever occurs first |
| Continuous Current, S or D | 30 mA |
| Peak Current, S or D (Pulsed at 1 ms, 10% Duty-Cycle Maximum) | 100 mA |
| Operating Temperature Range | |
| Industrial (B Version) | -40°C to +125°C |
| Extended (T Version) | -55°C to +125°C |
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature | 150°C |
| CERDIP Package, Power Dissipation | 600 mW |
| θ_{JA} , Thermal Impedance | 110°C/W |
| Lead Temperature, Soldering (10 sec) | 300°C |
| PDIP Package, Power Dissipation | 400 mW |
| θ_{JA} , Thermal Impedance | 100°C/W |
| Lead Temperature, Soldering (10 sec) | 260°C |
| SOIC Package, Power Dissipation | 400 mW |
| θ_{JA} , Thermal Impedance | 155°C/W |
| MSOP Package, Power Dissipation | 315 mW |
| θ_{JA} , Thermal Impedance | 205°C/W |
| Lead Temperature, Soldering | |
| Vapor Phase (60 sec) | 215°C |
| Infrared (15 sec) | 220°C |

¹Overvoltages at IN, S or D is clamped by internal diodes. Limit current to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ADG419

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

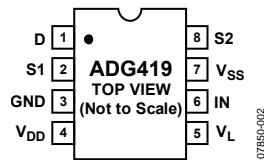


Figure 2. Pin Configuration

Table 4. Pin Function Description

| Pin No. | Mnemonic | Description |
|---------|-----------------|--|
| 1 | D | Drain terminal. May be an input or an output. |
| 2 | S1 | Source terminal. May be an input or an output. |
| 3 | GND | Ground (0 V) reference. |
| 4 | V _{DD} | Most positive power supply potential. |
| 5 | V _L | Logic power supply (5 V). |
| 6 | IN | Logic control input. |
| 7 | V _{SS} | Most negative power supply potential in dual-supply applications. In single-supply applications, it may be connected to GND. |
| 8 | S2 | Source terminal. May be an input or an output. |

Table 5. Truth Table

| Logic | Switch 1 | Switch 2 |
|-------|----------|----------|
| 0 | On | Off |
| 1 | Off | On |

TYPICAL PERFORMANCE CHARACTERISTICS

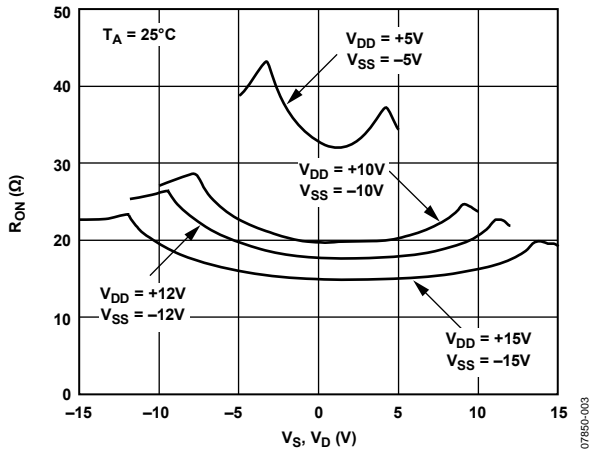


Figure 3. R_{ON} as a Function of V_D (V_S), Dual-Supply Voltage

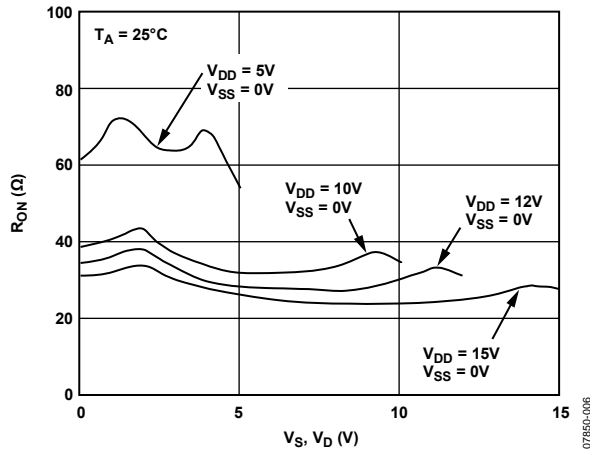


Figure 6. R_{ON} as a Function of V_D (V_S), Single-Supply Voltage

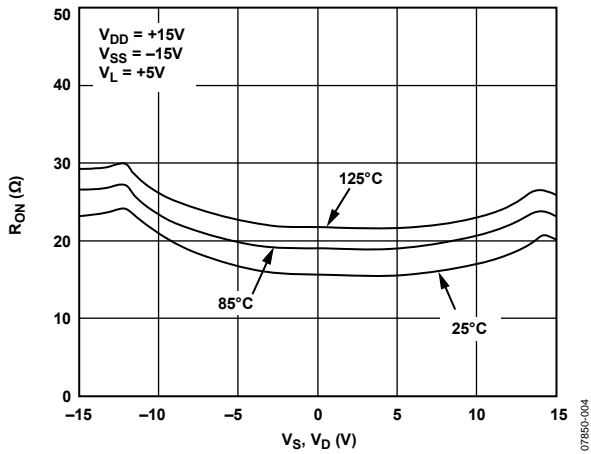


Figure 4. R_{ON} as a Function of V_D (V_S) for Different Temperatures

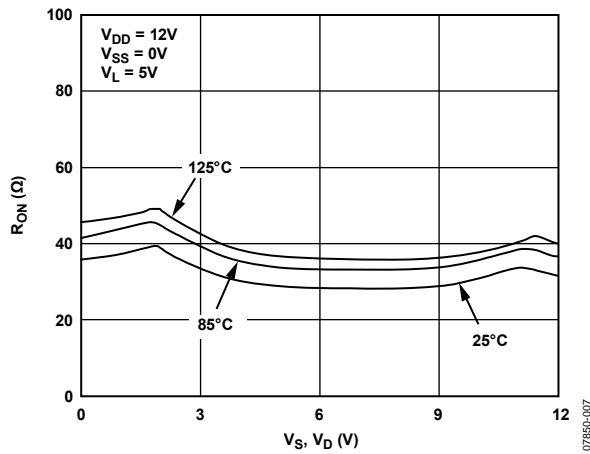


Figure 7. R_{ON} as a Function of V_D (V_S) for Different Temperatures

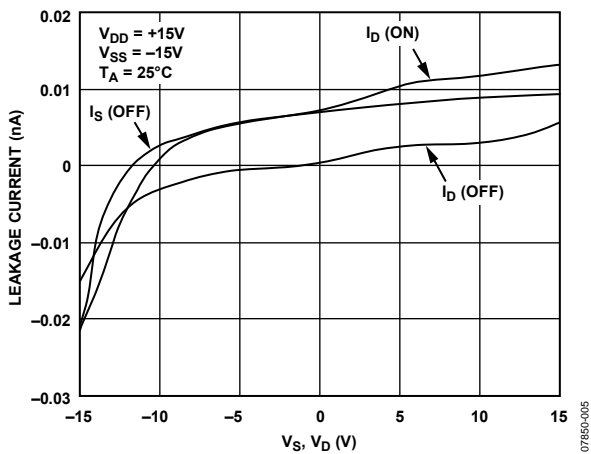


Figure 5. Leakage Currents as a Function of V_S (V_D)

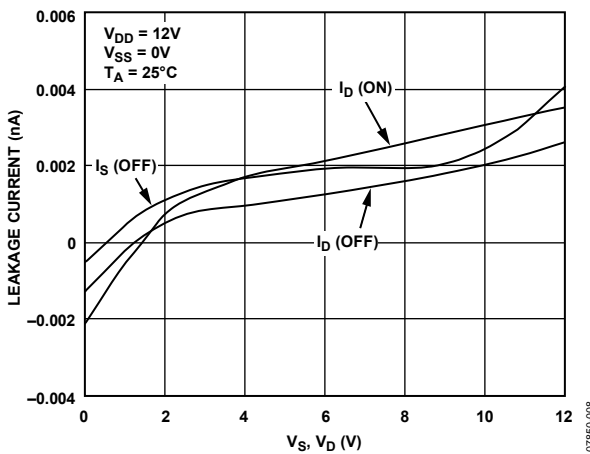


Figure 8. Leakage Currents as a Function of V_S (V_D)

ADG419

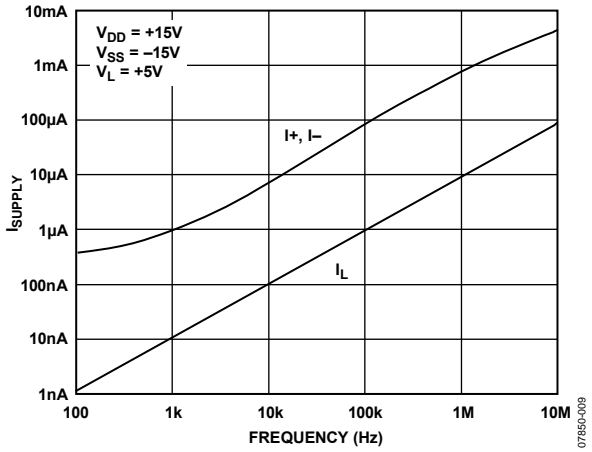


Figure 9. Supply Current (I_{SUPPLY}) vs. Input Switching Frequency

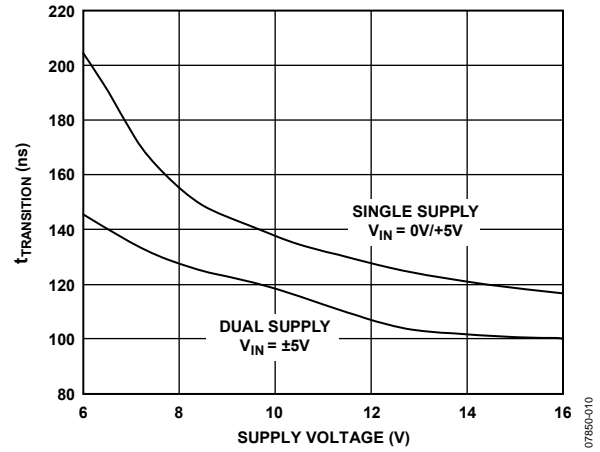


Figure 10. Transition Time ($t_{TRANSITION}$) vs. Power Supply Voltage

TEST CIRCUITS

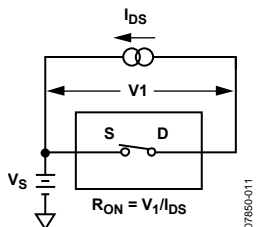


Figure 11. On Resistance

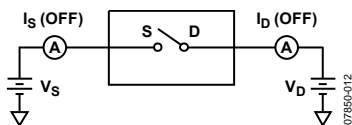


Figure 12. Off Leakage

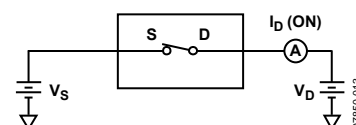


Figure 13. On Leakage

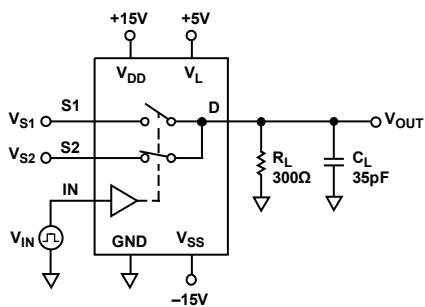
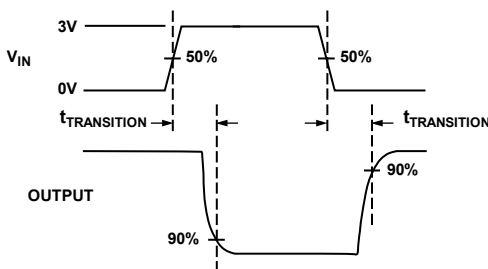


Figure 14. Transition Time, $t_{\text{TRANSITION}}$



07850-014

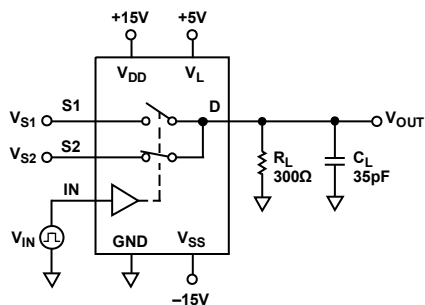
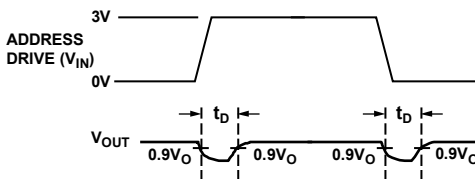


Figure 15. Break-Before-Make Time Delay, t_D



07850-015

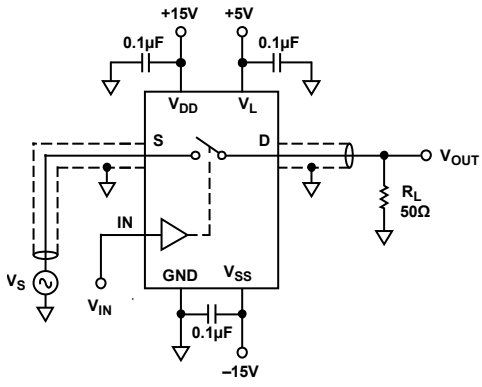
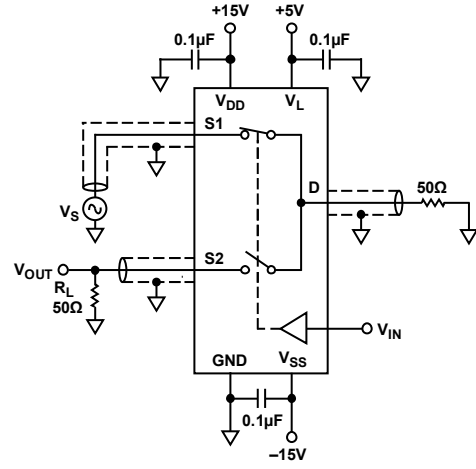


Figure 16. Off Isolation

07850-016



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \times \log |V_S/V_{OUT}|$$

Figure 17. Crosstalk

07850-017

TERMINOLOGY

V_{DD}

Most positive power supply potential.

V_{SS}

Most negative power supply potential in dual-supply applications.
In single-supply applications, it may be connected to GND.

V_L

Logic power supply (5 V).

GND

Ground (0 V) reference.

S

Source terminal. May be an input or an output.

D

Drain terminal. May be an input or an output.

IN

Logic control input.

R_{ON}

Ohmic resistance between D and S.

I_S (Off)

Source leakage current with the switch off.

I_D (Off)

Drain leakage current with the switch off.

I_D, I_S (On)

Channel leakage current with the switch on.

V_D (V_S)

Analog voltage on terminals D, S.

C_S (Off)

Off switch source capacitance.

C_D, C_S (On)

On switch capacitance.

t_{TRANSITION}

Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

t_D

Off time or on time measured between the 90% points of both switches when switching from one address state to the other.

V_{INL}

Maximum input voltage for Logic 0.

V_{INH}

Minimum input voltage for Logic 1.

I_{INL} (I_{INH})

Input current of the digital input.

Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Off Isolation

A measure of unwanted signal coupling through an off channel.

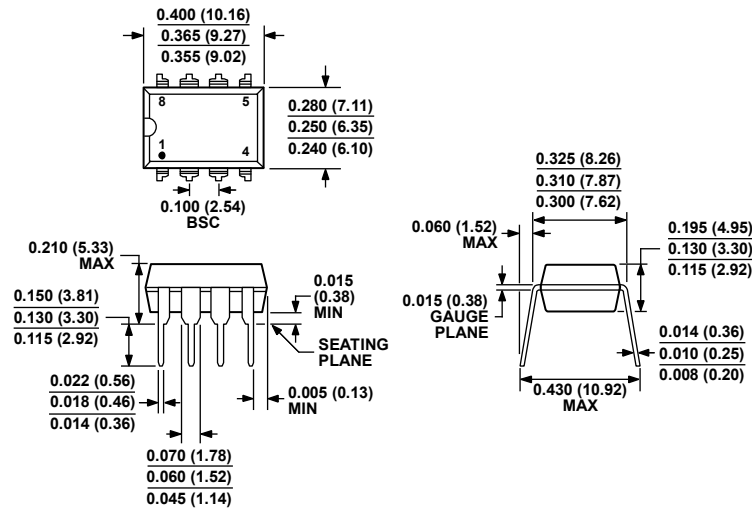
I_{DD}

Positive supply current.

I_{SS}

Negative supply current.

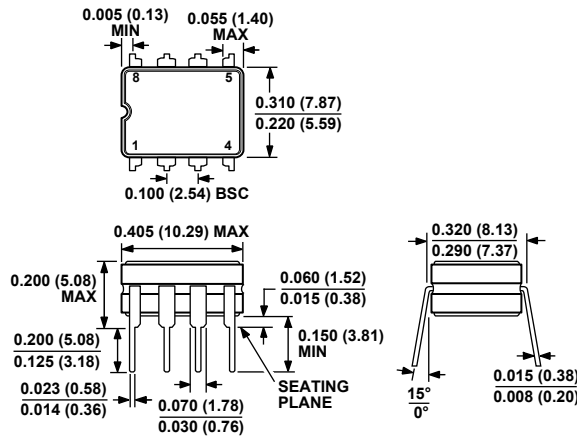
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 18. 8-Lead Plastic Dual In-Line Package [PDIP] Narrow Body (N-8)

Dimensions shown in inches and (millimeters)

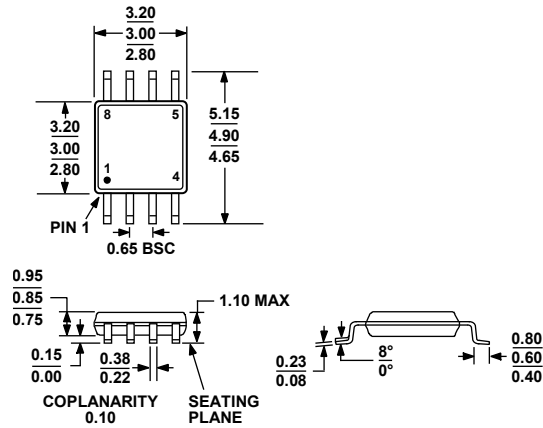


CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 19. 8-Lead Ceramic Dual In-Line Package [CERDIP] (Q-8)

Dimensions shown in inches and (millimeters)

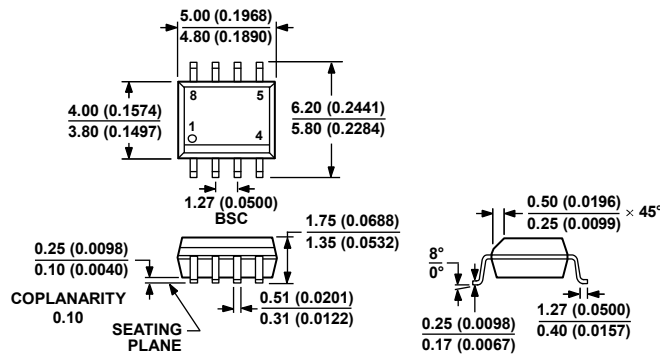
070606-A



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 20. 8-Lead Mini Small Outline Package [MSOP] (RM-8)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 21. 8-Lead Standard Small Outline Package [SOIC_N] Narrow Body (R-8)

Dimensions shown in millimeters and (inches)

012407-A

ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option | Branding |
|-------------------------------|-------------------|--|----------------|----------|
| ADG419BN | -40°C to +125°C | 8-Lead Plastic Dual In-Line Package [PDIP] | N-8 | |
| ADG419BNZ ¹ | -40°C to +125°C | 8-Lead Plastic Dual In-Line Package [PDIP] | N-8 | |
| ADG419BR | -40°C to +125°C | 8-Lead Standard Small Outline Package [SOIC_N] | R-8 | |
| ADG419BR-REEL | -40°C to +125°C | 8-Lead Standard Small Outline Package [SOIC_N] | R-8 | |
| ADG419BR-REEL7 | -40°C to +125°C | 8-Lead Standard Small Outline Package [SOIC_N] | R-8 | |
| ADG419BRZ ¹ | -40°C to +125°C | 8-Lead Standard Small Outline Package [SOIC_N] | R-8 | |
| ADG419BRZ-REEL ¹ | -40°C to +125°C | 8-Lead Standard Small Outline Package [SOIC_N] | R-8 | |
| ADG419BRZ-REEL7 ¹ | -40°C to +125°C | 8-Lead Standard Small Outline Package [SOIC_N] | R-8 | |
| ADG419BRM | -40°C to +125°C | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | SBB |
| ADG419BRM-REEL | -40°C to +125°C | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | SBB |
| ADG419BRM-REEL7 | -40°C to +125°C | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | SBB |
| ADG419BRMZ ¹ | -40°C to +125°C | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | SBB# |
| ADG419BRMZ-REEL ¹ | -40°C to +125°C | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | SBB# |
| ADG419BRMZ-REEL7 ¹ | -40°C to +125°C | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | SBB# |
| ADG419TQ | -55°C to +125°C | 8-Lead Ceramic Dual In-Line Package [CERDIP] | Q-8 | |

¹ Z = RoHS Compliant Part, # denotes that RoHS compliant part is top or bottom marked.

ADG419

NOTES

NOTES

ADG419

NOTES