

FEATURES

- 1.5 pF off source capacitance
- <1 pC charge injection
- 33 V supply range
- 120 Ω on resistance
- Fully specified at ±15 V, +12 V
- No V_L supply required
- 3 V logic-compatible inputs
- Rail-to-rail operation
- 14-lead TSSOP and 12-lead LFCSP
- Typical power consumption < 0.03 μW

APPLICATIONS

- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- Sample-and-hold systems
- Audio signal routing
- Video signal routing
- Communication systems

GENERAL DESCRIPTION

The **ADG1204** is a complementary metal-oxide semiconductor (CMOS) analog multiplexer, comprising four single channels designed on an *i*CMOS (industrial CMOS) process. *i*CMOS® is a modular manufacturing process that combines high voltage CMOS and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no previous generation of high voltage devices has been able to achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and reduced package size.

The ultralow capacitance and charge injection of this multiplexer makes it an ideal solution for data acquisition and sample-and-hold applications, where low glitch and fast settling are required. Fast switching speed coupled with high signal bandwidth makes the device suitable for video signal switching. *i*CMOS construction ensures ultralow power dissipation, making the device ideally suited for portable and battery-powered instruments.

FUNCTIONAL BLOCK DIAGRAM

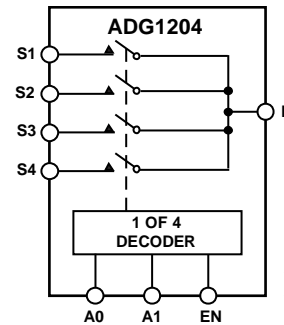


Figure 1.

The **ADG1204** switches one of four inputs to a common output, D, as determined by the 3-bit binary address lines: A0, A1, and EN. Logic 0 on the EN pin disables the device. Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked. All switches exhibit break-before-make switching action.

PRODUCT HIGHLIGHTS

1. 1.5 pF off capacitance (±15 V supply).
2. <1 pC charge injection.
3. 3 V logic-compatible digital inputs: V_{IH} = 2.0 V, V_{IL} = 0.8 V.
4. No V_L logic power supply required.
5. Ultralow power dissipation: <0.03 μW.
6. 14-lead TSSOP and 12-lead, 3 mm × 3 mm LFCSP packages.

ADG1204* Product Page Quick Links

Last Content Update: 08/30/2016

[Comparable Parts](#)

View a parametric search of comparable parts

[Documentation](#)

Application Notes

- AN-1024: How to Calculate the Settling Time and Sampling Rate of a Multiplexer
- AN-874: Operating the ADG12xx Series of Parts with 5 V Supplies and the Impact on Performance

Data Sheet

- ADG1204: Low Capacitance, Low Charge Injection, ± 15 V/ ± 12 V 4:1 iCMOS Multiplexer Data Sheet

[Reference Designs](#)

- CN0292

[Reference Materials](#)

Informational

- iCMOS Technology Enabling the +/-10V World

Product Selection Guide

- Switches and Multiplexers Product Selection Guide

Technical Articles

- CMOS Switches Offer High Performance in Low Power, Wideband Applications
- Data-acquisition system uses fault protection

[Design Resources](#)

- ADG1204 Material Declaration
- PCN-PDN Information
- Quality And Reliability
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TABLE OF CONTENTS

| | | | |
|--------------------------------|---|--|----|
| Features | 1 | ESD Caution..... | 7 |
| Applications..... | 1 | Pin Configurations and Function Descriptions | 8 |
| Functional Block Diagram | 1 | Truth Table | 8 |
| General Description | 1 | Typical Performance Characteristics | 9 |
| Product Highlights | 1 | Test Circuits..... | 12 |
| Revision History | 2 | Terminology | 14 |
| Specifications..... | 3 | Outline Dimensions | 15 |
| Dual Supply | 3 | Ordering Guide | 15 |
| Single Supply | 5 | | |
| Absolute Maximum Ratings..... | 7 | | |

REVISION HISTORY

3/16—Rev. B to Rev. C

| | |
|----------------------------------|------------|
| Changed LFCSP_VQ to LFCSP..... | Throughout |
| Changes to Figure 3..... | 8 |
| Updated Outline Dimensions | 15 |
| Changes to Ordering Guide | 15 |

2/09—Rev. A to Rev. B

| | |
|---|----|
| Changes to Power Requirements, I_{DD} , Digital Inputs = 5 V Parameter, Table 1..... | 4 |
| Changes to Power Requirements, I_{DD} , Digital Inputs = 5 V Parameter, Table 2..... | 6 |
| Updated Outline Dimensions | 15 |

7/06—Rev. 0 to Rev. A

| | |
|---|-----------|
| Updated Format..... | Universal |
| Changes to Table 1..... | 3 |
| Changes to Table 2..... | 5 |
| Changes to the Terminology Section..... | 14 |

7/05—Revision 0: Initial Version

SPECIFICATIONS

DUAL SUPPLY

$V_{DD} = 15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, GND = 0 V, unless otherwise noted.

Table 1.

| Parameter | Y Version ¹ | | | Unit | Test Conditions/Comments |
|--|------------------------|----------------|----------------------|-------------------|--|
| | 25°C | -40°C to +85°C | -40°C to +125°C | | |
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | V_{DD} to V_{SS} | V | |
| On Resistance (R_{ON}) | 120 | | | Ω typ | $V_S = \pm 10\text{ V}$, $I_S = -1\text{ mA}$; see Figure 21 |
| | 190 | 230 | 260 | Ω max | $V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$ |
| On Resistance Match Between Channels (ΔR_{ON}) | 3.5 | | | Ω typ | $V_S = \pm 10\text{ V}$, $I_S = -1\text{ mA}$ |
| | 6 | 10 | 12 | Ω max | |
| On Resistance Flatness ($R_{FLAT(ON)}$) | 20 | | | Ω typ | $V_S = -5\text{ V}, 0\text{ V}, +5\text{ V}$; $I_S = -1\text{ mA}$ |
| | 57 | 72 | 79 | Ω max | |
| LEAKAGE CURRENTS | | | | | |
| Source Off Leakage, I_S (OFF) | ± 0.02 | | | nA typ | $V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$ |
| | ± 0.1 | ± 0.6 | ± 1 | nA max | $V_S = \pm 10\text{ V}$, $V_D = \mp 10\text{ V}$; see Figure 22 |
| Drain Off Leakage, I_D (OFF) | ± 0.02 | | | nA typ | $V_S = \pm 10\text{ V}$, $V_D = \mp 10\text{ V}$; see Figure 22 |
| | ± 0.1 | ± 0.6 | ± 1 | nA max | |
| Channel On Leakage, I_D , I_S (ON) | ± 0.02 | | | nA typ | $V_S = V_D = \pm 10\text{ V}$; see Figure 23 |
| | ± 0.2 | ± 0.6 | ± 1 | nA max | |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, V_{INH} | | | 2.0 | V min | |
| Input Low Voltage, V_{INL} | | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | 0.005 | | | μA typ | $V_{IN} = V_{INL}$ or V_{INH} |
| | | | ± 0.1 | μA max | |
| Digital Input Capacitance, C_{IN} | 2.5 | | | pF typ | |
| DYNAMIC CHARACTERISTICS² | | | | | |
| Transition Time, t_{TRANS} | 120 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 150 | 180 | 200 | ns max | $V_S = 10\text{ V}$; see Figure 24 |
| t_{ON} (EN) | 70 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 85 | 100 | 110 | ns max | $V_S = 10\text{ V}$; see Figure 26 |
| t_{OFF} (EN) | 90 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 110 | 135 | 155 | ns max | $V_S = 10\text{ V}$; see Figure 26 |
| Break-Before-Make Time Delay, t_D | 25 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | | | 10 | ns min | $V_{S1} = V_{S2} = 10\text{ V}$; see Figure 25 |
| Charge Injection | -0.7 | | | pC typ | $V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 27 |
| Off Isolation | 85 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 28 |
| Channel-to-Channel Crosstalk | 80 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 30 |
| Total Harmonic Distortion + Noise | 0.15 | | | % typ | $R_L = 10\text{ k}\Omega$, 5 V rms , $f = 20\text{ Hz}$ to 20 kHz ; see Figure 31 |
| Bandwidth -3 dB | 800 | | | MHz typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 29 |
| C_S (OFF) | 1.2 | | | pF typ | $f = 1\text{ MHz}$, $V_S = 0\text{ V}$ |
| | 1.5 | | | pF max | $f = 1\text{ MHz}$, $V_S = 0\text{ V}$ |
| C_D (OFF) | 3.6 | | | pF typ | $f = 1\text{ MHz}$, $V_S = 0\text{ V}$ |
| | 4.2 | | | pF max | $f = 1\text{ MHz}$, $V_S = 0\text{ V}$ |
| C_D , C_S (ON) | 5.5 | | | pF typ | $f = 1\text{ MHz}$, $V_S = 0\text{ V}$ |
| | 6.5 | | | pF max | $f = 1\text{ MHz}$, $V_S = 0\text{ V}$ |

| Parameter | Y Version ¹ | | | Unit | Test Conditions/Comments |
|--------------------|------------------------|----------------|-----------------|-------------------|---|
| | 25°C | -40°C to +85°C | -40°C to +125°C | | |
| POWER REQUIREMENTS | | | | | $V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$ |
| I_{DD} | 0.001 | | | $\mu\text{A typ}$ | Digital inputs = 0 V or V_{DD} |
| | | | 1.0 | $\mu\text{A max}$ | |
| I_{DD} | 170 | | | $\mu\text{A typ}$ | Digital inputs = 5 V |
| | | | 285 | $\mu\text{A max}$ | |
| I_{SS} | 0.001 | | | $\mu\text{A typ}$ | Digital inputs = 0 V or V_{DD} |
| | | | 1.0 | $\mu\text{A max}$ | |
| I_{SS} | 0.001 | | | $\mu\text{A typ}$ | Digital inputs = 5 V |
| | | | 1.0 | $\mu\text{A max}$ | |

¹ Y version temperature range is -40°C to +125°C.

² Guaranteed by design, not subject to production test.

SINGLE SUPPLY

$V_{DD} = 12\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 2.

| Parameter | Y Version ¹ | | | Unit | Test Conditions/Comments |
|--|------------------------|----------------|-----------------|-------------------|---|
| | 25°C | -40°C to +85°C | -40°C to +125°C | | |
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | 0 V to V_{DD} | V | |
| On Resistance (R_{ON}) | 300 | | | Ω typ | $V_S = 0\text{ V to }10\text{ V}$, $I_S = -1\text{ mA}$; see Figure 21 |
| | 475 | 567 | 625 | Ω max | $V_{DD} = 10.8\text{ V}$, $V_{SS} = 0\text{ V}$ |
| On Resistance Match Between Channels (ΔR_{ON}) | 5 | | | Ω typ | $V_S = 0\text{ V to }10\text{ V}$, $I_S = -1\text{ mA}$ |
| | 16 | 26 | 27 | Ω max | |
| On Resistance Flatness ($R_{FLAT(ON)}$) | 60 | | | Ω typ | $V_S = 3\text{ V, }6\text{ V, }9\text{ V}$; $I_S = -1\text{ mA}$ |
| LEAKAGE CURRENTS | | | | | |
| Source Off Leakage, I_S (OFF) | ± 0.02 | | | nA typ | $V_{DD} = 13.2\text{ V}$ |
| | ± 0.1 | ± 0.6 | ± 1 | nA max | $V_S = 1\text{ V/}10\text{ V}$, $V_D = 10\text{ V/}1\text{ V}$; see Figure 22 |
| Drain Off Leakage, I_D (OFF) | ± 0.02 | | | nA typ | $V_S = 1\text{ V/}10\text{ V}$, $V_D = 10\text{ V/}1\text{ V}$; see Figure 22 |
| | ± 0.1 | ± 0.6 | ± 1 | nA max | |
| Channel On Leakage, I_D , I_S (ON) | ± 0.02 | | | nA typ | $V_S = V_D = 1\text{ V or }10\text{ V}$; see Figure 23 |
| | ± 0.2 | ± 0.6 | ± 1 | nA max | |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, V_{INH} | | | 2.0 | V min | |
| Input Low Voltage, V_{INL} | | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | 0.001 | | | μA typ | $V_{IN} = V_{INL}$ or V_{INH} |
| | | | ± 0.1 | μA max | |
| Digital Input Capacitance, C_{IN} | 2.5 | | | pF typ | |
| DYNAMIC CHARACTERISTICS² | | | | | |
| Transition Time, t_{TRANS} | 150 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 190 | 240 | 265 | ns max | $V_S = 8\text{ V}$; see Figure 24 |
| t_{ON} (EN) | 95 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 120 | 150 | 170 | ns max | $V_S = 8\text{ V}$; see Figure 26 |
| t_{OFF} (EN) | 100 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 125 | 155 | 170 | ns max | $V_S = 8\text{ V}$; see Figure 26 |
| Break-Before-Make Time Delay, t_D | 50 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | | | 10 | ns min | $V_{S1} = V_{S2} = 8\text{ V}$; see Figure 25 |
| Charge Injection | -0.4 | | | pC typ | $V_S = 6\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 27 |
| Off Isolation | 85 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 28 |
| Channel-to-Channel Crosstalk | 80 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 30 |
| Bandwidth -3 db | 550 | | | MHz typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 29 |
| C_S (OFF) | 1.2 | | | pF typ | $f = 1\text{ MHz}$; $V_S = 6\text{ V}$ |
| | 1.5 | | | pF max | $f = 1\text{ MHz}$; $V_S = 6\text{ V}$ |
| C_D (OFF) | 3.6 | | | pF typ | $f = 1\text{ MHz}$; $V_S = 6\text{ V}$ |
| | 4.2 | | | pF max | $f = 1\text{ MHz}$; $V_S = 6\text{ V}$ |
| C_D , C_S (ON) | 5.5 | | | pF typ | $f = 1\text{ MHz}$; $V_S = 6\text{ V}$ |
| | 6.5 | | | pF max | $f = 1\text{ MHz}$; $V_S = 6\text{ V}$ |

| Parameter | Y Version ¹ | | | Unit | Test Conditions/Comments |
|--------------------|------------------------|----------------|-----------------|--|----------------------------------|
| | 25°C | -40°C to +85°C | -40°C to +125°C | | |
| POWER REQUIREMENTS | | | | | $V_{DD} = 13.2\text{ V}$ |
| I_{DD} | 0.001 | | 1.0 | $\mu\text{A typ}$ $\mu\text{A max}$ | Digital inputs = 0 V or V_{DD} |
| I_{DD} | 170 | | 285 | $\mu\text{A typ}$ $\mu\text{A max}$ | Digital inputs = 5 V |

¹ Y version temperature range is -40°C to +125°C.

² Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

| Parameter | Rating |
|---|--|
| V_{DD} to V_{SS} | 35 V |
| V_{DD} to GND | -0.3 V to +25 V |
| V_{SS} to GND | +0.3 V to -25 V |
| Analog Inputs ¹ | $V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first |
| Digital Inputs ¹ | GND - 0.3 V to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first |
| Peak Current, S or D | 100 mA (pulsed at 1 ms, 10% duty cycle maximum) |
| Continuous Current | 45 mA |
| Operating Temperature Range | |
| Automotive (Y Version) | -40°C to +125°C |
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature | 150°C |
| 14-Lead TSSOP, θ_{JA} Thermal Impedance (4-Layer Board) | 112°C/W |
| 12-Lead LFCSP, θ_{JA} Thermal Impedance | 80°C/W |
| Reflow Soldering Peak Temperature, Pb Free | 260°C |

¹ Overvoltages at IN, S, or D are clamped by internal diodes. Current must be limited to the maximum ratings given.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

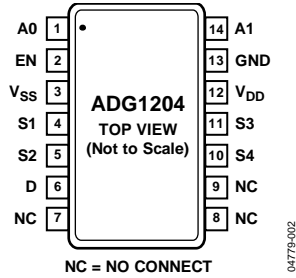
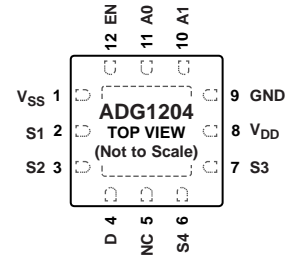


Figure 2. TSSOP Pin Configuration



NOTES
 1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.
 2. THE EXPOSED PAD MUST BE TIED TO SUBSTRATE, V_{SS}.

Figure 3. LFCSP Pin Configuration

Table 4. Pin Function Descriptions

| Pin No. | | Mnemonic | Description |
|---------|-------|-----------------|---|
| TSSOP | LFCSP | | |
| 1 | 11 | A0 | Logic Control Input. |
| 2 | 12 | EN | Active High Digital Input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine on switches. |
| 3 | 1 | V _{SS} | Most Negative Power Supply Potential. |
| 4 | 2 | S1 | Source Terminal. Can be an input or an output. |
| 5 | 3 | S2 | Source Terminal. Can be an input or an output. |
| 6 | 4 | D | Drain Terminal. Can be an input or an output. |
| 7 to 9 | 5 | NC | No Connection. |
| 10 | 6 | S4 | Source Terminal. Can be an input or an output. |
| 11 | 7 | S3 | Source Terminal. Can be an input or an output. |
| 12 | 8 | V _{DD} | Most Positive Power Supply Potential. |
| 13 | 9 | GND | Ground (0 V) Reference. |
| 14 | 10 | A1 | Logic Control Input. |

TRUTH TABLE

Table 5.

| EN | A1 | A0 | S1 | S2 | S3 | S4 |
|----|----|----|-----|-----|-----|-----|
| 0 | X | X | Off | Off | Off | Off |
| 1 | 0 | 0 | On | Off | Off | Off |
| 1 | 0 | 1 | Off | On | Off | Off |
| 1 | 1 | 0 | Off | Off | On | Off |
| 1 | 1 | 1 | Off | Off | Off | On |

TYPICAL PERFORMANCE CHARACTERISTICS

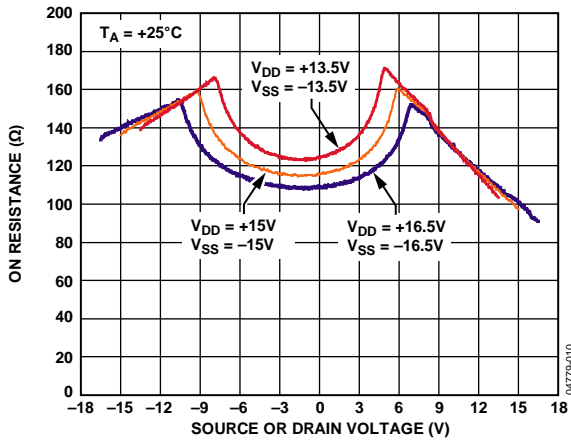


Figure 4. On Resistance as a Function of V_D (V_S), Dual Supply

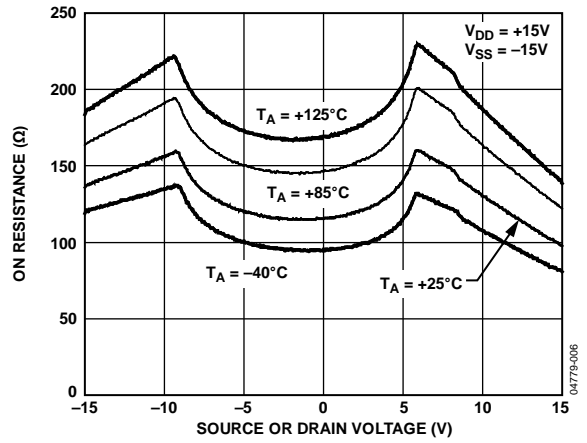


Figure 7. On Resistance as a Function of V_D (V_S) for Different Temperatures, Dual Supply

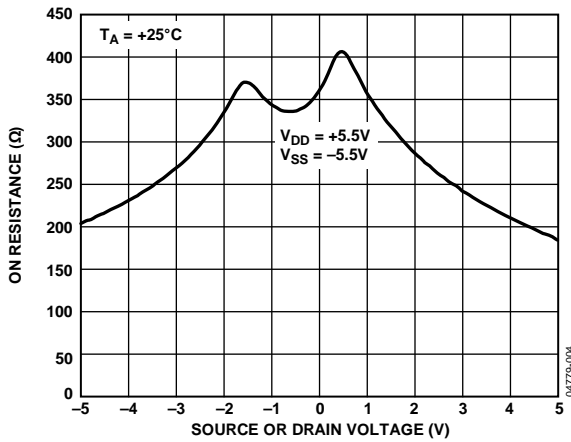


Figure 5. On Resistance as a Function of V_D (V_S), Dual Supply

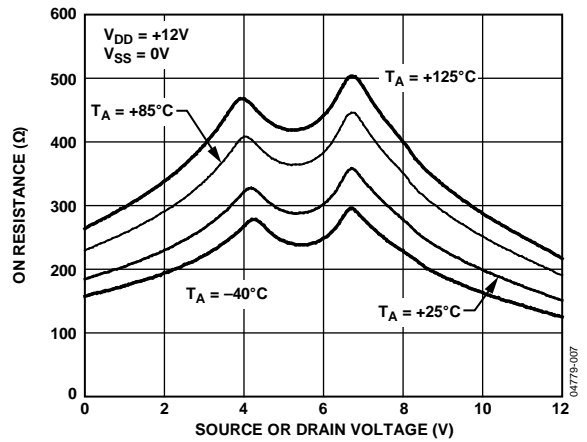


Figure 8. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply

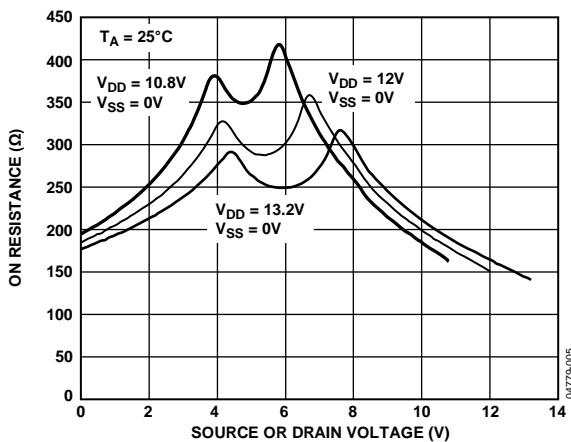


Figure 6. On Resistance as a Function of V_D (V_S), Single Supply

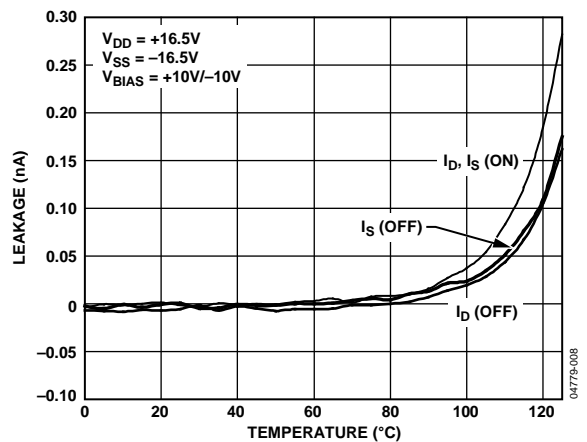


Figure 9. Leakage Currents as a Function of Temperature, Dual Supply

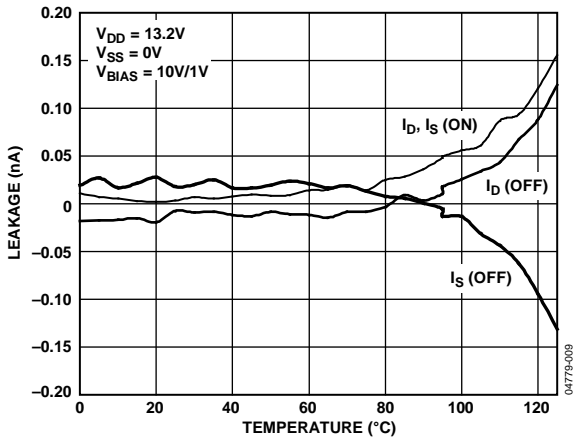


Figure 10. Leakage Currents as a Function of Temperature, Single Supply

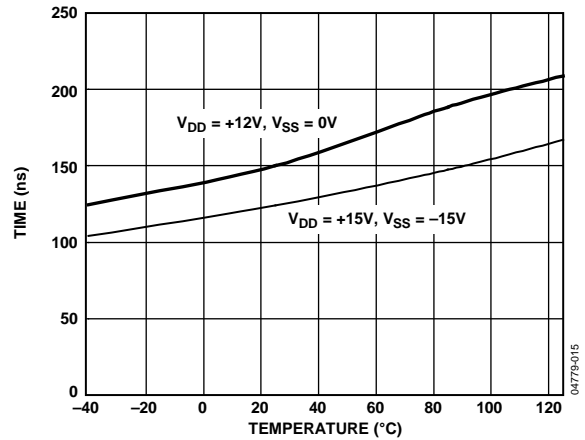


Figure 13. Transition Times vs. Temperature

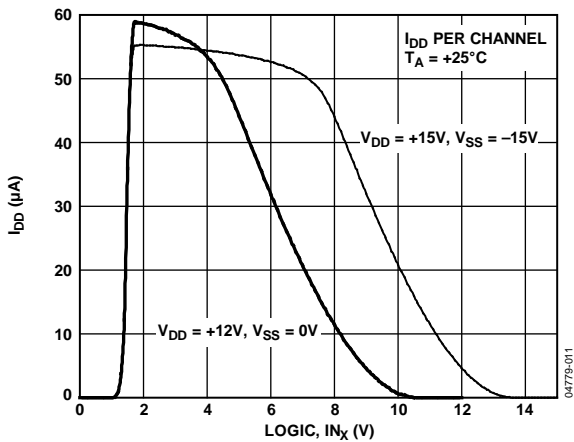


Figure 11. I_{DD} vs. Logic Level

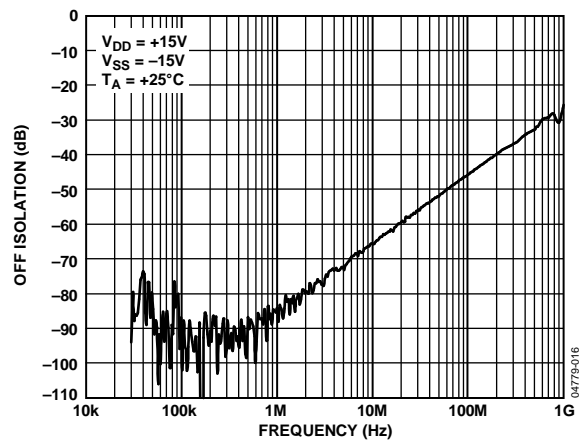


Figure 14. Off Isolation vs. Frequency

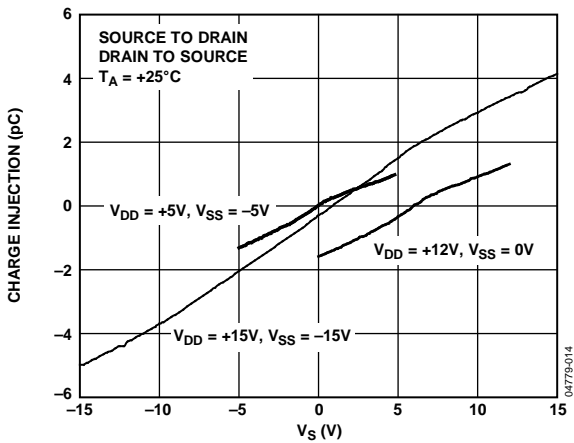


Figure 12. Charge Injection vs. Source Voltage

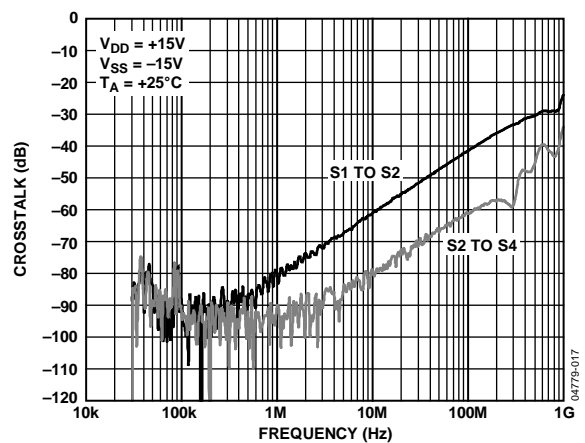


Figure 15. Crosstalk vs. Frequency

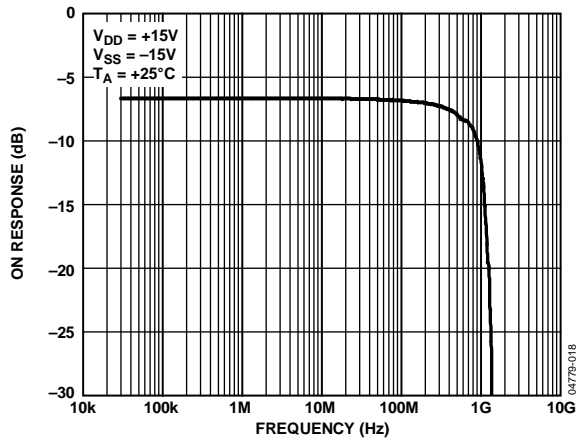


Figure 16. On Response vs. Frequency

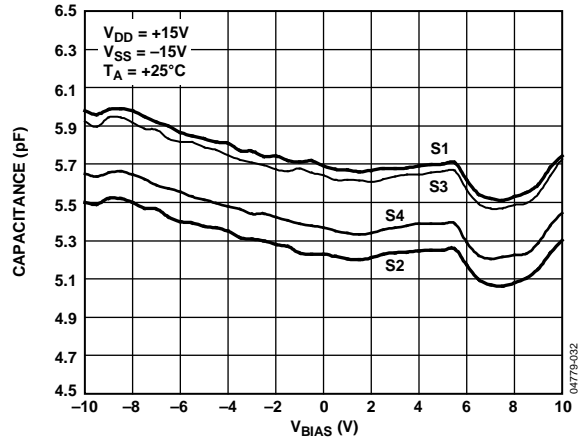


Figure 19. On Capacitance vs. Source Voltage

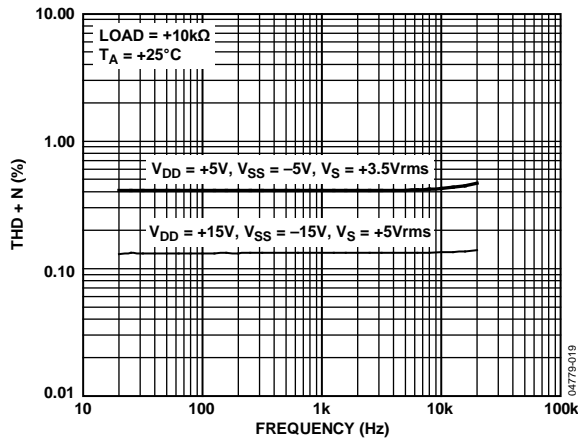


Figure 17. THD + N vs. Frequency

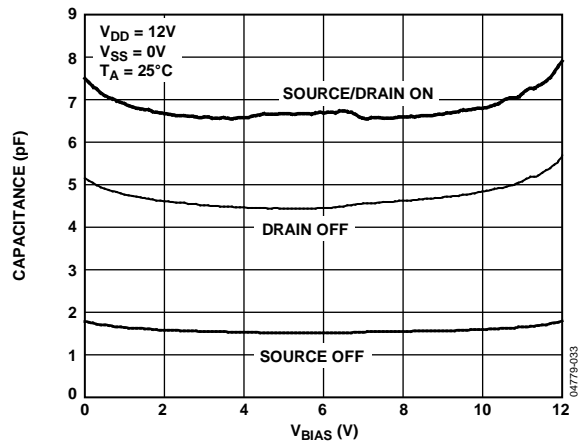


Figure 20. Capacitance vs. Source Voltage, Single Supply

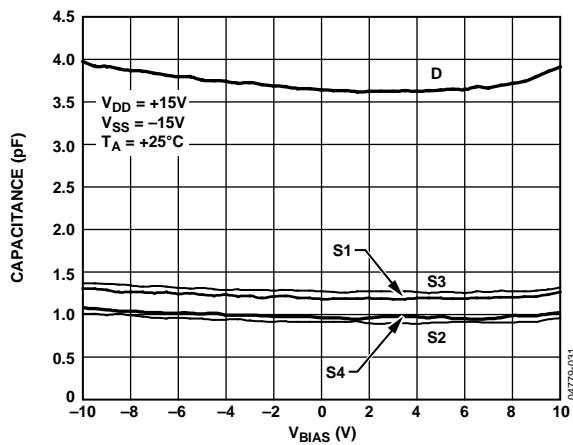


Figure 18. Off Capacitance vs. Source Voltage

TEST CIRCUITS

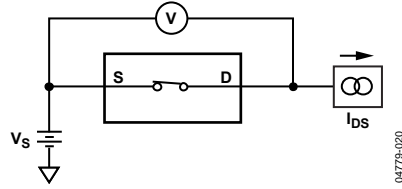


Figure 21. On Resistance

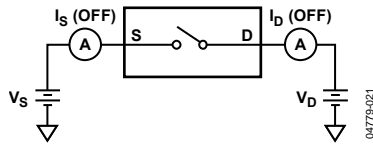


Figure 22. Off Leakage

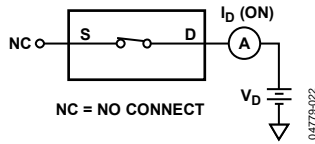


Figure 23. On Leakage

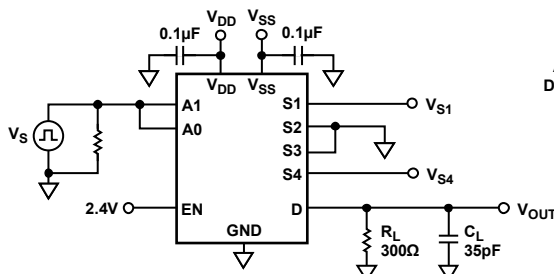


Figure 24. Address to Output Switching Times

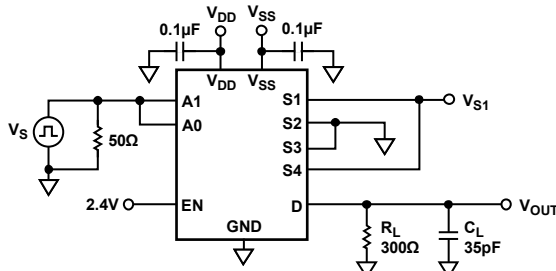
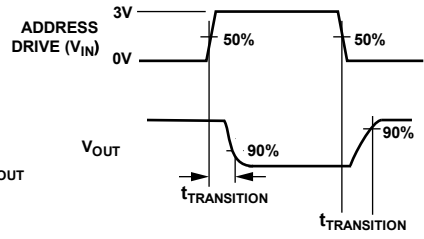


Figure 25. Break-Before-Make Time Delay

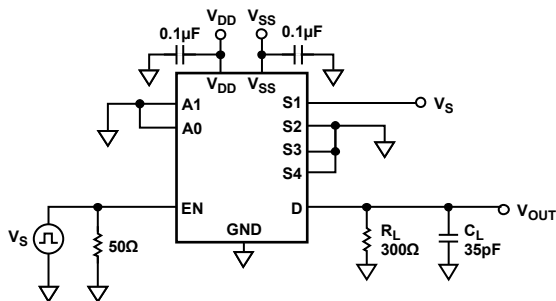
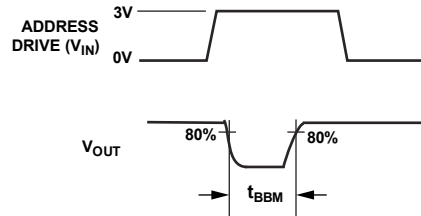
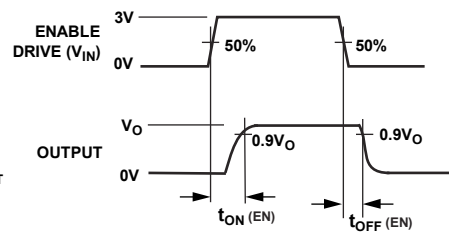


Figure 26. Enable-to-Output Switching Delay



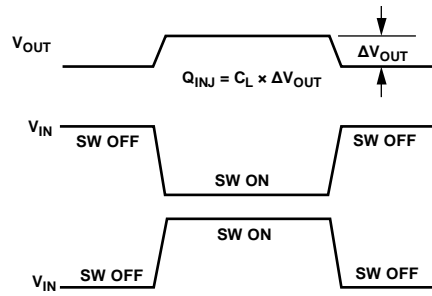
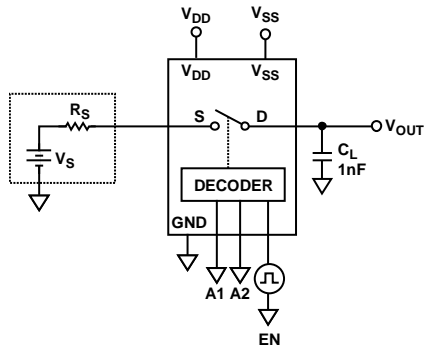
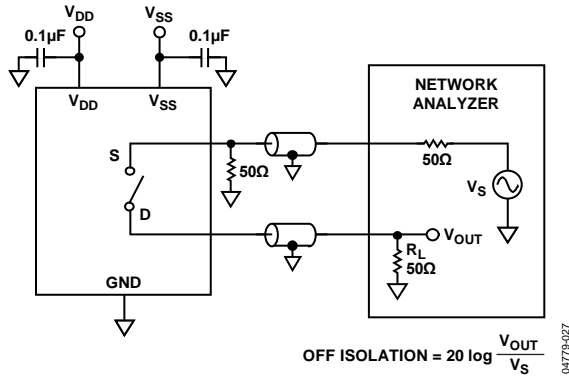
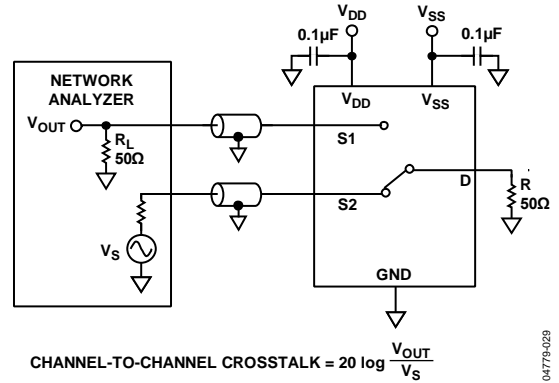


Figure 27. Charge Injection



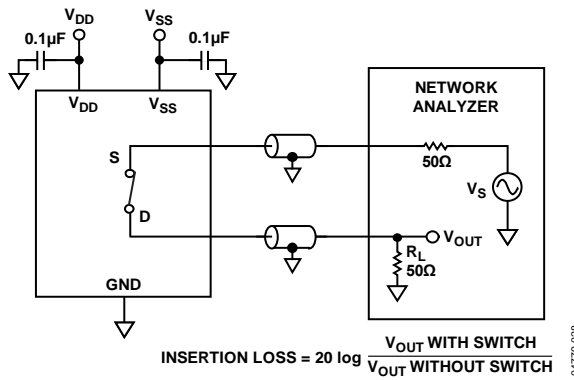
$$\text{OFF ISOLATION} = 20 \log \frac{V_{\text{OUT}}}{V_S}$$

Figure 28. Off Isolation



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \log \frac{V_{\text{OUT}}}{V_S}$$

Figure 30. Channel-to-Channel Crosstalk



$$\text{INSERTION LOSS} = 20 \log \frac{V_{\text{OUT WITH SWITCH}}}{V_{\text{OUT WITHOUT SWITCH}}}$$

Figure 29. Bandwidth

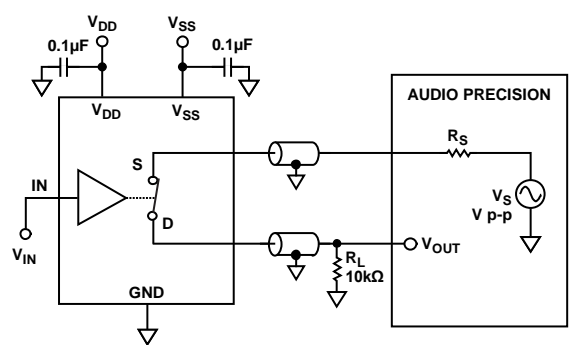


Figure 31. THD + Noise

TERMINOLOGY

I_{DD}

The positive supply current.

I_{SS}

The negative supply current.

$V_D (V_S)$

The analog voltage on Terminal D and Terminal S.

R_{ON}

The ohmic resistance between D and S.

$R_{FLAT(ON)}$

Flatness is defined as the difference between the maximum and minimum value of on resistance, as measured over the specified analog signal range.

$I_S (OFF)$

The source leakage current with the switch off.

$I_D (OFF)$

The drain leakage current with the switch off.

$I_D, I_S (ON)$

The channel leakage current with the switch on.

V_{INL}

The maximum input voltage for Logic 0.

V_{INH}

The minimum input voltage for Logic 1.

$I_{INL} (I_{INH})$

The input current of the digital input.

$C_S (OFF)$

The off switch source capacitance, which is measured with reference to ground.

$C_D (OFF)$

The off switch drain capacitance, which is measured with reference to ground.

$C_D, C_S (On)$

The on switch capacitance, measured with reference to ground.

C_{IN}

The digital input capacitance.

$t_{ON} (EN)$

The delay between applying the digital control input and the output switching on.

$t_{OFF} (EN)$

The delay between applying the digital control input and the output switching off.

t_{TRANS}

The delay time between the 50% and 90% points of the digital input and switch on condition when switching from one address state to another.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation

A measure of unwanted signal coupling through an off switch.

Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth

The frequency at which the output is attenuated by -3 dB.

On Response

The frequency response of the on switch.

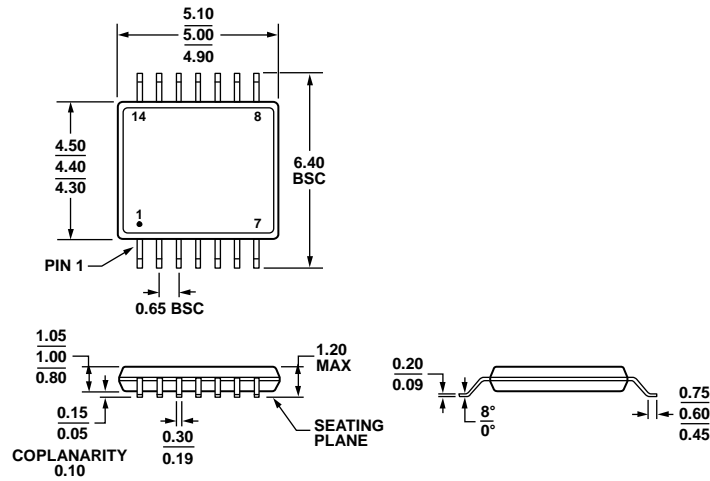
Insertion Loss

The loss due to the on resistance of the switch.

Total Harmonic Distortion + Noise (THD + N)

The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

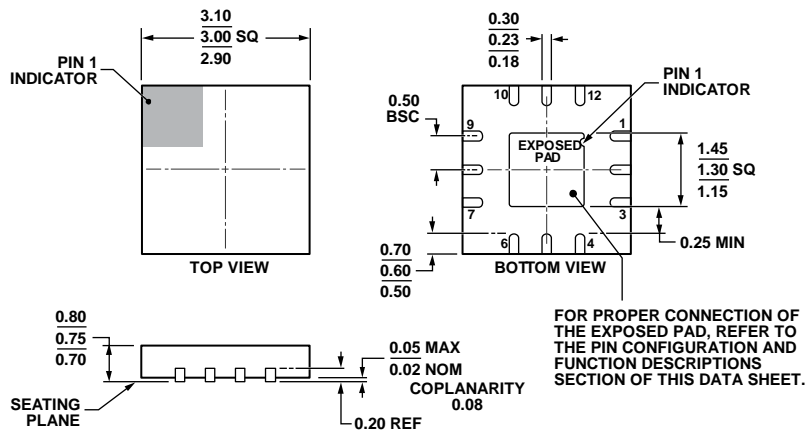
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 32. 14-Lead Thin Shrink Small Outline Package [TSSOP] (RU-14)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WEED.

Figure 33. 12-Lead Lead Frame Chip Scale Package [LFCSP] 3 mm x 3 mm Body and 0.75 mm Package Height (CP-12-4)

Dimensions shown in millimeters

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option |
|--------------------|-------------------|---|----------------|
| ADG1204YRUZ | -40°C to +125°C | 14-Lead Thin Shrink Small Outline Package [TSSOP] | RU-14 |
| ADG1204YRUZ-REEL | -40°C to +125°C | 14-Lead Thin Shrink Small Outline Package [TSSOP] | RU-14 |
| ADG1204YRUZ-REEL7 | -40°C to +125°C | 14-Lead Thin Shrink Small Outline Package [TSSOP] | RU-14 |
| ADG1204YCPZ-500RL7 | -40°C to +125°C | 12-Lead Lead Frame Chip Scale Package [LFCSP] | CP-12-4 |
| ADG1204YCPZ-REEL7 | -40°C to +125°C | 12-Lead Lead Frame Chip Scale Package [LFCSP] | CP-12-4 |

¹ Z = RoHS Compliant Part.

NOTES