Improved Second Source to the EL2020

ADEL2020

FEATURES

Ideal for Video Applications
- 0.02% Differential Gain
- 0.04° Differential Phase
- 0.1 dB Bandwidth to 25 MHz (G = +2)

High Speed
- 90 MHz Bandwidth (–3 dB)
- 500 V/μs Slew Rate
- 60 ns Settling Time to 0.1% (V_O = 10 V Step)

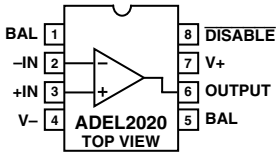
Low Noise
- 2.9 nV/√Hz Input Voltage Noise

Low Power
- 6.8 mA Supply Current
- 2.1 mA Supply Current (Power-Down Mode)

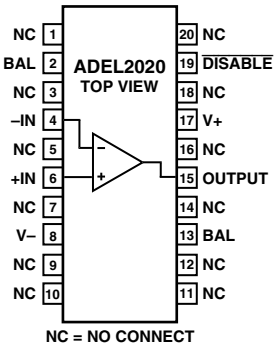
High Performance Disable Function
- Turn-Off Time of 100 ns
- Input to Output Isolation of 54 dB (Off State)

CONNECTION DIAGRAMS

8-Lead PDIP (N)



20-Lead SOIC (R)



NC = NO CONNECT

GENERAL DESCRIPTION

The ADEL2020 is an improved second source to the EL2020. This op amp improves on all the key dynamic specifications while offering lower power and lower cost. The ADEL2020 offers 50% more bandwidth and gain flatness of 0.1 dB to beyond 25 MHz. In addition, differential gain and phase are less than 0.05% and 0.05° while driving one back terminated cable (150 Ω).

The ADEL2020 offers other significant improvements. The most important is lower power supply current (33% less than the competition) with higher output drive. Important specifications like voltage noise and offset voltage are less than half of those for the EL2020. The ADEL2020 also provides an improved disable feature. The disable time (to high output impedance) is 100 ns with guaranteed break before make. The ADEL2020 is offered for the industrial temperature range of –40°C to +85°C and comes in both PDIP and SOIC packages.

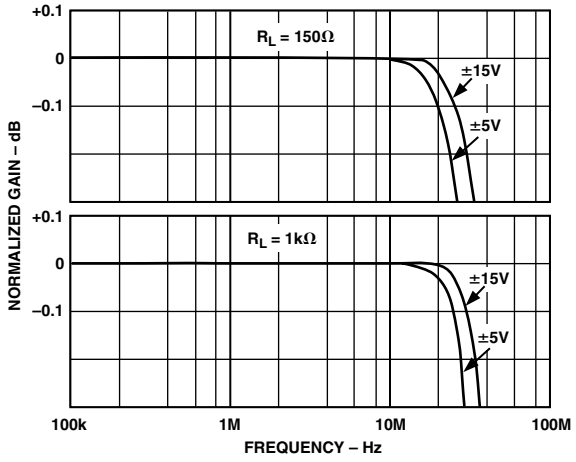


Figure 1. Fine-Scale Gain (Normalized) vs. Frequency for Various Supply Voltages, R_F = 750 Ω, Gain = +2

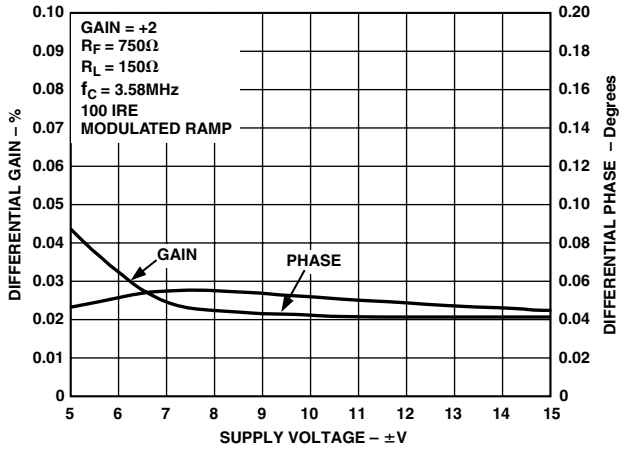


Figure 2. Differential Gain and Phase vs. Supply Voltage

REV. A

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ADEL2020* Product Page Quick Links

Last Content Update: 08/30/2016

Comparable Parts

View a parametric search of comparable parts

Documentation

Application Notes

- AN-402: Replacing Output Clamping Op Amps with Input Clamping Amps
- AN-417: Fast Rail-to-Rail Operational Amplifiers Ease Design Constraints in Low Voltage High Speed Systems
- AN-581: Biasing and Decoupling Op Amps in Single Supply Applications

Data Sheet

- ADEL2020: Improved Second Source to the EL2020 Data Sheet

Tools and Simulations

- Op Amp Stability with Capacitive Load
- Power Dissipation vs Die Temp
- VRMS/dBm/dBu/dBV calculators

Reference Materials

Tutorials

- MT-032: Ideal Voltage Feedback (VFB) Op Amp
- MT-033: Voltage Feedback Op Amp Gain and Bandwidth
- MT-047: Op Amp Noise
- MT-048: Op Amp Noise Relationships: 1/f Noise, RMS Noise, and Equivalent Noise Bandwidth
- MT-049: Op Amp Total Output Noise Calculations for Single-Pole System
- MT-050: Op Amp Total Output Noise Calculations for Second-Order System
- MT-052: Op Amp Noise Figure: Don't Be Misled
- MT-053: Op Amp Distortion: HD, THD, THD + N, IMD, SFDR, MTPR
- MT-056: High Speed Voltage Feedback Op Amps
- MT-058: Effects of Feedback Capacitance on VFB and CFB Op Amps
- MT-059: Compensating for the Effects of Input Capacitance on VFB and CFB Op Amps Used in Current-to-Voltage Converters
- MT-060: Choosing Between Voltage Feedback and Current Feedback Op Amps

Design Resources

- ADEL2020 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

Discussions

View all ADEL2020 EngineerZone Discussions

Sample and Buy

Visit the product page to see pricing options

Technical Support

Submit a technical question or find your regional support number

ADEL2020–SPECIFICATIONS (@ T_A = 25°C, V_S = ±15 V dc, R_L = 150 Ω, unless otherwise noted.)

Parameter	Conditions	Temperature	ADEL2020A Min	Typ	Max	Unit
INPUT OFFSET VOLTAGE				1.5	7.5	mV
		T_{MIN} to T_{MAX}		2.0	10.0	mV
Offset Voltage Drift				7		µV/°C
COMMON-MODE REJECTION	V_{CM} = ±10 V					
V_{OS}		T_{MIN} to T_{MAX}	50	64		dB
±Input Current		T_{MIN} to T_{MAX}		0.1	1.0	µA/V
POWER SUPPLY REJECTION	V_S = ±4.5 V to ±18 V					
V_{OS}		T_{MIN} to T_{MAX}	65	72		dB
±Input Current		T_{MIN} to T_{MAX}		0.05	0.5	µA/V
INPUT BIAS CURRENT	–Input	T_{MIN} to T_{MAX}		0.5	7.5	µA
	+Input	T_{MIN} to T_{MAX}		1	15	µA
INPUT CHARACTERISTICS						
+Input Resistance			1	10		MΩ
–Input Resistance				40		Ω
+Input Capacitance				2		pF
OPEN-LOOP TRANSRESISTANCE	V_O = ±10 V					
	R_L = 400 Ω	T_{MIN} to T_{MAX}	1	3.5		MΩ
OPEN-LOOP DC VOLTAGE GAIN	R_L = 400 Ω, V_{OUT} = ±10 V	T_{MIN} to T_{MAX}	80	100		dB
	R_L = 100 Ω, V_{OUT} = ±2.5 V	T_{MIN} to T_{MAX}	76	88		dB
OUTPUT VOLTAGE SWING	R_L = 400 Ω	T_{MIN} to T_{MAX}	±12.0	±13.0		V
Short-Circuit Current				150		mA
Output Current		T_{MIN} to T_{MAX}	30	60		mA
POWER SUPPLY						
Operating Range			±3.0		±18	V
Quiescent Current		T_{MIN} to T_{MAX}		6.8	10.0	mA
Power-Down Current		T_{MIN} to T_{MAX}		2.1	3.0	mA
Disable Pin Current	Disable Pin = 0 V	T_{MIN} to T_{MAX}		290	400	µA
Min Disable Pin Current to Disable		T_{MIN} to T_{MAX}		30		µA
DYNAMIC PERFORMANCE						
3 dB Bandwidth	G = +1; R_{FB} = 820			90		MHz
	G = +2; R_{FB} = 750			70		MHz
	G = +10; R_{FB} = 680			30		MHz
0.1 dB Bandwidth	G = +2; R_{FB} = 750			25		MHz
Full Power Bandwidth	V_O = 20 V p-p,					
	R_L = 400 Ω			8		MHz
Slew Rate	R_L = 400 Ω, G = +1			500		V/µs
Settling Time to 0.1%	10 V Step, G = –1			60		ns
Differential Gain	f = 3.58 MHz			0.02		%
Differential Phase	f = 3.58 MHz			0.04		Degree
INPUT VOLTAGE NOISE	f = 1 kHz			2.9		nV/$\sqrt{\text{Hz}}$
INPUT CURRENT NOISE	$-I_{IN}$, f = 1 kHz			13		pA/$\sqrt{\text{Hz}}$
	$+I_{IN}$, f = 1 kHz			1.5		pA/$\sqrt{\text{Hz}}$
OUTPUT RESISTANCE	Open Loop (5 MHz)			15		Ω

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2] . . . . . Observe Derating Curves
Output Short Circuit Duration . . . . Observe Derating Curves
Common-Mode Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±6 V
Storage Temperature Range
PDIP and SOIC . . . . . –65°C to +125°C
Operating Temperature Range . . . . . –40°C to +85°C
Lead Temperature Range (Soldering 60 sec) . . . . . 300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Lead PDIP: θ_{JA} = 90°C/W
20-Lead SOIC Package: θ_{JA} = 150°C/W

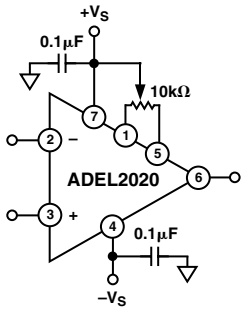


Figure 3. Offset Null Configuration

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the ADEL2020 is limited by the associated rise in junction temperature. For the plastic packages, the maximum safe junction temperature is 145°C. If the maximum is exceeded momentarily, proper circuit operation will be restored as soon as the die temperature is reduced. Leaving the device in the overheated condition for an extended period can result in device burnout. To ensure proper operation, it is important to observe the derating curves in figure 4.

While the ADEL2020 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature is not exceeded under all conditions.

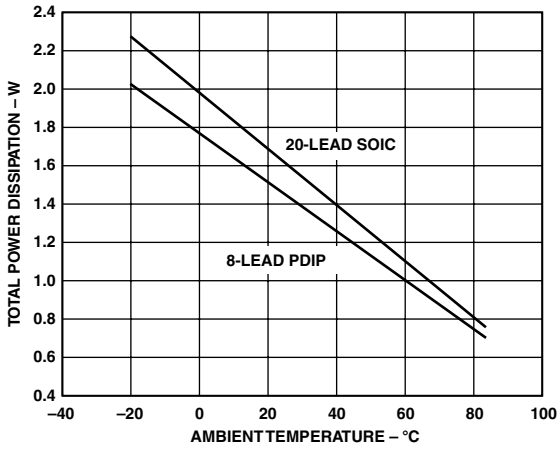


Figure 4. Maximum Power Dissipation vs. Temperature

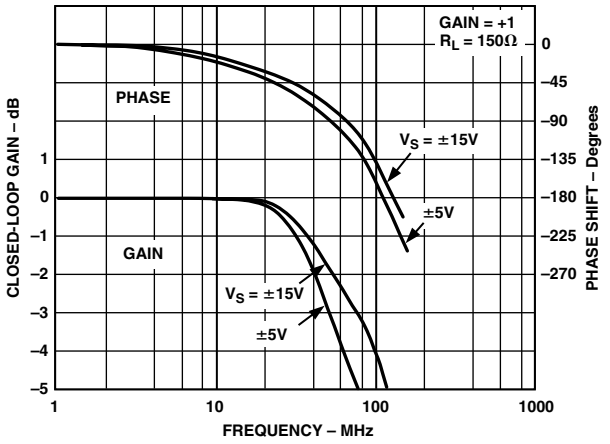
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADEL2020AN	–40°C to +85°C	8-Lead PDIP	N-8
ADEL2020AR-20	–40°C to +85°C	20-Lead SOIC	R-20
ADEL2020AR-20-REEL	–40°C to +85°C	20-Lead SOIC	R-20

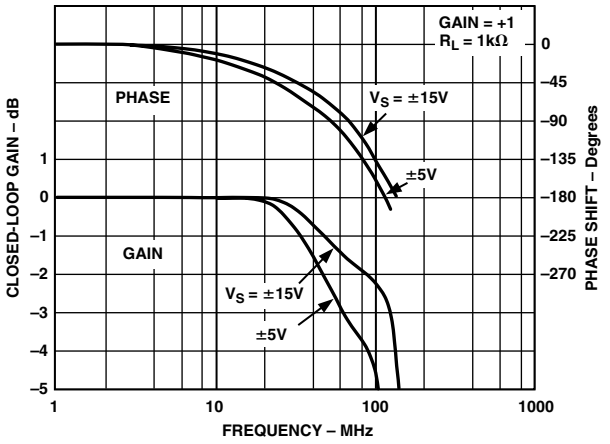
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADEL2020 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

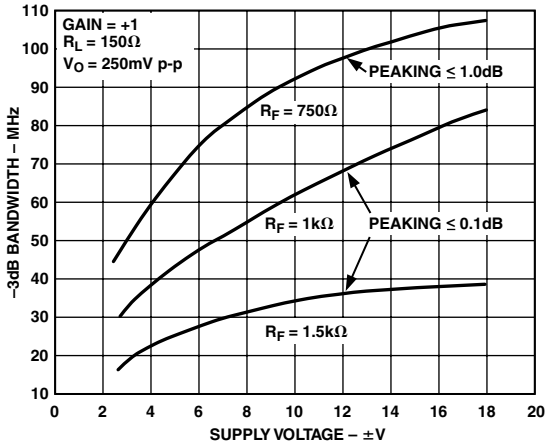
ADEL2020–Typical Performance Characteristics



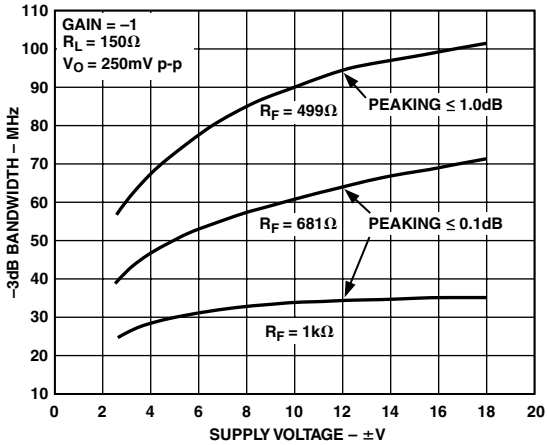
TPC 1. Closed-Loop Gain and Phase vs. Frequency, G = + 1, R_L = 150 Ω, R_F = 1 kΩ for ±15 V, 910 Ω for ±5 V



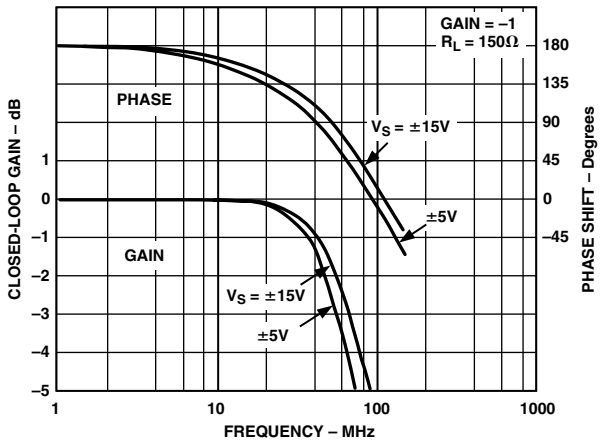
TPC 4. Closed-Loop Gain and Phase vs. Frequency, G = +1, R_L = 1 kΩ, R_F = 1 kΩ for ±15 V, 910 Ω for ±5 V



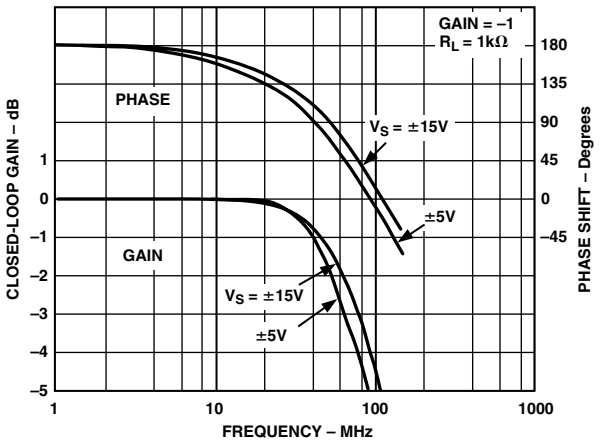
TPC 2. –3 dB Bandwidth vs. Supply Voltage, Gain = +1, R_L = 150 Ω



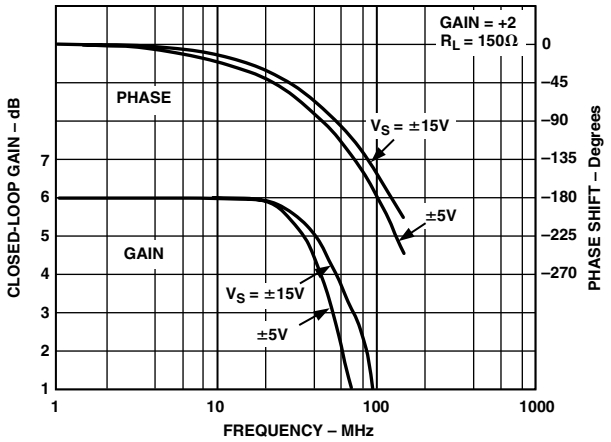
TPC 5. –3 dB Bandwidth vs. Supply Voltage, Gain = –1, R_L = 150 Ω



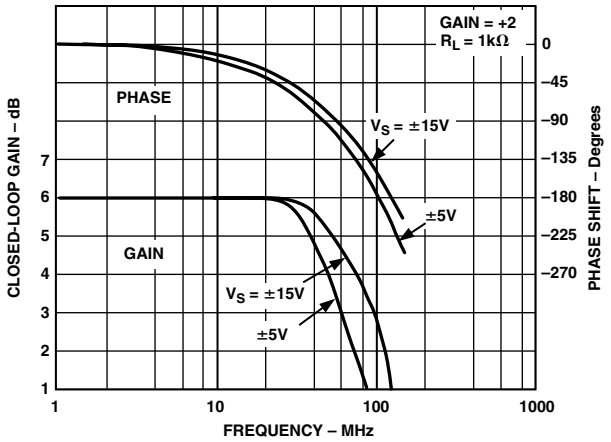
TPC 3. Closed-Loop Gain and Phase vs. Frequency, G = –1, R_L = 150 Ω, R_F = 680 Ω for ±15 V, 620 Ω for ±5 V



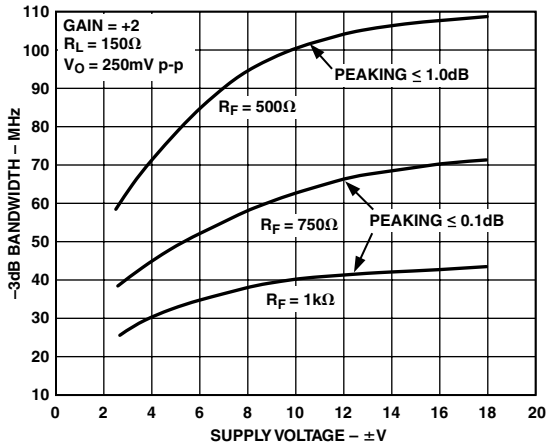
TPC 6. Closed-Loop Gain and Phase vs. Frequency, G = –1, R_L = 1 kΩ, R_F = 680 Ω for V_S = ±15 V, 620 Ω for ±5 V



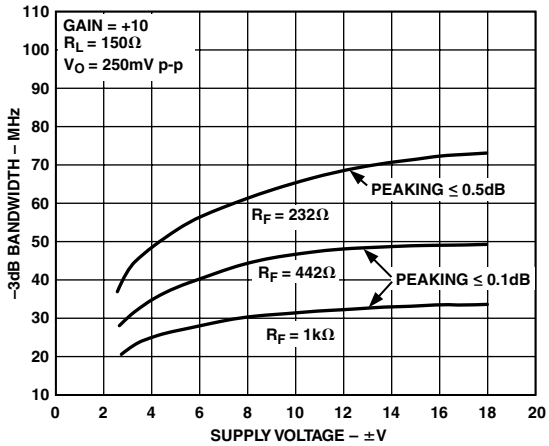
TPC 7. Closed-Loop Gain and Phase vs. Frequency, G = +2, R_L = 150 Ω, R_F = 750 Ω for ±15 V, 715 Ω for ±5 V



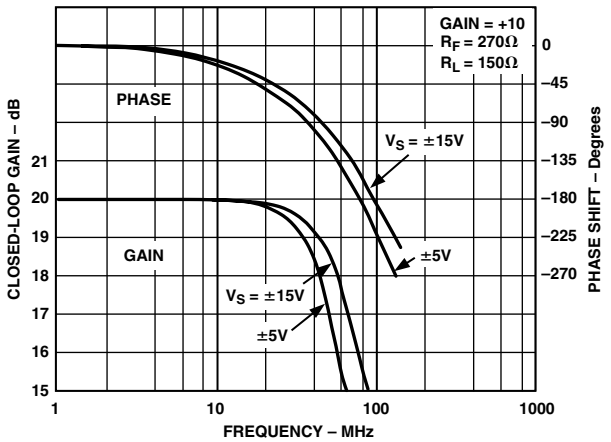
TPC 10. Closed-Loop Gain and Phase vs. Frequency, G = +2, R_L = 1 kΩ, R_F = 750 Ω for ±15 V, 715 Ω for ±5 V



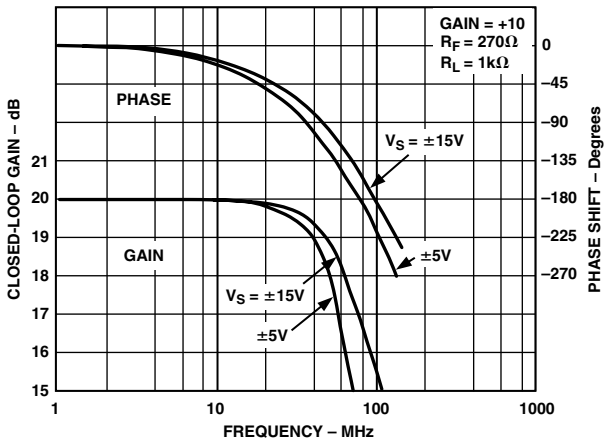
TPC 8. –3 dB Bandwidth vs. Supply Voltage, Gain = +2, R_L = 150 Ω



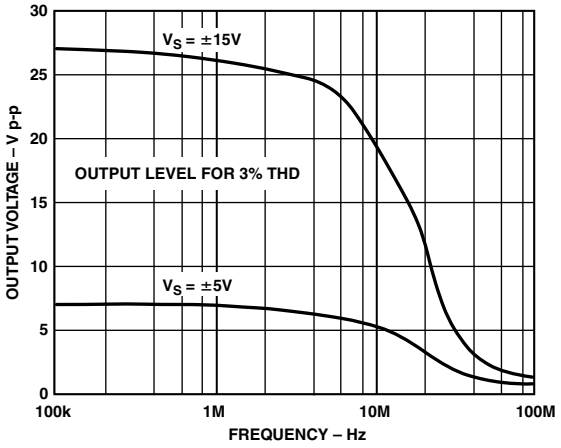
TPC 11. –3 dB Bandwidth vs. Supply Voltage, Gain = +10, R_L = 150 Ω



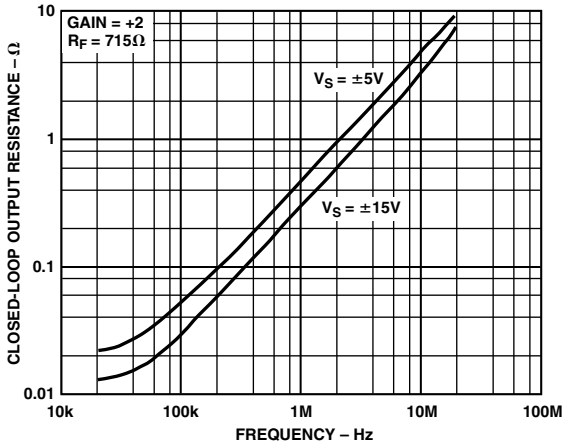
TPC 9. Closed-Loop Gain and Phase vs. Frequency, G = +10, R_L = 150 kΩ



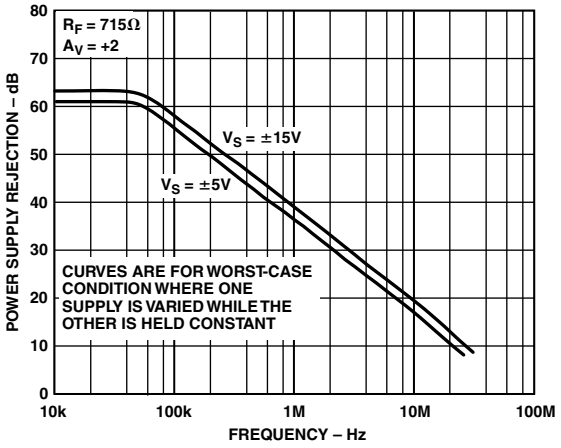
TPC 12. Closed-Loop Gain and Phase vs. Frequency, G = +10, R_L = 1 kΩ



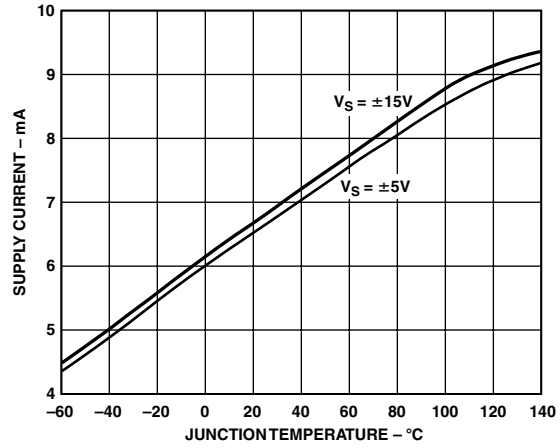
TPC 13. Maximum Undistorted Output Voltage vs. Frequency



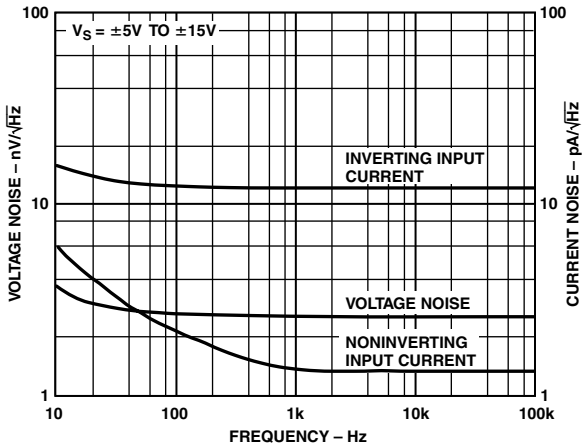
TPC 16. Closed-Loop Output Resistance vs. Frequency



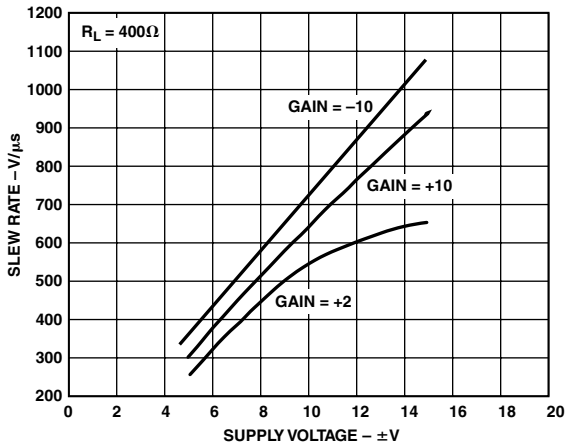
TPC 14. Power Supply Rejection vs. Frequency



TPC 17. Supply Current vs. Junction Temperature



TPC 15. Input Voltage and Current Noise vs. Frequency



TPC 18. Slew Rate vs. Supply Voltage

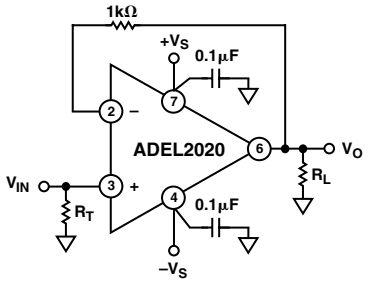


Figure 5. Connection Diagram for A_{VCL} = +1

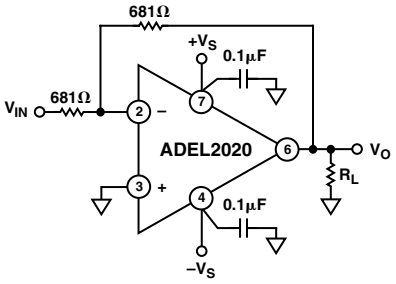


Figure 6. Connection Diagram for A_{VCL} = –1

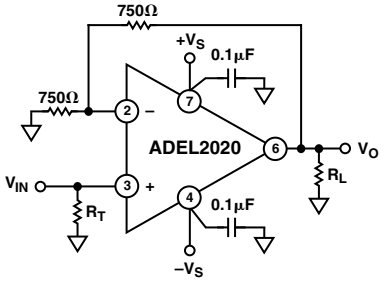


Figure 7. Connection Diagram for A_{VCL} = +2

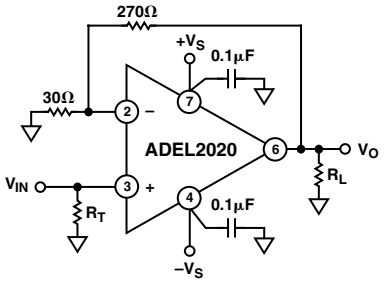


Figure 8. Connection Diagram for A_{VCL} = +10

GENERAL DESIGN CONSIDERATIONS

The ADEL2020 is a current feedback amplifier optimized for use in high performance video and data acquisition systems. Since it uses a current feedback architecture, its closed-loop bandwidth depends on the value of the feedback resistor. The –3 dB bandwidth is also somewhat dependent on the power supply voltage. Lowering the supplies increases the values of internal capacitances, reducing the bandwidth. To compensate for this, smaller values of feedback resistors are used at lower supply voltages.

POWER SUPPLY BYPASSING

Adequate power supply bypassing can be critical when optimizing the performance of a high frequency circuit. Inductance in the power supply leads can contribute to resonant circuits that produce peaking in the amplifier's response. In addition, if large current transients must be delivered to the load, then bypass capacitors (typically greater than 1 μF) will be required to provide the best settling time and lowest distortion. Although the recommended 0.1 μF power supply bypass capacitors will be sufficient in most applications, more elaborate bypassing (such as using two paralleled capacitors) may be required in some cases.

CAPACITIVE LOADS

When used with the appropriate feedback resistor, the ADEL2020 can drive capacitive loads exceeding 1000 pF directly without oscillation. Another method of compensating for large load capacitance is to insert a resistor in series with the loop output. In most cases, less than 50 Ω is all that is needed to achieve an extremely flat gain response.

OFFSET NULLING

A 10 kΩ pot connected between Pins 1 and 5, with its wiper connected to V+, can be used to trim out the inverting input current (with about ±20 μA of range). For closed-loop gains above about 5, this may not be sufficient to trim the output offset voltage to zero. Tie the pot's wiper to ground through a large value resistor (50 kΩ for ±5 V supplies, 150 kΩ for ±15 V supplies) to trim the output to zero at high closed-loop gains.

OPERATION AS A VIDEO LINE DRIVER

The ADEL2020 is designed to offer outstanding performance at closed-loop gains of 1 or greater. At a gain of 2, the ADEL2020 makes an excellent video line driver. The low differential gain and phase errors and wide –0.1 dB bandwidth are nearly independent of supply voltage and load. For applications requiring widest 0.1 dB bandwidth, it is recommended to use 715 Ω feedback and gain resistors. This will result in about 0.05 dB of peaking and a –0.1 dB bandwidth of 30 MHz on ±15 V supplies.

DISABLE MODE

By pulling the voltage on Pin 8 to common (0 V), the ADEL2020 can be put into a disabled state. In this condition, the supply current drops to less than 2.8 mA, the output becomes a high impedance, and there is a high level of isolation from input to output. In the case of a line driver, for example, the output impedance will be about the same as that for a 1.5 kΩ resistor (the feedback plus gain resistors) in parallel with a 13 pF capacitor (due to the output), and the input to output isolation will be better than 50 dB at 10 MHz.

Leaving the disable pin disconnected (floating) will leave the part in the enabled state.

In cases where the amplifier is driving a high impedance load, the input to output isolation will decrease significantly if the input signal is greater than about 1.2 V p–p. The isolation can be restored to the 50 dB level by adding a dummy load (say 150 Ω) at the amplifier output. This will attenuate the feedthrough signal. (This is not an issue for multiplexer applications where the outputs of multiple ADEL2020s are tied together as long as at least one channel is in the ON state.) The input impedance of the disable pin is about 35 kΩ in parallel with a few pF. When grounded, about 50 μA flows out of the disable pin for ±5 V supplies.

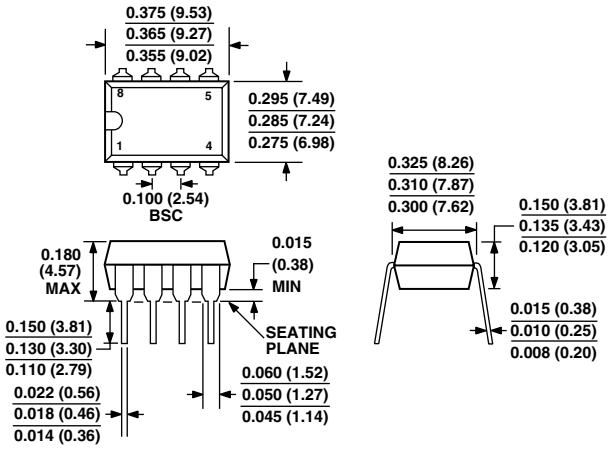
Break-before-make operation is guaranteed by design. If driven by standard CMOS logic, the disable time (until the output is high impedance) is about 100 ns and the enable time (to low impedance output) is about 160 ns. Since it has an internal pull-up resistor of about 35 kΩ, the ADEL2020 can be used with open drain logic as well. In that case, the enable time increases to about 1 μs.

If there is a nonzero voltage present on the amplifier's output at the time it is switched to the disabled state, some additional decay time will be required for the output voltage to relax to zero. The total time for the output to go to zero will normally be about 250 ns; it is somewhat dependent on the load impedance.

OUTLINE DIMENSIONS

8-Lead Plastic Dual-in-Line Package [PDIP]
(N-8)

Dimensions shown in inches and (millimeters)

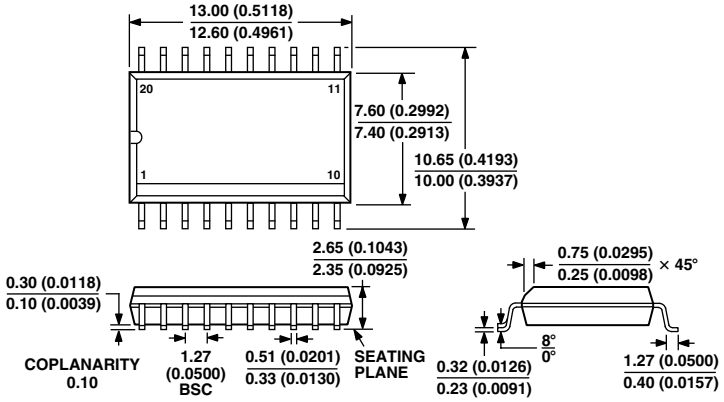


COMPLIANT TO JEDEC STANDARDS MO-095AA

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

20-Lead Standared Small Outline Pacakge [SOIC]
Wide Body
(R-20)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-013AC

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Revision History

Location	Page
1/03—Data Sheet changed from REV. 0 to REV. A.	
Format updated	Universal
8-Lead PDIP (N) and 20-Lead SOIC (R) updated	Universal
OUTLINE DIMENSIONS updated	9

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