



March 2015

MTD3055VL

# MTD3055VL

## N-Channel Logic Level Enhancement Mode Field Effect Transistor

### General Description

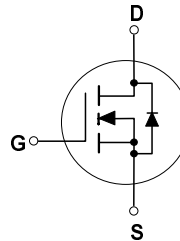
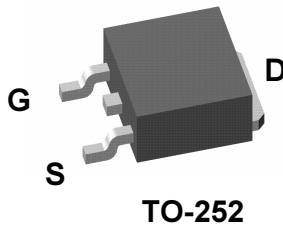
This N-Channel Logic Level MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

These MOSFETs feature faster switching and lower gate charge than other MOSFETs with comparable  $R_{DS(ON)}$  specifications.

The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC/DC power supply designs with higher overall efficiency.

### Features

- 12 A, 60 V.  $R_{DS(ON)} = 0.18 \Omega @ V_{GS} = 5 V$
- Critical DC electrical parameters specified at elevated temperature.
- Low drive requirements allowing operation directly from logic drivers.  $V_{GS(th)} < 2 V$ .
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.



### Absolute Maximum Ratings $T_c=25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	60	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Maximum Drain Current -Continuous (Note 1) $T_C = 100^\circ C$ (Note 1)	12 8	A
	Maximum Drain Current -Pulsed	42	
$P_D$	Maximum Power Dissipation @ $T_C = 25^\circ C$ (Note 1)	48	W
	$T_A = 25^\circ C$ (Note 1a)	3.9	
	$T_A = 25^\circ C$ (Note 1b)	1.5	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +175	$^\circ C$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to- Case (Note 1)	3.13	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to- Ambient (Note 1a)	71.4	$^\circ C/W$

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
MTD3055VL	MTD3055VL	13"	16mm	2500

\* Die and manufacturing source subject to change without prior notification.

## Electrical Characteristics

T<sub>C</sub> = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### DRAIN-SOURCE AVALANCHE RATINGS (Note 2)

W <sub>DSS</sub>	Single Pulse Drain-Source Avalanche Energy	V <sub>DD</sub> = 25 V, I <sub>D</sub> = 12 A			72	mJ
I <sub>AR</sub>	Maximum Drain-Source Avalanche Current				12	A

### Off Characteristics

BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C		54		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V			10	μA
		V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 150°C			100	
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 15 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -15 V, V <sub>DS</sub> = 0 V			-100	nA

### On Characteristics (Note 2)

V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1	1.5	2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C		-2.6		mV/°C
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 5 V, I <sub>D</sub> = 6 A,			0.18	Ω
V <sub>DS(on)</sub>	Drain-Source On-Voltage On-Resistance	V <sub>GS</sub> = 5 V, I <sub>D</sub> = 12 A			2.6	V
		I <sub>D</sub> = 6 A, T <sub>J</sub> = 150°C			2.5	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 8 V, I <sub>D</sub> = 6 A	5.0			S

### Dynamic Characteristics

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz			570	pF
C <sub>oss</sub>	Output Capacitance				160	pF
C <sub>rss</sub>	Reverse Transfer Capacitance				40	pF

### Switching Characteristics (Note 2)

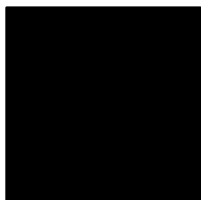
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 12 A, V <sub>GS</sub> = 5 V, R <sub>GEN</sub> = 9.1 Ω			20	ns
t <sub>r</sub>	Turn-On Rise Time				190	ns
t <sub>d(off)</sub>	Turn-Off Delay Time				30	ns
t <sub>f</sub>	Turn-Off Fall Time				90	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 48 V, I <sub>D</sub> = 12 A, V <sub>GS</sub> = 5 V			10	nC
Q <sub>gs</sub>	Gate-Source Charge			2		nC
Q <sub>gd</sub>	Gate-Drain Charge			6.1		nC

### Drain-Source Diode Characteristics and Maximum Ratings

I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current (Note 2)				12	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current (Note 2)				42	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 12 A (Note 2)			1.3	V
t <sub>rr</sub>	Drain-Source Reverse Recovery Time	I <sub>F</sub> = 12 A, di/dt = 100A/μs		51		nS

**Notes:**

- R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the drain tab. R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design.

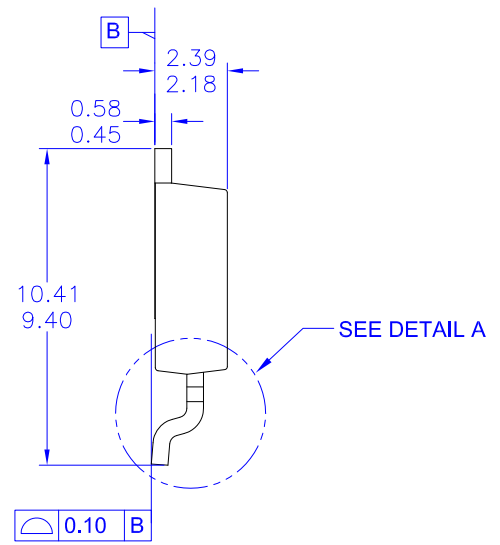
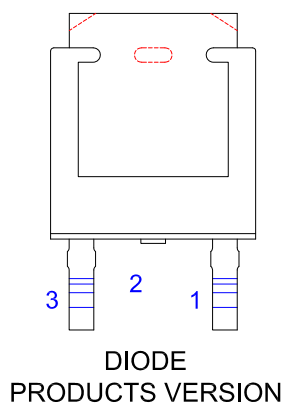
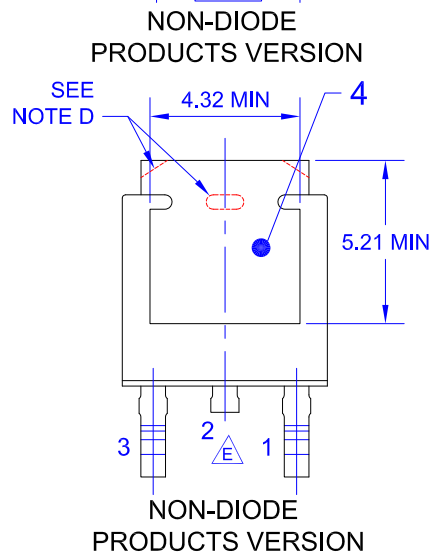
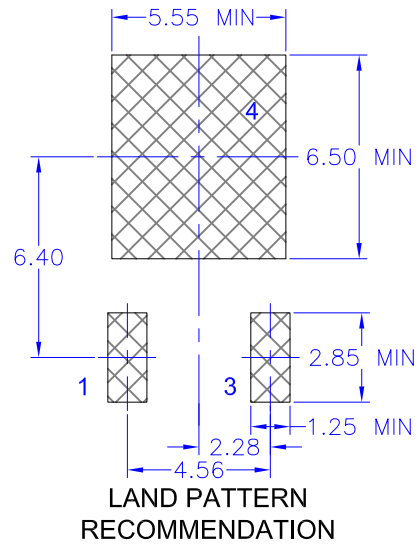
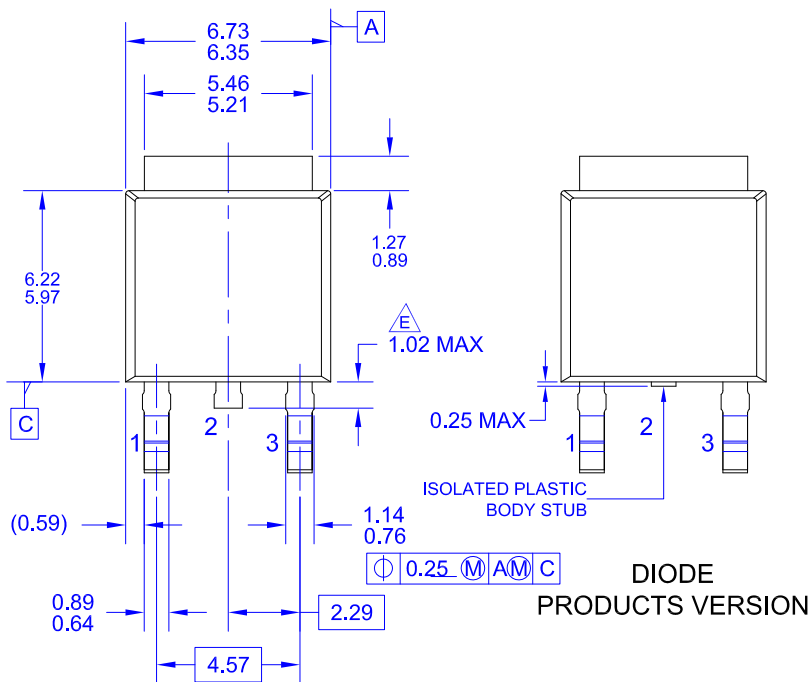


■ a) R<sub>θJA</sub> = 38°C/W when mounted on a 1 in<sup>2</sup> pad of 2oz copper.

■ b) R<sub>θJA</sub> = 96°C/W when mounted on a minimum pad.

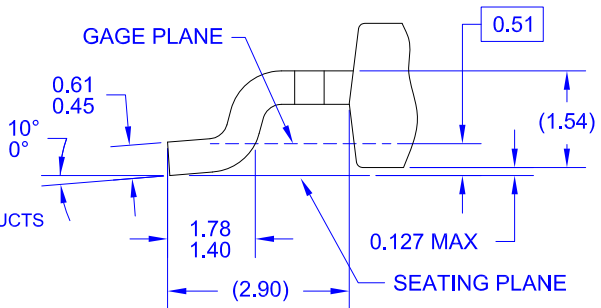
Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%



**NOTES: UNLESS OTHERWISE SPECIFIED**






- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
- F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
- H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11





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