MAX14738/MAX14739

High-Current Overvoltage Protectors with Adjustable OVLO

General Description

The MAX14738/MAX14739 overvoltage protection devices feature a low 76mΩ (typ) on-resistance (R_{ON}) internal FET and protect low-voltage systems against voltage faults up to +36V. When the input voltage exceeds the overvoltage threshold, the internal FET is turned off to prevent damage to the protected components.

The overvoltage-protection threshold can be adjusted with optional external resistors to any voltage between 4V and 20V. With the OVLO input set below the external OVLO select voltage, the devices automatically choose the accurate internal trip thresholds. The internal overvoltage thresholds (OVLO) are preset to 6.8V (typ) (MAX14738) or 10V (typ) (MAX14739). The devices are also protected against overcurrent events by an internal thermal shutdown.

The MAX14738/MAX14739 are offered in a small, 6-bump 1.3mm x 0.9mm wafer-level package (WLP) with an exposed pad and operate over the -40°C to +85°C extended temperature range.

Applications

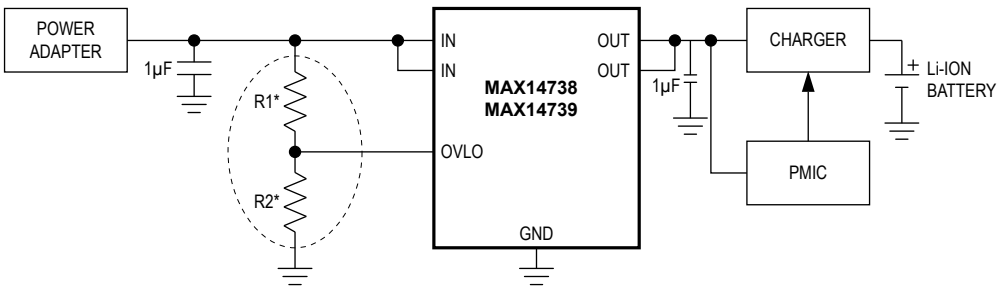
- Smartphones
- Tablet PCs
- Mobile Internet Devices

Benefits and Features

- Protects High-Power Portable Devices
  - Wide Operating Input-Voltage Protection from +2.2V to +36V
  - 3A Continuous-Current Capability
  - Integrated 76mΩ (typ) nMOSFET Switch
- Flexible Overvoltage Protection Design
  - Adjustable Overvoltage Protection Trip Level
  - Wide Adjustable OVLO Threshold Range from +4V to +20V
    - Preset Internal Accurate OVLO Thresholds: 6.8V±2.9% (MAX14738) 10V±3.0% (MAX14739)
- Additional Protection Features Increase System Reliability
  - Soft-Start to Minimize In-Rush Current
  - Internal 18ms Startup Debounce
  - Thermal-Shutdown Protection
- Minimize PCB Area
  - 6-Bump WLP (1.3mm x 0.9mm)

Ordering Information ***appears at end of data sheet.***

Typical Application Circuit



*R1 AND R2 ARE ONLY REQUIRED FOR ADJUSTABLE OVLO; OTHERWISE, CONNECT OVLO TO GND.

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Absolute Maximum Ratings

(All voltages referenced to GND.)
IN .....-0.3V to +40V
OUT.....-0.3V to (V_{IN} + 0.3V)
OVLO.....-0.3V to +6V
Continuous IN, OUT Current (Note 1).....3A
Peak IN, OUT Current (10ms).....5A

Continuous Power Dissipation (T_A = +70°C)
2 x 3 Array 6-Bump 1.3mm x 0.9mm WLP
(derate 10.5mW/°C).....840W
Operating Temperature Range.....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Soldering Temperature (reflow).....+260°C

Note 1: Continuous current limited by thermal design.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....95.2°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = +2.2V to +36V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN} = +5.0V and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}			2.5		36	V
Input Startup Voltage	V_{IN_ST}				1.65	2.5	V
Input Sustaining Voltage	V_{IN_SU}	I_{OUT} = 0A			1.23	2.2	V
Input Supply Current	I_{IN}	V_{IN} = 5V			110	200	µA
IN Overvoltage Trip Level	V_{IN_OVLO}	V_{IN} rising	MAX14738	6.60	6.80	7.00	V
			MAX14739	9.7	10	10.3	
		V_{IN} falling	MAX14738	6.5			
			MAX14739	9.6			
IN Overvoltage Lockout Hysteresis	$V_{IN\_OVLO\_HYS}$				0.3		%
OVLO Set Threshold	V_{OVLO_THRESH}			1.18	1.22	1.26	V
Adjustable OVLO Threshold Range				4		20	V
External OVLO Select Threshold	V_{OVLO_SELECT}			0.25		0.35	V
Switch On-Resistance	R_{ON}	I_{OUT} = 100mA, T_A = +25°C, V_{IN} = 5V			76	102	mΩ
OVLO Clamp		I_{CLAMP} = 10µA, V_{IN} = 5V			3.9		V
OUT Capacitor	C_{OUT}					1000	µF
Clamp Leakage at Minimum Voltage		V_{OVLO} = 1.8V			0.5		nA

Electrical Characteristics (continued)

(V_{IN} = +2.2V to +36V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN} = +5.0V and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Clamping Current		V_{OVLO} = 5.5V		200		µA
OVLO Input Leakage Current	I_{OVLO}	V_{OVLO_THRESH} = 1.22	-100		+100	nA
Thermal Shutdown				+150		°C
Thermal-Shutdown Hysteresis				20		°C
TIMING CHARACTERISTICS (Figure 1)						
Debounce Time	t_{INDBC}	Time from 2.5V < V_{IN} < V_{IN_OVLO} to V_{OUT} = 10% of V_{IN}		18		ms
Soft-Start Time	t_{SS}	Soft-start time beginning from V_{OUT} = 10% of V_{IN} to soft-start off		17		ms
Switch Turn-On Time	t_{ON}	V_{IN} = 5V, R_{LOAD} = 100Ω, C_{LOAD} = 100µF; V_{OUT} from 10% to 90% of V_{IN}		2		ms
		V_{IN} = 5V, R_{LOAD} = 100Ω, C_{LOAD} = 1mF; V_{OUT} from 10% to 90% of V_{IN}		6		
Switch Turn-Off Response Time	t_{OFF}	V_{IN} > V_{OVLO}, 2V/µs to V_{OUT} stops rising, R_{LOAD} = 100Ω		0.5		µs

Note 3: All specifications are 100% production tested at T_A = +25°C, unless otherwise noted. Specifications are over -40°C to +85°C and are guaranteed by design.

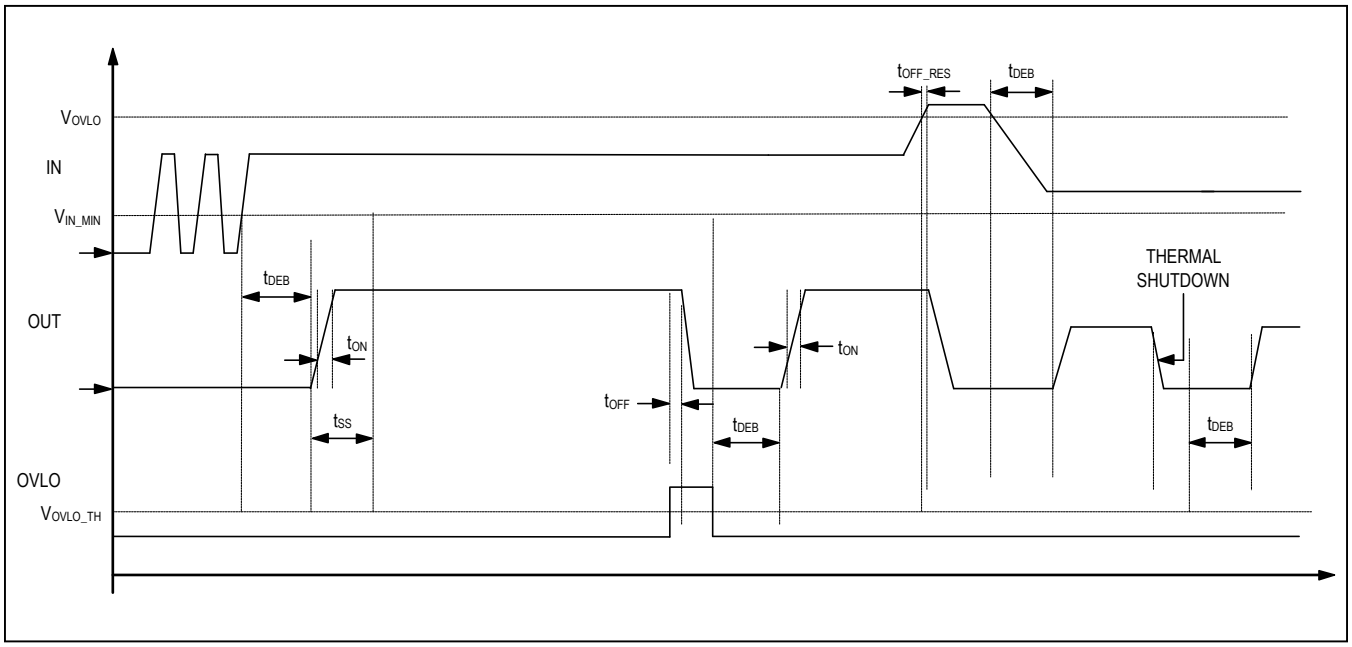
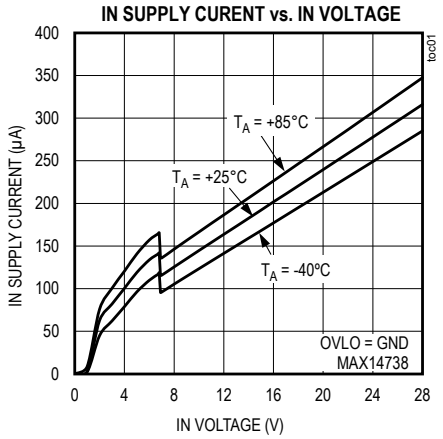
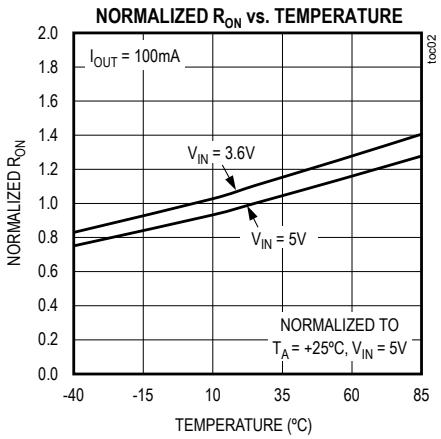


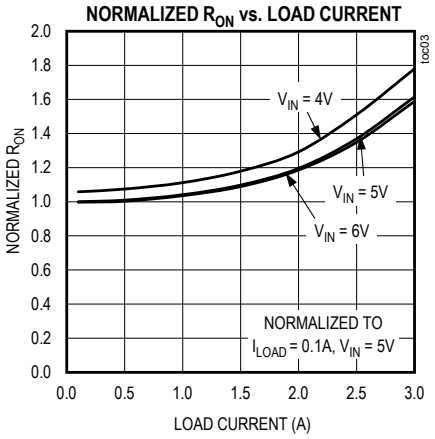
Figure 1. Timing Diagram

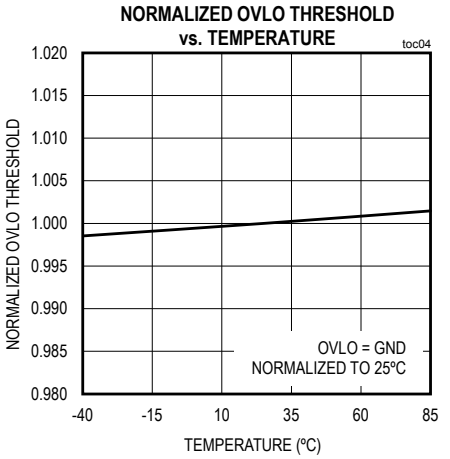
Typical Operating Characteristics

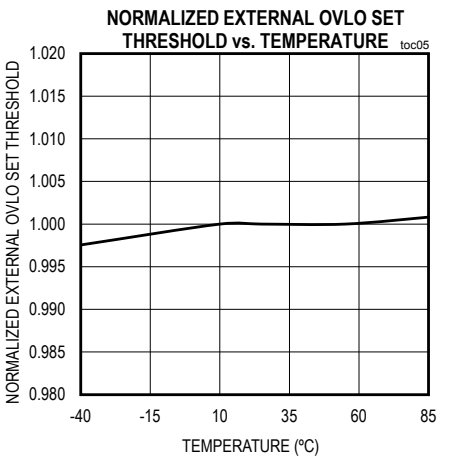
(V_{IN} = +5.0V, C_{IN} = 1µF, C_{OUT} = 1µF, T_A = +25°C, unless otherwise noted.)

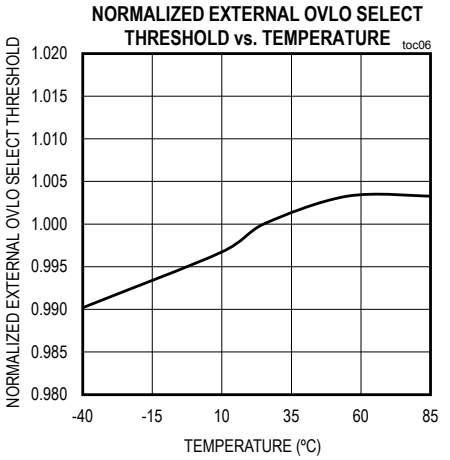








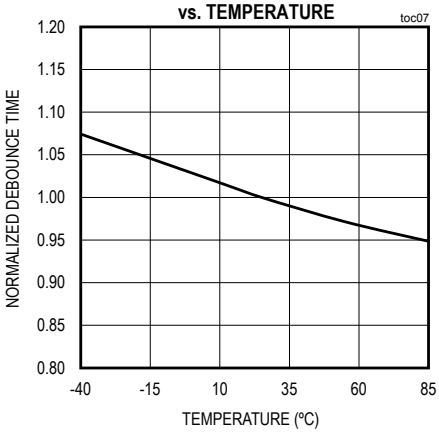




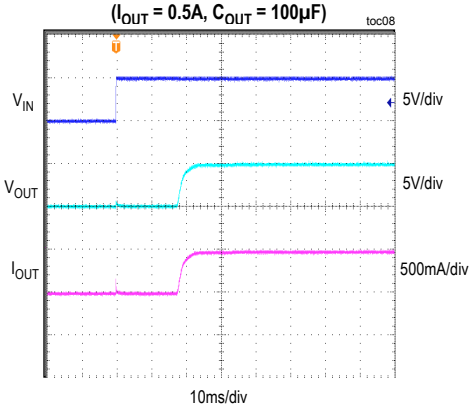
Typical Operating Characteristics (continued)

(V_{IN} = +5.0V, C_{IN} = 1µF, C_{OUT} = 1µF, T_A = +25°C, unless otherwise noted.)

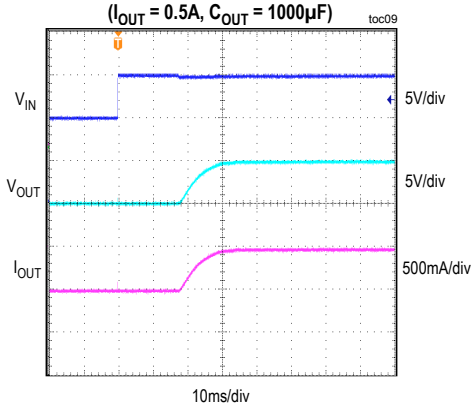
NORMALIZED DEBOUNCE TIME vs. TEMPERATURE



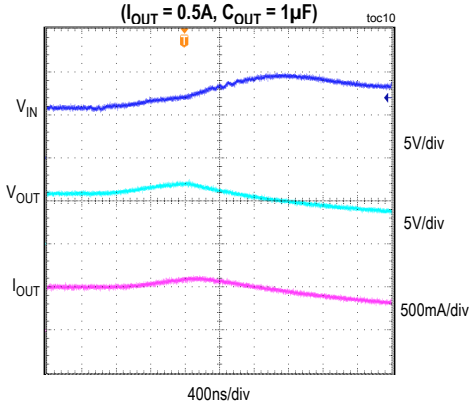
POWER-UP RESPONSE (I_{OUT} = 0.5A, C_{OUT} = 100µF)



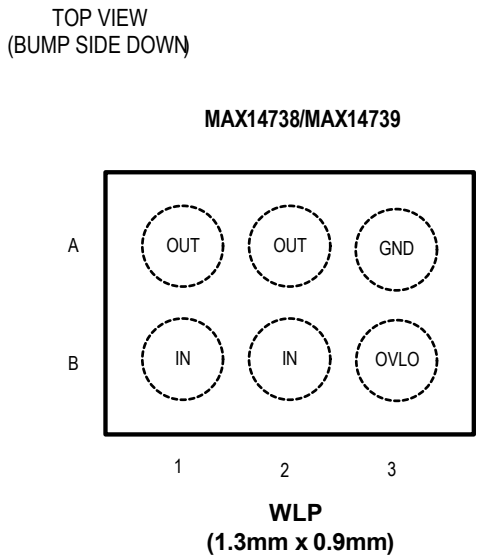
POWER-UP RESPONSE (I_{OUT} = 0.5A, C_{OUT} = 1000µF)



OVERVOLTAGE FAULT RESPONSE (I_{OUT} = 0.5A, C_{OUT} = 1µF)



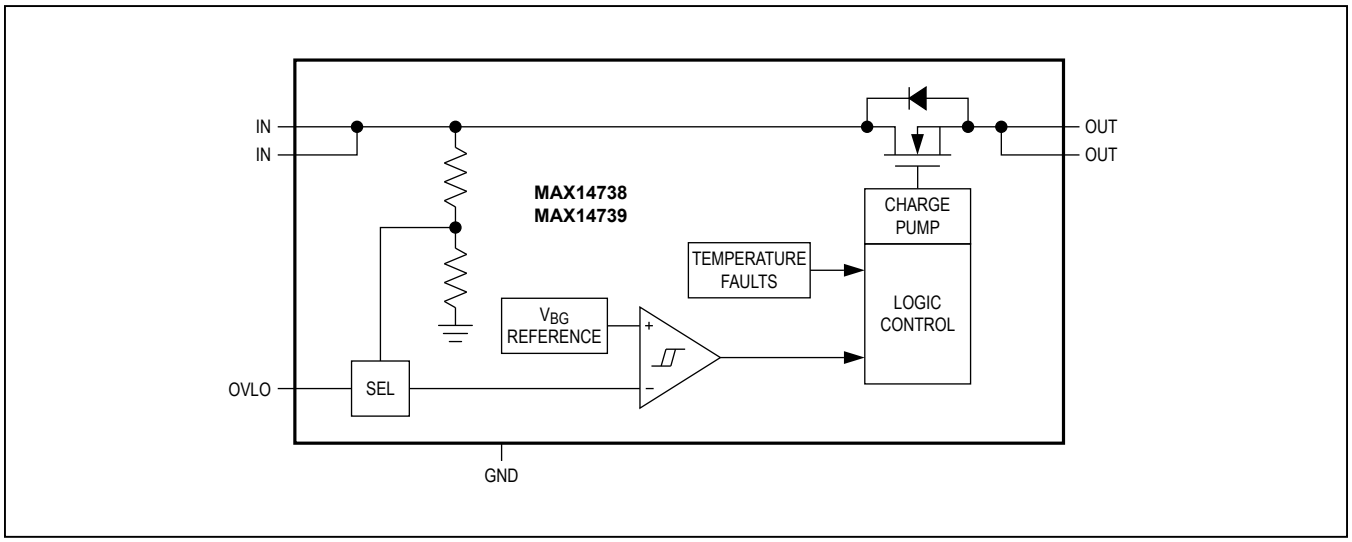
Bump Configuration



Bump Description

BUMP	NAME	FUNCTION
A1, A2	OUT	Output Voltage. Output of internal switch. Bypass OUT with a 1µF (at least) ceramic capacitor as close as possible to the device. Connect both OUT pins together for proper operation.
A3	GND	Ground
B1, B2	IN	Voltage Input. Bypass IN with a 1µF ceramic capacitor as close as possible to the device to obtain ±15kV Human Body Model (HBM) ESD protection. Connect both IN pins together for proper operation. IN is protected to ±2kV HBM when IN is not bypassed with a capacitor to GND.
B3	OVLO	External OVLO Adjustment. Connect OVLO to GND when using the internal threshold. Connect a resistor-divider to OVLO to set a different OVLO threshold; this external resistor-divider is completely independent from the internal threshold.

Functional Diagram



Detailed Description

The MAX14738/MAX14739 overvoltage-protection devices feature a low on-resistance (R_{ON}) internal FET and protect low-voltage systems against voltage faults up to +36V. If the input voltage exceeds the overvoltage threshold, the internal FET is turned off to prevent damage to the protected components. The 18ms debounce time prevents false turn-on of the internal FET during startup.

Device Operation

The devices have timing logic that controls the turn-on of the internal FET. If $V_{IN} < V_{OVLO\_THRESH}$, the internal charge pump is enabled. The charge-pump startup turns on the internal FET after a 18ms debounce delay (see the *Functional Diagram*). After the debounce time, softstart limits the FET inrush current for 17ms (typ). At any time, if V_{IN} rises above V_{OVLO_THRESH}, OUT is disconnected from IN.

Internal Switch

The devices incorporate an internal FET with a 76mΩ (typ) R_{ON}. The FET is internally driven by a charge pump that generates a necessary gate voltage above IN. The internal FET can pass more than 5A inrush current.

Overvoltage Lockout (OVLO)

The MAX14738 has a 6.8V (typ) overvoltage threshold. The MAX14739 has a 10V (typ) overvoltage threshold.

Thermal Shutdown Protection

The devices feature thermal-shutdown circuitry. The internal FET turns off when the junction temperature exceeds +150°C (typ). The device exits thermal shutdown after the junction temperature cools by 20°C (typ).

Applications Information

IN Bypass Capacitor

For most applications, bypass IN to GND with a 1µF ceramic capacitor as close as possible to the device to enable ±15kV (HBM) ESD protection on IN. If ±15kV (HBM) ESD is not required, there is no capacitor required at IN. If the power source has significant inductance due to long lead length, take care to prevent overshoots due to the LC tank circuit and provide protection if necessary to prevent exceeding the +40V absolute maximum rating on IN.

OUT Output Capacitor

The slow turn-on time provides a soft-start function that allows the devices to charge an output capacitor up to 1000µF without turning off due to an overcurrent condition.

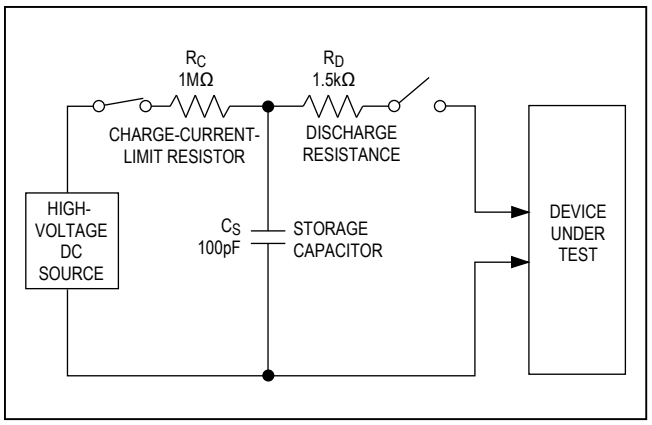


Figure 2a. Human Body ESD Test Model

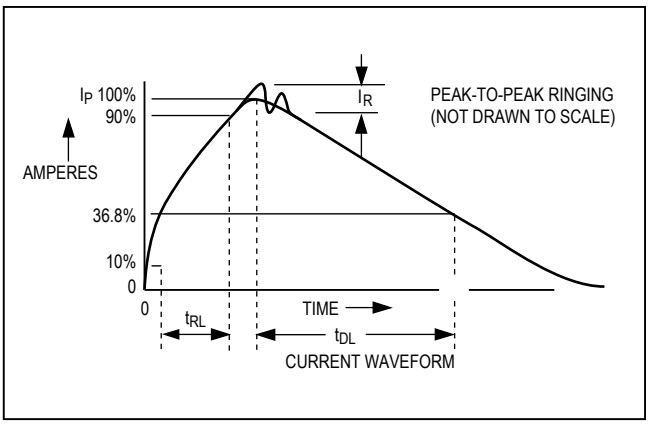


Figure 2b. Human Body Current Waveform

External OVLO Adjustment Functionality

If OVLO is connected to ground, the internal OVLO comparator uses the internally set OVLO value.

If an external resistor-divider is connected to OVLO and V_{OVLO} exceeds the OVLO select voltage (V_{OVLO_SELECT}), the internal OVLO comparator reads the IN fraction fixed by the external resistor-divider.

R1 = 1MΩ is a good starting value for minimum current consumption. Since V_{IN_OVLO}, V_{OVLO_THRESH}, and R1 are known, R2 can be calculated from the following formula:

$$V_{IN\_OVLO} = V_{OVLO\_THRESH} \times \left[1 + \frac{R1}{R2}\right]$$

This external resistor-divider is completely independent from the internal resistor-divider.

ESD Test Conditions

ESD performance depends on a number of conditions.

The devices are specified for ±15kV (HBM) typical ESD resistance on IN when IN is bypassed to ground with a 1µF ceramic capacitor.

Human Body Model ESD Protection

Figure 2a shows the HBM and Figure 2b shows the current waveform it generates when discharged into a low-impedance state. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

Ordering Information/Selector Guide

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK	OVLO (V)
MAX14738EWT+	-40°C to +85°C	6 WLP	DF	6.8
MAX14739EWT+	-40°C to +85°C	6 WLP	DG	10

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
6 WLP	W60B1+1	**21-100021**	Refer to **Application Note 1891**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/15	Initial release	—

