Low Voltage, Micropower, Quad Operational Amplifier

OP490

FEATURES

Single/dual-supply operation
- **1.6 V to 36 V**
- **±0.8 V to ±18 V**

Single-supply operation; input and output voltage ranges include ground
Low supply current: 80 µA maximum
High output drive: 5 mA minimum
Low offset voltage: 1.0 mV maximum
High open-loop gain: 800 V/mV typical
Industry-standard quad pinouts

FUNCTIONAL BLOCK DIAGRAMS

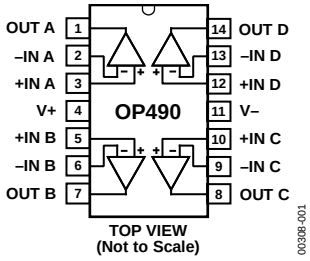

Figure 1. 14-Lead Plastic DIP (P-Suffix)

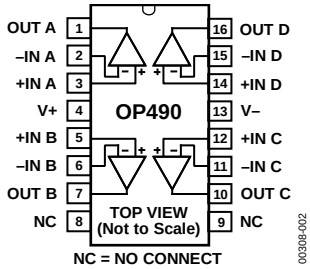

Figure 2. 16-Lead SOIC (S-Suffix)

GENERAL DESCRIPTION

The OP490 is a high performance micropower quad op amp that operates from a single supply of 1.6 V to 36 V or from dual supplies of ±0.8 V to ±18 V. The input voltage range includes the negative rail allowing the OP490 to accommodate input signals down to ground in single-supply operation. The output swing of the OP490 also includes ground when operating from a single supply, enabling zero-in, zero-out operation.

The quad OP490 draws less than 20 µA of quiescent supply current per amplifier, but each amplifier is able to deliver over 5 mA of output current to a load. Input offset voltage is under 0.5 mV. Gain exceeds over 400,000 and CMR is better than 90 dB. A PSRR of under 5.6 µV/V minimizes offset voltage changes experienced in battery-powered systems.

The quad OP490 combines high performance with the space and cost savings of quad amplifiers. The minimal voltage and current requirements of the OP490 make it ideal for battery and solar-powered applications, such as portable instruments and remote sensors.

Rev. E
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Documentation

Application Notes

- AN-649: Using the Analog Devices Active Filter Design Tool

Data Sheet

- OP490: Low Voltage Micropower Quad Operational Amplifier Data Sheet
- OP490: Military Data Sheet

Tools and Simulations

- OP490 SPICE Macro-Model

Design Resources

- OP490 Material Declaration
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REVISION HISTORY

5/10—Rev. D to Rev. E

Changes to Features Section ... 1
Changes to Figure 24 ... 12

7/09—Rev. C to Rev. D

Deleted 14-Lead CERDIP (Y-Suffix) ... Universal
Deleted Figure 1, Renumbered Figures Sequentially ... 1
Changes to Table 1 ... 3
Changes to Table 2 ... 4
Changes to Figure 16 ... 8
Updated Outline Dimensions ... 14
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4/02—Rev. B to Rev. C

Deleted 28-Pin LCC (TC-Suffix) Pin Connection Diagram ... 1
Deleted Electrical Characteristics ... 3
Edits to Absolute Maximum Ratings ... 6
Edits to Ordering Guide ... 16

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

@ V_S = ±1.5 V to ±15 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Input Offset Voltage	V_{OS}			0.6	1.0	mV
Input Offset Current	I_{OS}	V_{CM} = 0 V		0.4	5	nA
Input Bias Current	I_B	V_{CM} = 0 V		4.2	25	nA
Large Signal Voltage Gain	A_{VO}	V_S = ±15 V, V_O = ±10 V				
		R_L = 100 kΩ	400	800		V/mV
		R_L = 10 kΩ	200	400		V/mV
		R_L = 2 kΩ	100	200		V/mV
		V+ = 5 V, V− = 0 V, 1 V < V_O < 4 V				
		R_L = 100 kΩ	100	250		V/mV
		R_L = 10 kΩ	70	140		V/mV
Input Voltage Range[1]	IVR	V+ = 5 V, V− = 0 V	0		4	V
Common-Mode Rejection Ratio	CMRR	V+ = 5 V, V− = 0 V, 0 V < V_{CM} < 4 V	80	100		dB
		V_S = ±15 V, −15 V < V_{CM} < +13.5 V	90	120		dB
Input Resistance Differential Mode	R_{IN}	V_S = ±15 V		30		MΩ
Input Resistance Common-Mode	R_{INCM}	V_S = ±15 V		20		GΩ
OUTPUT CHARACTERISTICS						
Output Voltage Swing	$V_{O\ L}$	V_S = ±15 V, R_L = 10 kΩ	±13.5	±14.2		V
		V_S = ±15 V, R_L = 2 kΩ	±10.5	±11.5		V
Output Voltage High	V_{OH}	V+ = 5 V, V− = 0 V, R_L = 2 kΩ	4.0	4.2		V
Output Voltage Low	V_{OL}	V+ = 5 V, V− = 0 V, R_L = 10 kΩ		100	500	µV
Capacitive Load Stability		A_V = 1		650		pF
DYNAMIC PERFORMANCE						
Slew Rate	SR	V_S = ±15 V	5	12		V/ms
Channel Separation[2]	CS	f_O = 10 Hz, V_O = 20 V p-p, V_S = ±15 V	120	150		dB
Gain Bandwidth Product	GBWP	A_V = 1		20		kHz
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR			3.2	10	µV/V
Supply Current (All Amplifiers)	I_{SY}	V_S = ±1.5 V, no load		40	60	µA
		V_S = ±15 V, no load		60	80	µA
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	f_O = 0.1 Hz to 10 Hz, V_S = ±15 V		3		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		60		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.07		pA/√Hz

[1] Guaranteed by CMRR test.
[2] Guaranteed but not 100% tested.

@ V_S = ±1.5 V to ±15 V, −40°C ≤ T_A ≤ +85°C

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Input Offset Voltage	V_{OS}			0.8	1.5	mV
Average Input Offset Voltage Drift	TCV_{OS}	V_S = ±15 V		4		μV/°C
Input Offset Current	I_{OS}	V_{CM} = 0 V		1.3	7	nA
Input Bias Current	I_B	V_{CM} = 0 V		4.4	25	nA
Large Signal Voltage Gain	A_{VO}	V_S = ±15 V, V_O = ±10 V				
		R_L = 100 kΩ	300	600		V/mV
		R_L = 10 kΩ	150	250		V/mV
		R_L = 2 kΩ	75	125		V/mV
		V+ = 5 V, V− = 0 V, 1 V < V_O < 4 V				
		R_L = 100 kΩ	80	160		V/mV
		R_L = 10 kΩ	40	90		V/mV
Input Voltage Range[1]	IVR	V+ = 5 V, V− = 0 V	0.3		5	V
			−15		+13.5	V
Common-Mode Rejection Ratio	CMRR	V+ = 5 V, V− = 0 V, 0 V < V_{CM} < 3.5 V	80	100		dB
		V_S = ±15 V, −15 V < V_{CM} < +13.5 V	90	110		dB
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	V_S = ±15 V	±13	±14		V
		R_L = 2 kΩ	±10	±11		V
Output Voltage High	V_{OH}	V+ = 5 V, V− = 0 V, R_L = 2 kΩ	3.9	4.1		V
Output Voltage Low	V_{OL}	V+ = 5 V, V− = 0 V, R_L = 10 kΩ		100	500	μV
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR			5.6	17.8	μV/V
Supply Current (All Amplifiers)	I_{SY}	V_S = ±1.5 V, no load		60	100	mA
		V_S = ±15 V, no load		75	120	mA

[1] Guaranteed by CMRR test.

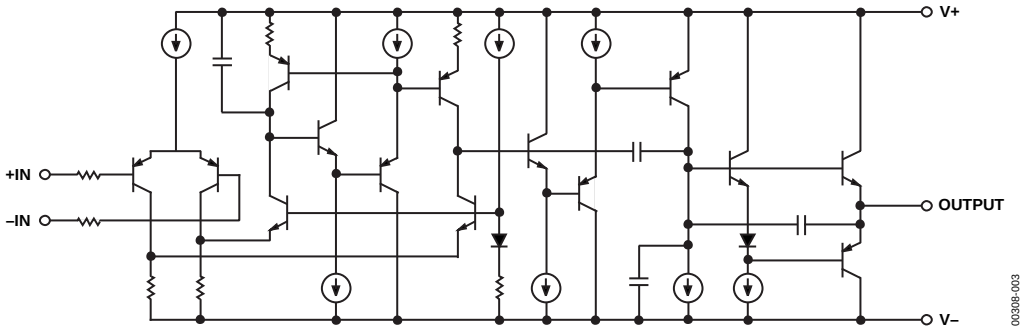


Figure 3. Simplified Schematic

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	±18 V
Digital Input Voltage	[(V–) – 20 V] to [(V+) + 20 V]
Common-Mode Input Voltage	[(V–) – 20 V] to [(V+) + 20 V]
Output Short-Circuit Duration	Continuous
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	–40°C to +85°C
Junction Temperature (T_J) Range	–65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for worst-case mounting conditions, that is, θ_{JA} is specified for a device in socket for the PDIP package; θ_{JA} is specified for a device soldered to a printed circuit board (PCB) for the SOIC package.

Table 4.

Package Type	θ_{JA}	θ_{JC}	Unit
14-Lead PDIP_N (S-Suffix)	76	33	°C/W
16-Lead SOIC_R (S-Suffix)	92	27	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

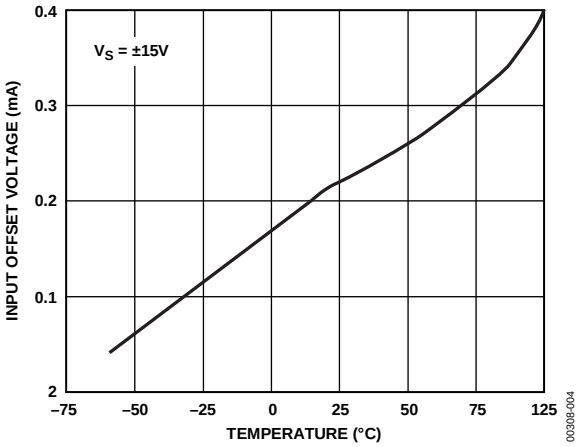


Figure 4. Input Offset Voltage vs. Temperature

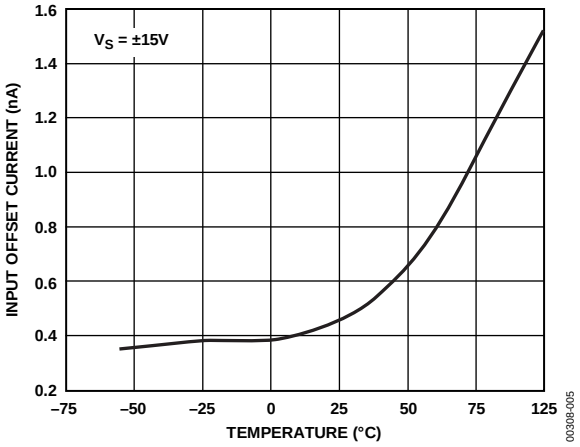


Figure 5. Input Offset Current vs. Temperature

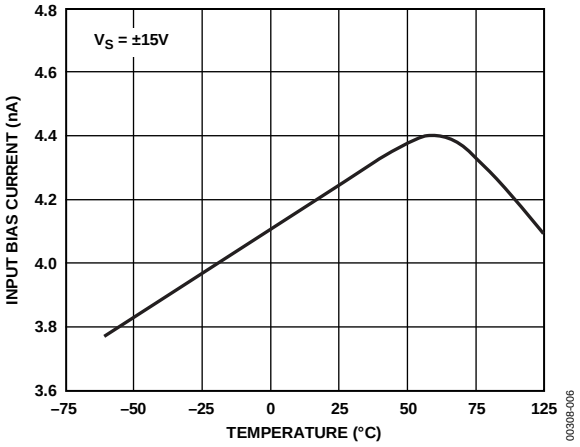


Figure 6. Input Bias Current vs. Temperature

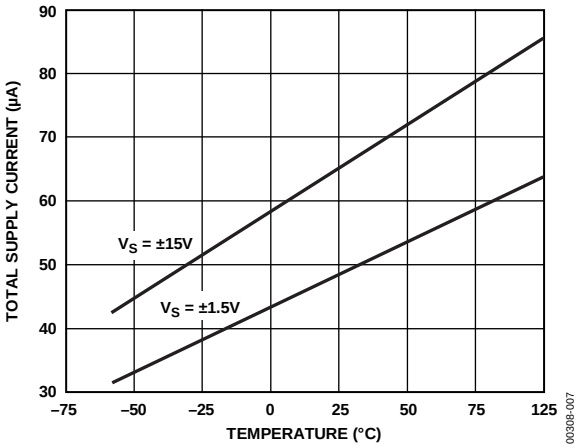


Figure 7. Total Supply Current vs. Temperature

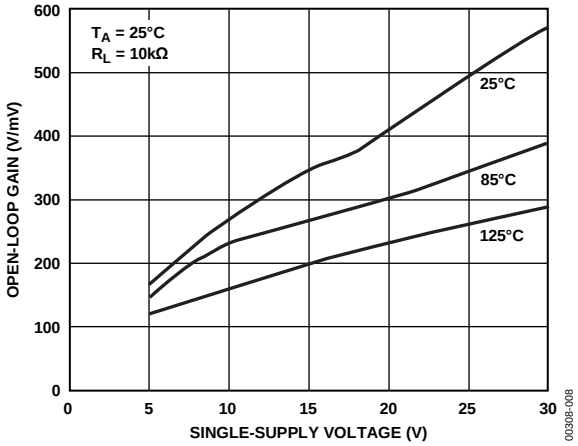


Figure 8. Open-Loop Gain vs. Single-Supply Voltage

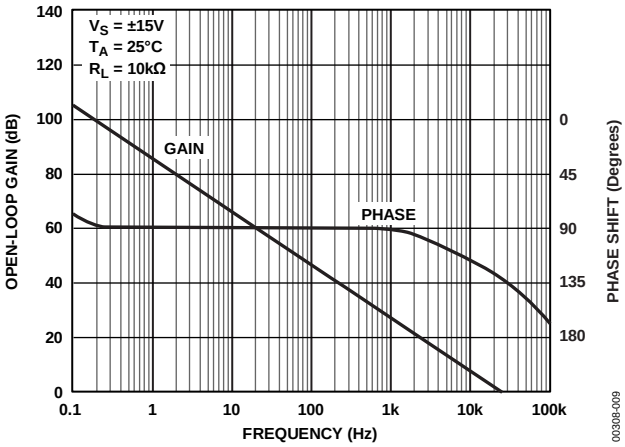


Figure 9. Open-Loop Gain and Phase Shift vs. Frequency

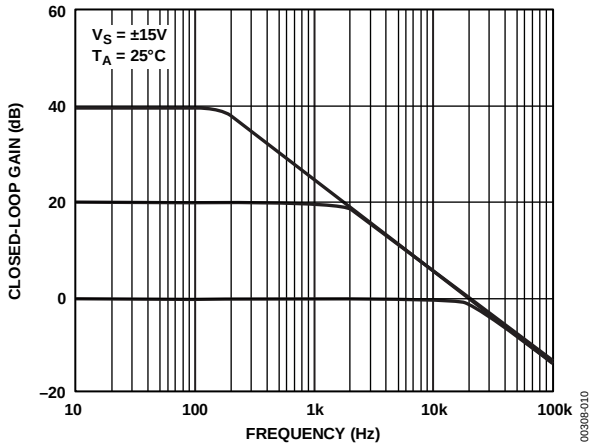


Figure 10. Closed-Loop Gain vs. Frequency

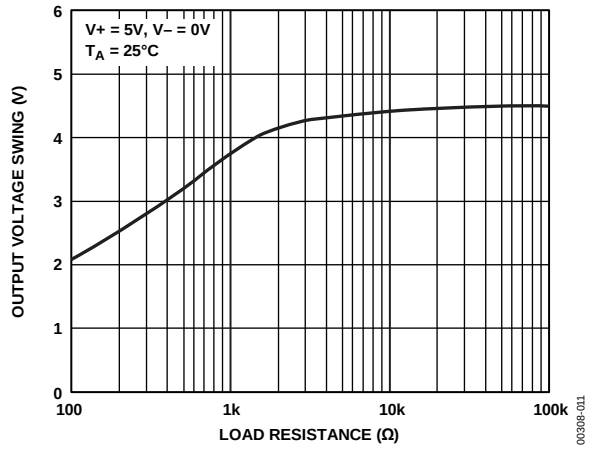


Figure 11. Output Voltage Swing vs. Load Resistance

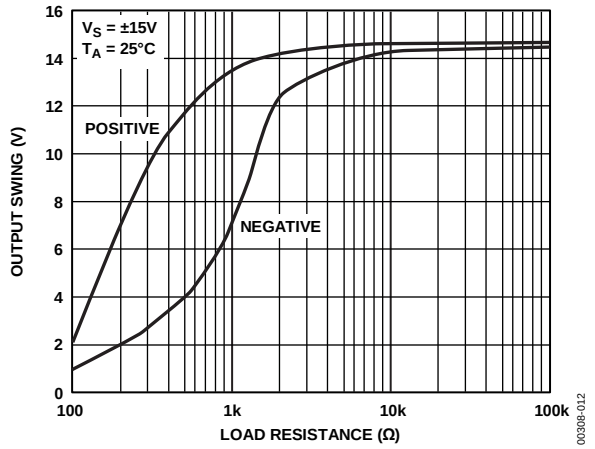


Figure 12. Output Voltage Swing vs. Load Resistance

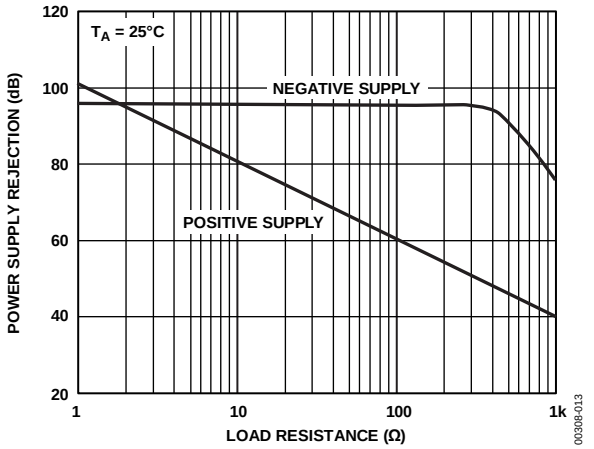


Figure 13. Power Supply Rejection vs. Frequency

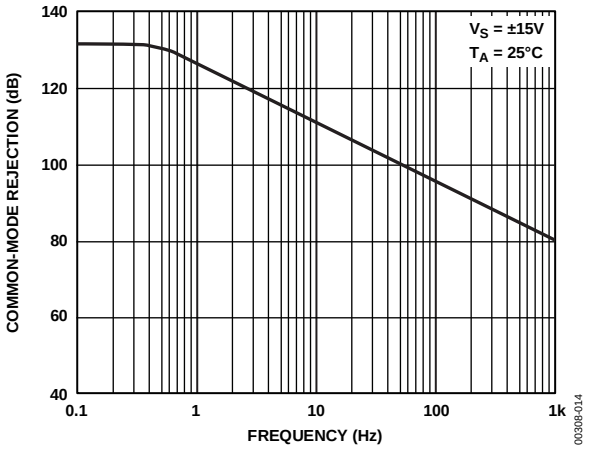


Figure 14. Common-Mode Rejection vs. Frequency

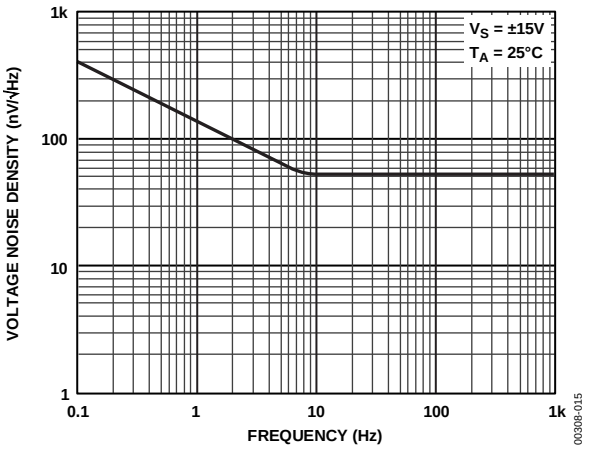


Figure 15. Voltage Noise Density vs. Frequency

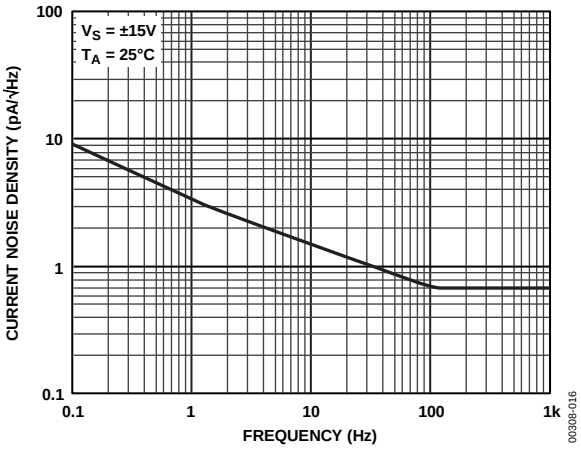


Figure 16. Current Noise Density vs. Frequency

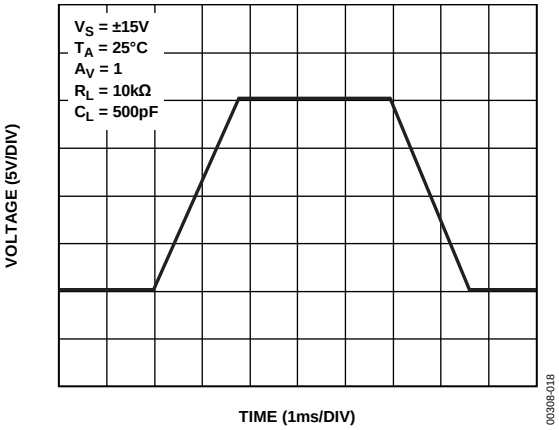


Figure 18. Large Signal Transient Response

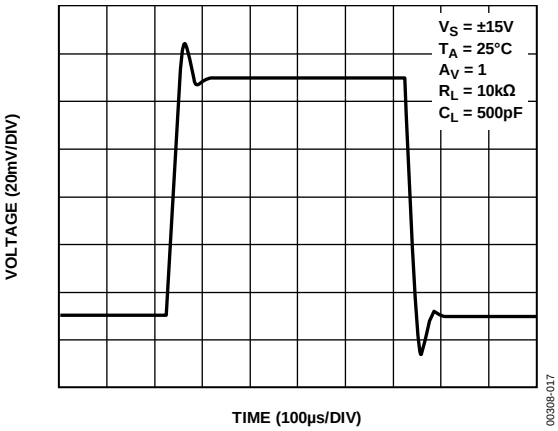


Figure 17. Small Signal Transient Response

APPLICATIONS INFORMATION

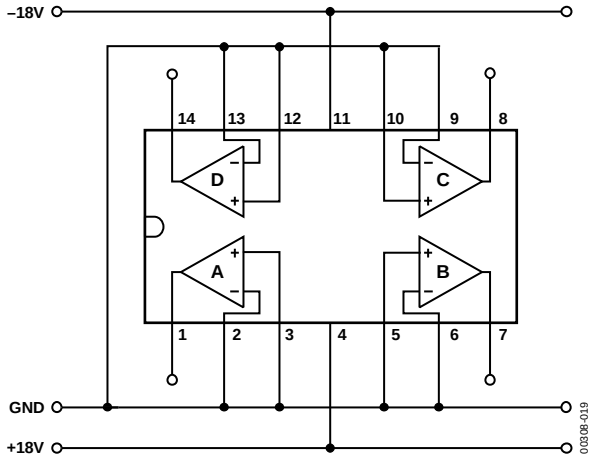


Figure 19. Burn-In Circuit

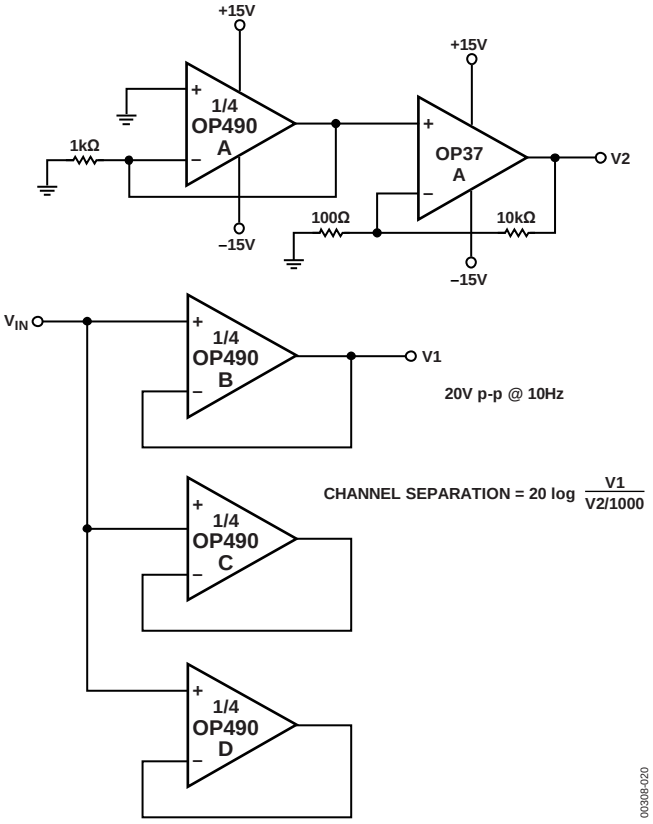


Figure 20. Channel Separation Test Circuit

BATTERY-POWERED APPLICATIONS

The OP490 can be operated on a minimum supply voltage of 1.6 V or with dual supplies of ±0.8 V drawing only 60 µA of supply current. In many battery-powered circuits, the OP490 can be continuously operated for hundreds of hours before requiring battery replacement, thereby reducing equipment downtime and operating costs.

High performance portable equipment and instruments frequently use lithium cells because of their long shelf life, light weight, and high energy density relative to older primary cells. Most lithium cells have a nominal output voltage of 3 V and are noted for a flat discharge characteristic. The low supply current requirement of the OP490, combined with the flat discharge characteristic of the lithium cell, indicates that the OP490 can be operated over the entire useful life of the cell. Figure 21 shows the typical discharge characteristic of a 1 Ah lithium cell powering an OP490 with each amplifier, in turn, driving full output swing into a 100 kΩ load.

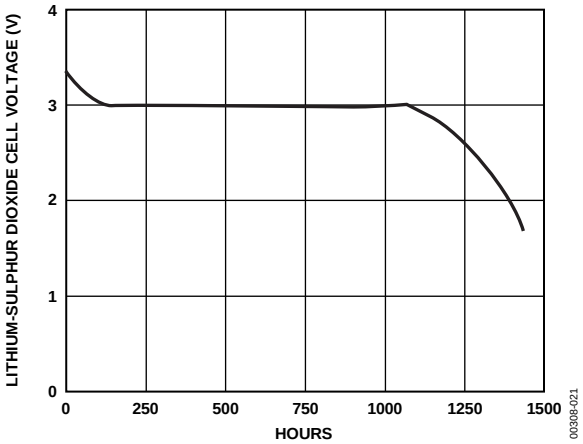


Figure 21. Lithium-Sulphur Dioxide Cell Discharge Characteristic with OP490 and 100 kΩ Loads

SINGLE-SUPPLY OUTPUT VOLTAGE RANGE

In single-supply operation the input and output ranges of the OP490 include ground. This allows true zero-in, zero-out operation. The output stage provides an active pull-down to around 0.8 V above ground. Below this level, a load resistance of up to 1 MΩ to ground is required to pull the output down to zero.

In the region from ground to 0.8 V, the OP490 has voltage gain equal to the data sheet specification. Output current source capability is maintained over the entire voltage range including ground.

INPUT VOLTAGE PROTECTION

The OP490 uses a PNP input stage with protection resistors in series with the inverting and noninverting inputs. The high breakdown of the PNP transistors coupled with the protection resistors provides a large amount of input protection, allowing the inputs to be taken 20 V beyond either supply without damaging the amplifier.

MICROPOWER VOLTAGE-CONTROLLED OSCILLATOR

An OP490 in combination with an inexpensive quad CMOS switch comprise the precision V_{CO} of Figure 22. This circuit provides triangle and square wave outputs and draws only 75 µA from a 5 V supply. A acts as an integrator; S1 switches the charging current symmetrically to yield positive and negative ramps. The integrator is bounded by B, which acts as a Schmitt trigger with a precise hysteresis of 1.67 V, set by Resistors R5, R6, and R7, and the associated CMOS switches. The resulting output of A is a triangle wave with upper and lower levels of 3.33 V and 1.67 V. The output of B is a square wave with almost rail-to-rail swing. With the components shown, frequency of operation is given by the equation

$$f_{OUT} = V_{CONTROL} \text{ (Volts)} \times 10 \text{ Hz/V}$$

but this is easily changed by varying C1. The circuit operates well up to a few hundred hertz.

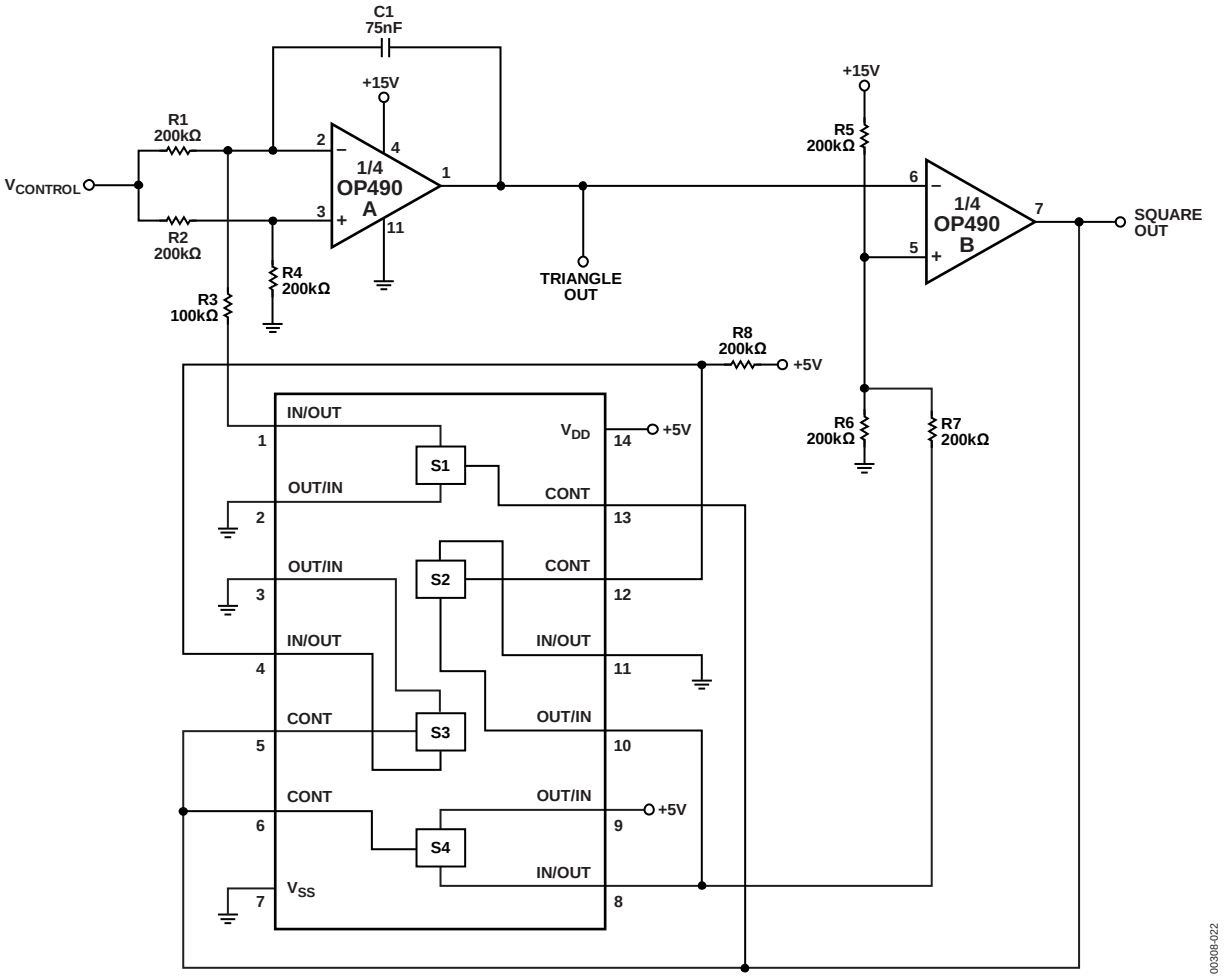


Figure 22. Micropower Voltage Controlled Oscillator

MICROPOWER SINGLE-SUPPLY QUAD VOLTAGE-OUTPUT 8-BIT DAC

The circuit shown in Figure 23 uses the DAC8408 CMOS quad 8-bit DAC, and the OP490 to form a single-supply quad voltage output DAC with a supply drain of only 140 µA. The DAC8408 is used in voltage switching mode and each DAC has an output resistance (≈10 kΩ) independent of the digital input code. The output amplifiers act as buffers to avoid loading the DACs. The 100 kΩ resistors ensure that the OP490 outputs swing below 0.8 V when required.

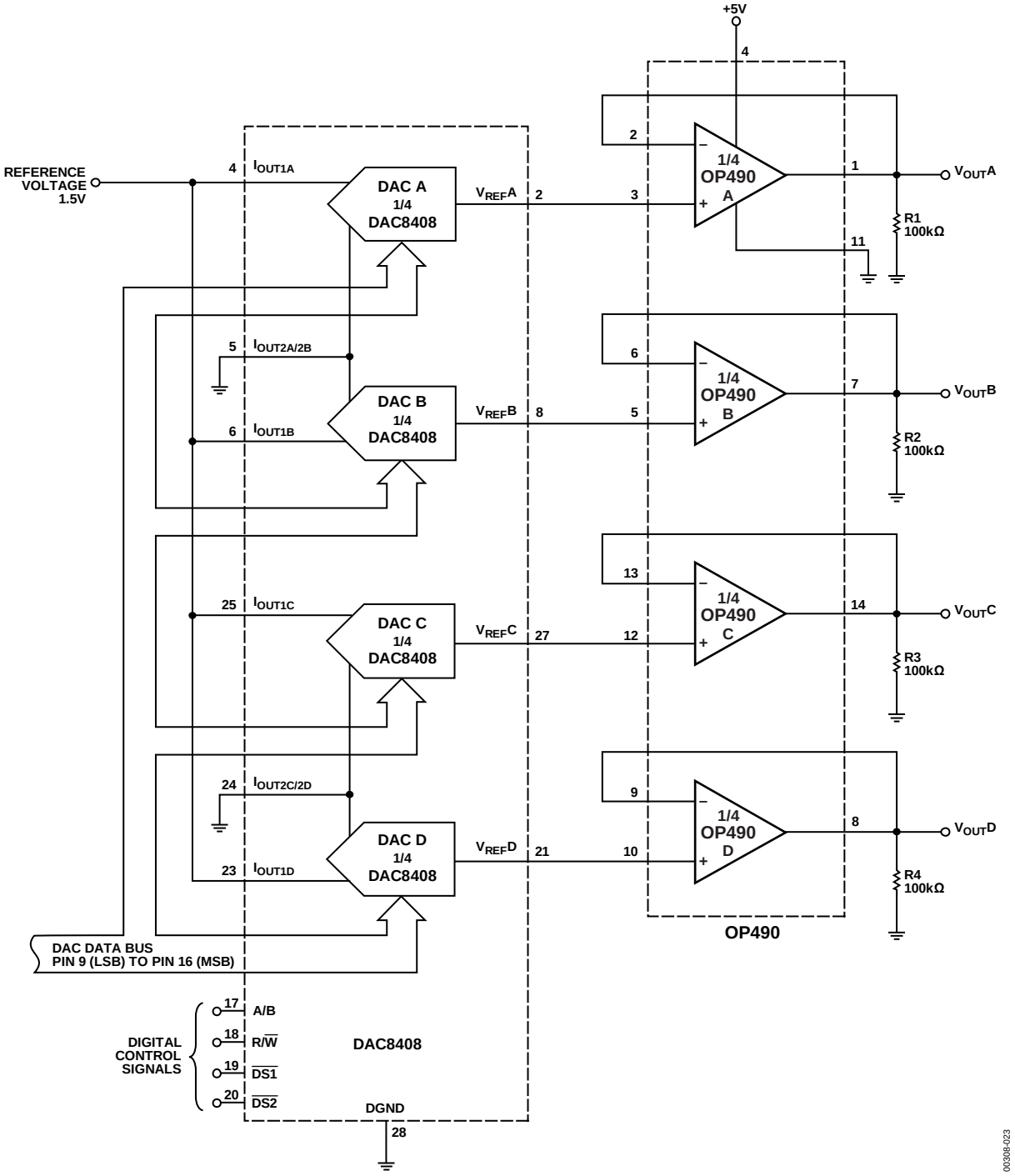


Figure 23. Micropower Single-Supply Quad Voltage Output 8-Bit DAC

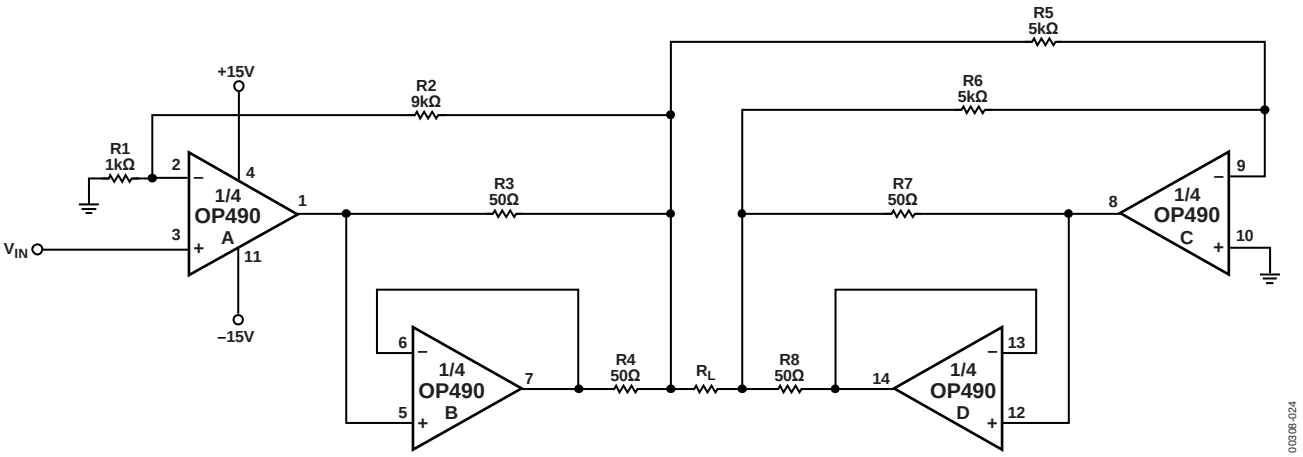


Figure 24. High Output Amplifier

HIGH OUTPUT AMPLIFIER

The amplifier shown in Figure 24 is capable of driving 25 V p-p into a 1 kΩ load. Design of the amplifier is based on a bridge configuration. A amplifies the input signal and drives the load with the help of B. Amplifier C is a unity-gain inverter which drives the load with help from D. Gain of the high output amplifier with the component values shown is 10, but can easily be changed by varying R1 or R2.

SINGLE-SUPPLY MICROPOWER QUAD PROGRAMMABLE GAIN AMPLIFIER

The combination of a quad OP490 and the DAC8408 quad 8-bit CMOS DAC creates a quad programmable-gain amplifier with a quiescent supply drain of only 140 μA. The digital code present at the DAC, which is easily set by a microprocessor, determines the ratio between the fixed DAC feedback resistor and the resistance of the DAC ladder seen by the op amp feedback loop. The gain of each amplifier is:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{256}{n}$$

where *n* equals the decimal equivalent of the 8-bit digital code present at the DAC. If the digital code present at the DAC consists of all zeros, the feedback loop opens causing the op amp output to saturate. The 10 MΩ resistors placed in parallel with the DAC feedback loop eliminate this problem with a very small reduction in gain accuracy. The 2.5 V reference biases the amplifiers to the center of the linear region providing maximum output swing.

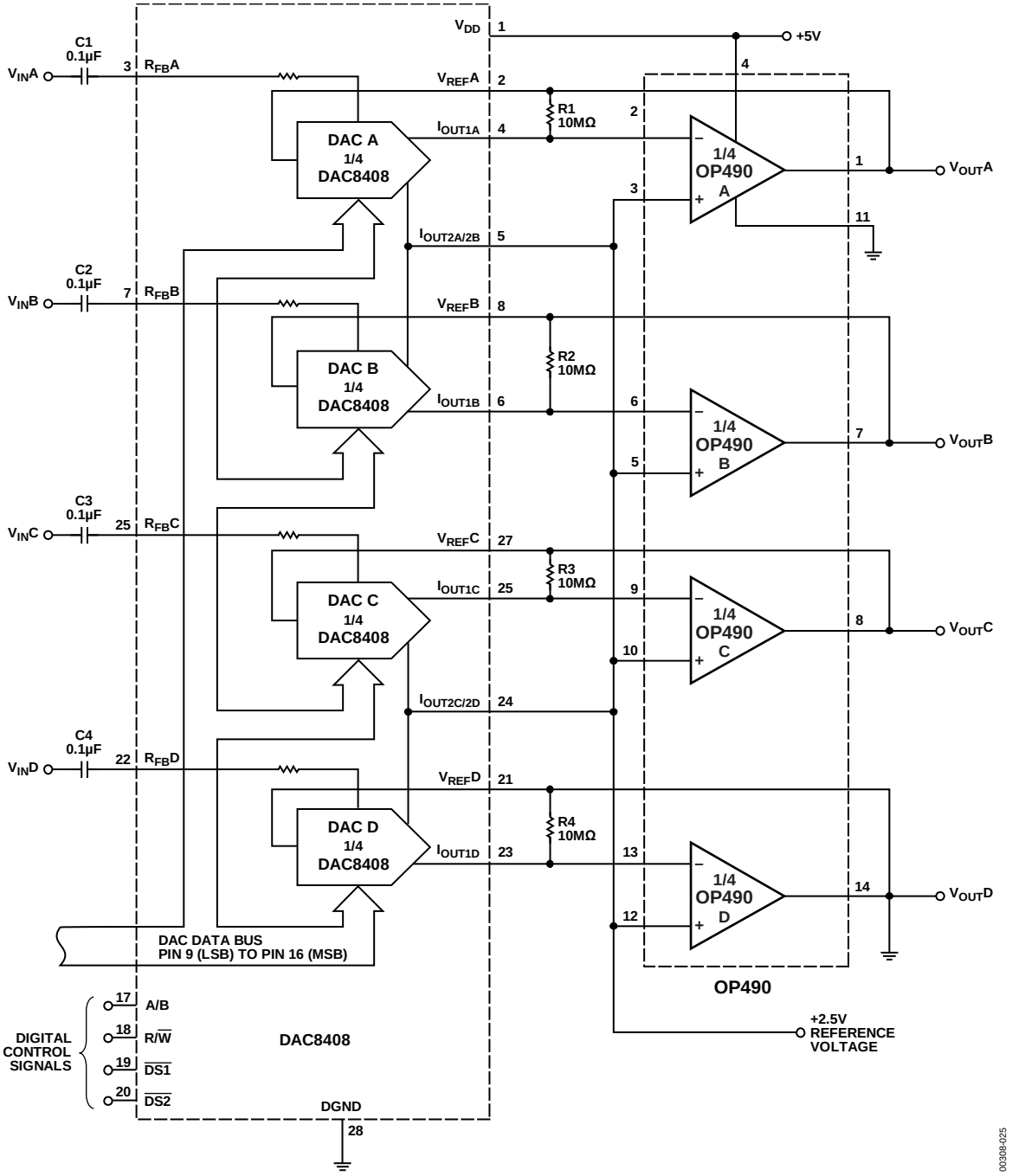
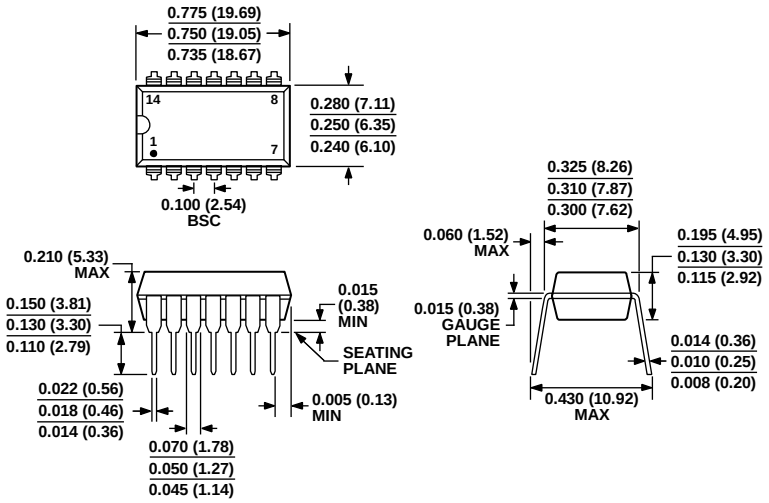


Figure 25. Single-Supply Micropower Quad Programmable Gain Amplifier

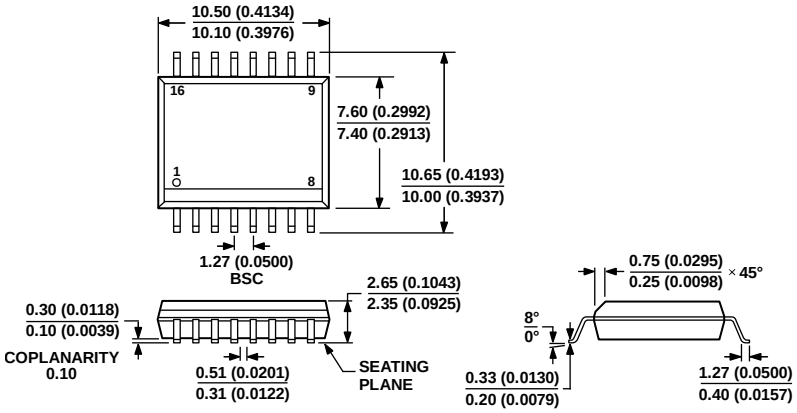
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

070606-A

Figure 26. 14-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
P-Suffix
(N-14)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-013-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

032707-B

Figure 27. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
S-Suffix
(RW-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
OP490GP	−40°C to +85°C	14-Lead PDIP_N	N-14 (P-Suffix)
OP490GPZ	−40°C to +85°C	14-Lead PDIP_N	N-14 (P-Suffix)
OP490GS	−40°C to +85°C	16-Lead SOIC_W	RW-16 (S-Suffix)
OP490GSZ	−40°C to +85°C	16-Lead SOIC_W	RW-16 (S-Suffix)
OP490GSZ-REEL	−40°C to +85°C	16-Lead SOIC_W	RW-16 (S-Suffix)

[1] Z = RoHS Compliant Part.

NOTES

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