TPS61096 28-V Output Voltage Boost Converter with Ultra-Low Quiescent Current

1 Features

- 1 µA ultra-low I_Q into VIN pin
- Operating Input Voltage from 1.8 V to 5.5 V
- Adjustable Output Voltage from 4.5 V to 28 V
- Selectable Inductor Peak Current:
  - 0.25 A and 0.5 A
- Integrated Power Diode
- Integrated Level Shifters
- 70% Efficiency at 10 µA load
- 12-Pin 3-mm x 2-mm WSON Package

2 Applications

- Stylus
- Memory LCD Bias
- Sensor Power
- General Purpose Bias
- RF Mems Relay Power

3 Description

The TPS61096 is a high output voltage boost converter with ultra-low quiescent current. It is designed for products that require high efficiency at light load conditions powered by either two-cell alkaline, or one-cell Li-Ion or Li-polymer battery.

The TPS61096 integrates a 30-V power switch and a power diode. It can output up to 28 Volts. The TPS61096 uses a PFM peak current control scheme to obtain the highest efficiency over a wide range of input and output load conditions. It only consumes 1 µA quiescent current and can achieve up to 70% efficiency under 10-µA load condition.

The TPS61096 can also support selective inductor peak current. With 250-mA current limit, the TPS61096 can reduce inductor ripple so that it reduces external component size for light load applications. With 500 mA current limit, the TPS61096 can provide 30 mA output current for a conversion from 3.3 V to 18 V.

The TPS61096 integrates two-channel low-power level shifters to convert low level signals to output voltage level signals for specific applications. It only consumes 1-µA static current per channel and ensures very low static and dynamic power consumption across the entire output range.

The TPS61096 is available in a 12-pin 3.0-mm x 2.0-mm WSON Package.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61096	WSON (12)	3 mm x 2 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit

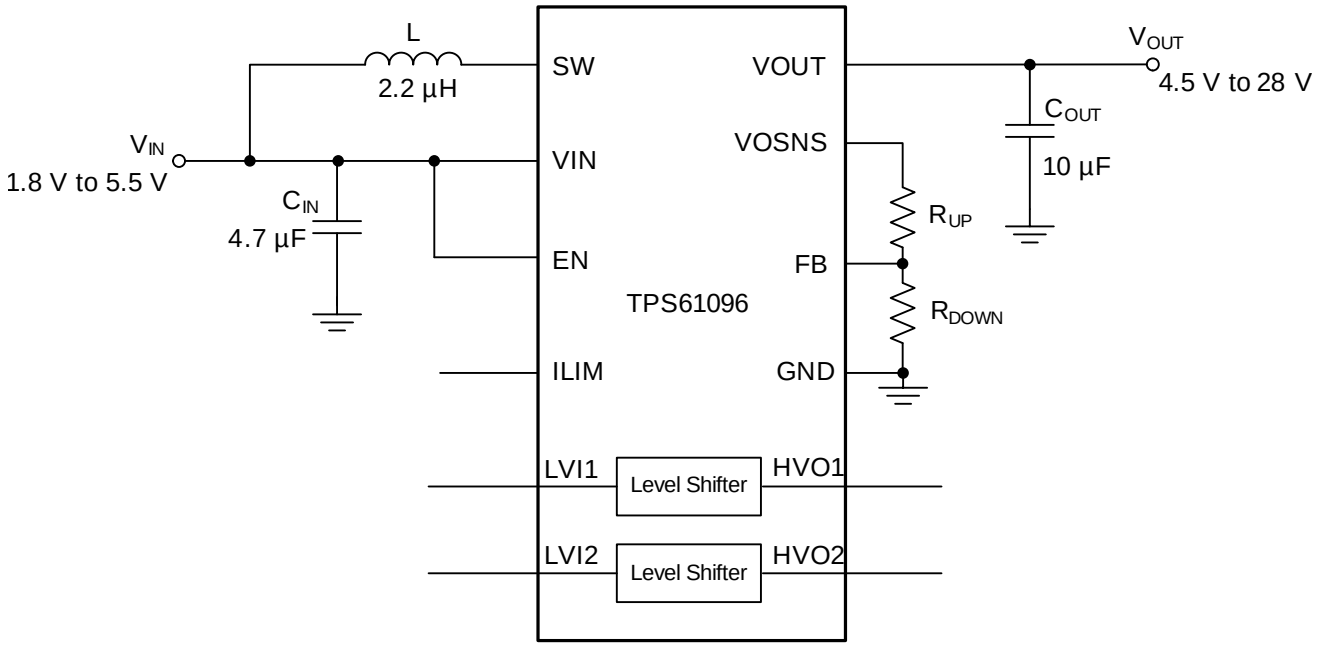


Table of Contents

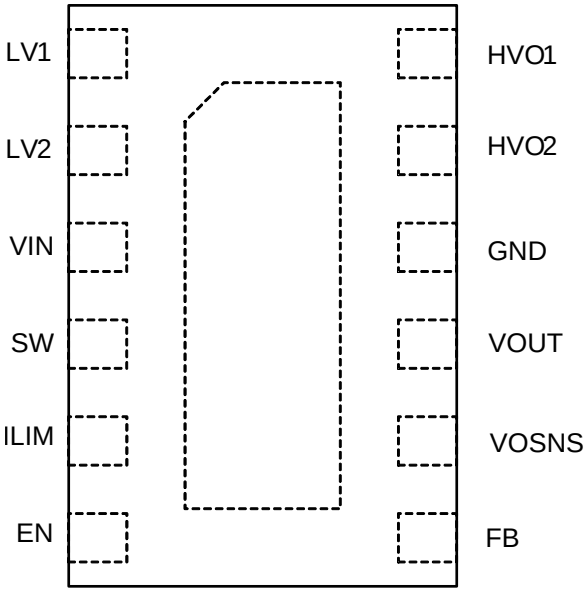
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (June 2016) to Revision A	Page
• Added full specification data - global	4

5 Pin Configuration and Functions

DSS Package
12-Pin WSON, 3 mm × 2 mm × 0.75 mm
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
LVI1	1	I	Input of level shifter 1
LVI2	2	I	Input of level shifter 2
VIN	3	I	IC power supply input
SW	4	PWR	Switch pin of the converter. It is connected to inductor.
ILIM	5	I	Inductor peak current limit selection pin. Logic low voltage to select 250mA peak current limit, logic high voltage to select 500mA peak current limit. Must be actively tied high or low. Do not leave it floating.
EN	6	I	Enable logic input. Logic high voltage enables the device, logic low voltage disables the device. Must be actively tied high or low. Do not leave it floating.
FB	7	I	Voltage feedback of adjustable output voltage. Connect to the center tap of a resistor divider to program the output voltage.
VOSNS	8	I/O	Boost converter output voltage sense pin. Connect an external resistor divider between this pin and FB pin.
VOUT	9	PWR	Boost converter output
GND	10	PWR	Ground pin
HVO2	11	O	Output of level shifter 2
HVO1	12	O	Output of level shifter 1

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage range at terminals	VIN, EN, ILIM, LVI1, LVI2	–0.3	6	V
	FB	-0.3	3.6	V
	SW, VOUT, VOSNS, HVO1, HVO2	–0.3	32	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	± 2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	± 500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	1.8		5.5	V
V_{OUT}	Boost converter output voltage	4.5		28	V
L	Inductor	1.0	2.2	47	µH
C_{IN}	Input capacitor	1.0	4.7		µF
C_{OUT}	Output capacitor	10	10	100	µF
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		TPS61096 DSS (WSON) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	10.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

-40°C ≤ T_J ≤ 125°C and V_{IN}=3.6V. Typical values are at T_J = 25°C, unless otherwise noted.

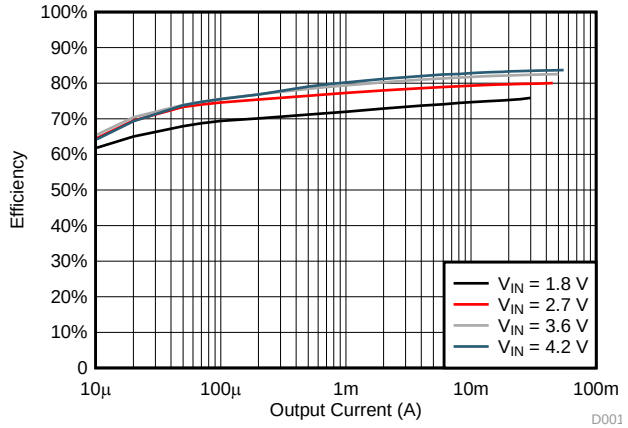
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		1.8		5.5	V
V_{UVLO}	Undervoltage lockout threshold	Input voltage rising		1.5	1.7	V
	Hysteresis			0.2	0.3	V
I_{Q_VIN}	Quiescent current into VIN pin	Device enabled, no load, no switching -40°C ≤ T_J ≤ 85 °C		1.2	2.5	µA
I_{Q_VOUT}	Quiescent current into VOUT pin	Device enabled internal LS main switch on, VOSNS switch on V_{OUT} = 20 V, I_Q to level shifter excluded, -40°C ≤ T_J ≤ 85 °C			0.2	µA
I_{SD}	Shutdown current into VIN pin	Device disabled -40°C ≤ T_J ≤ 85 °C		0.07	0.3	µA
OUTPUT						
V_{OUT}	Output voltage range		4.5		28	V
V_{REF}	Internal reference voltage		0.98	1	1.02	V
I_{OUT_LKG}	Leakage current into V_{OUT} pin	Device disabled V_{OUT} = 20 V -40°C ≤ T_J ≤ 85 °C			0.2	µA
I_{FB_LKG}	Leakage current into FB pin	V_{FB} = 1.0 V			0.2	µA
V_{OVP}	Output overvoltage protection threshold	Rising edge at VOUT pin	28.2	29.4	30.6	V
V_{OVP_HYS}	Overvoltage protection hysteresis		0.4	0.8	1.2	V
POWER SWITCH AND CURRENT LIMIT						
$R_{DS(on)}$	MOSFET on-resistance	V_{IN} = 3.6 V		450	700	mΩ
I_{ILIM}	Peak switch current limit	ILIM = Low	0.15	0.25	0.35	A
		ILIM = High	0.35	0.5	0.6	A
t_{SS}	Soft-start time			1	4.5	ms
I_{SW_LKG}	Leakage current into SW pin (from SW pin to GND)	Device disabled , V_{SW} = 20 V -40°C ≤ T_J ≤ 85 °C			0.5	µA
LEVEL SHIFTER						
I_{Q_LS}	Level shifters quiescent current into V_{OUT} pin	Both level shifter channel enabled, LVIx = Low		0.5	1	µA
		Both level shifter channel enabled, LVIx = High		1.5	3	µA
f_{PULSE}	Pulse frequency	C_{HVOx} ≤ 10 pF			200	kHz
V_{IL}	Low level input voltage threshold at LVIx pin	Falling edge	0.15 × Vin			V
V_{IH}	High level input voltage threshold at LVIx pin	Rising edge			0.8 × Vin	V
V_{OH}	High-level output voltage at HVOx pin	12 V ≤ V_{OUT} ≤ 28 V I_{HVOx} = 10 µA	V_{OUT} – 0.1 V			V
		12 V ≤ V_{OUT} ≤ 28 V I_{HVOx} = 100 µA	V_{OUT} – 0.3 V			V
V_{OL}	Low-level output voltage at HVOx	12 V ≤ V_{OUT} ≤ 28 V I_{HVOx} = -10 µA			0.1	V
		12 V ≤ V_{OUT} ≤ 28 V I_{HVOx} = -100 µA			0.3	V
I_{SRC}	Level shifter high-side FET sourcing current	V_{OUT} = 20 V, V_{HVOx} = 0 V	800			µA
I_{SINK}	Level shifter low-side FET sinking current	V_{HVOx} = 20 V	800			µA

Electrical Characteristics (continued)

-40°C ≤ T_J ≤ 125°C and V_{IN}=3.6V. Typical values are at T_J = 25°C, unless otherwise noted.

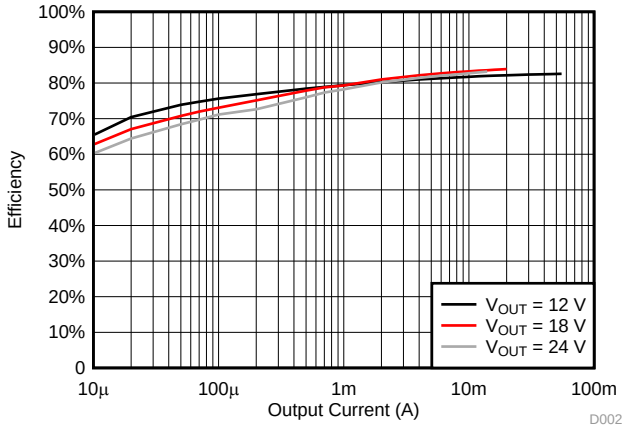
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{in}	Input leakage current at LVIx pin	V_{OUT} = 0 V to 28 V V_{LVIx} = 0 V to 4.5 V			0.5	µA
t_{pd}	Propagation delay from input to output	V_{OUT} = 20 V, C_{HVOx} = 5 pF From V_{LVIx} rising above 0.8×Vin to V_{HVOx} rising above 2 V			500	ns
		V_{OUT} = 20 V, C_{HVOx} = 5 pF From V_{LVIX} falling below 0.15×Vin to V_{HVOx} falling below 18 V			500	ns
Control Logic						
V_{IL_EN}	EN pin low level input voltage threshold		0.4			V
V_{IH_EN}	EN pin high level input voltage threshold				1.2	V
V_{IL_ILIM}	ILIM pin low level input voltage threshold		0.4			V
V_{IH_ILIM}	ILIM pin high level input voltage threshold				1.2	V
I_{EN_LKG}	Leakage current into EN pin	V_{EN} = 5 V -40°C ≤ T_J ≤ 85 °C			50	nA
I_{ILIM_LKG}	Leakage current into ILIM pin	V_{ILIM} = 5 V -40°C ≤ T_J ≤ 85 °C			50	nA
Protection						
T_{SD}	Overtemperature protection	T_J rising		150		°C
T_{SD_HYS}	Overtemperature hysteresis	T_J falling below T_{SD}		25		°C

6.6 Typical Characteristics



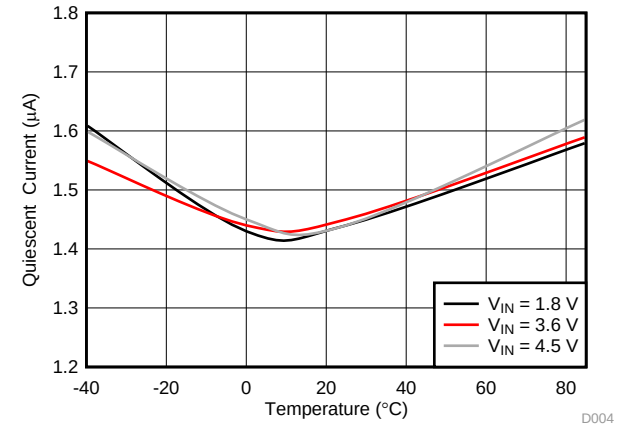
V_{IN} =1.8 V, 2.7 V, 3.6 V, 4.2 V V_{OUT}= 12 V

Figure 1. Load Efficiency with Different Inputs



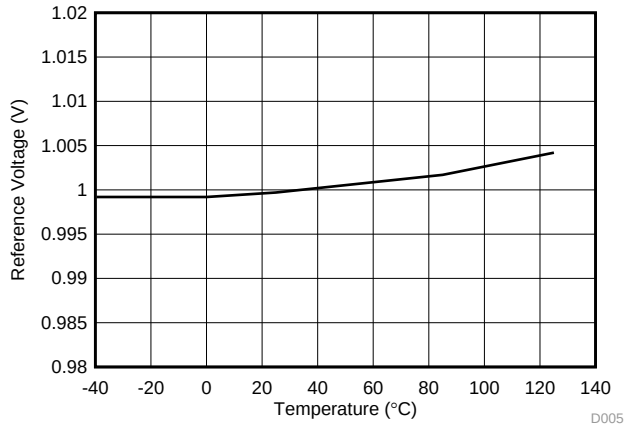
V_{IN} = 3.6 V V_{OUT} = 12 V, 18 V, 24 V

Figure 2. Load Efficiency with Different Outputs



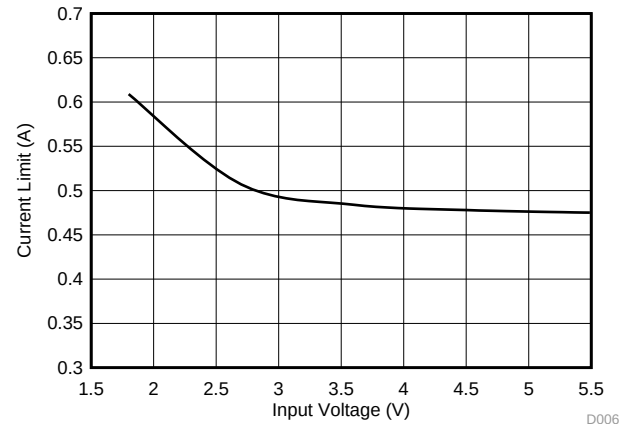
V_{IN} = 1.8 V, 3.6 V, 4.5 V No switching

Figure 3. Quiescent Current into V_{IN} vs Temperature



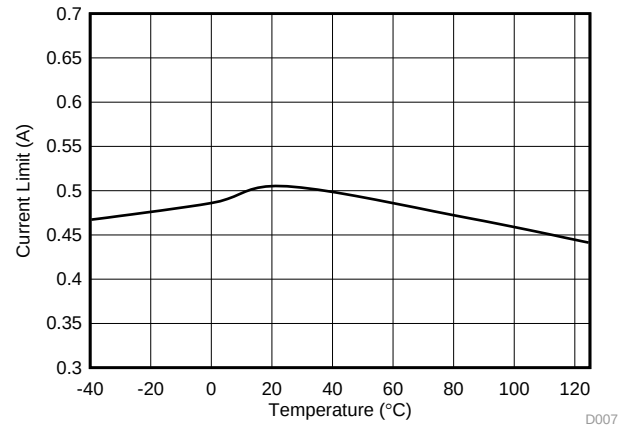
V_{IN} = 3.6 V T_J= –40°C to 125°C

Figure 4. Reference Voltage vs Temperature



V_{IN}= 1.8 V to 5.5 V T_J= 25°C

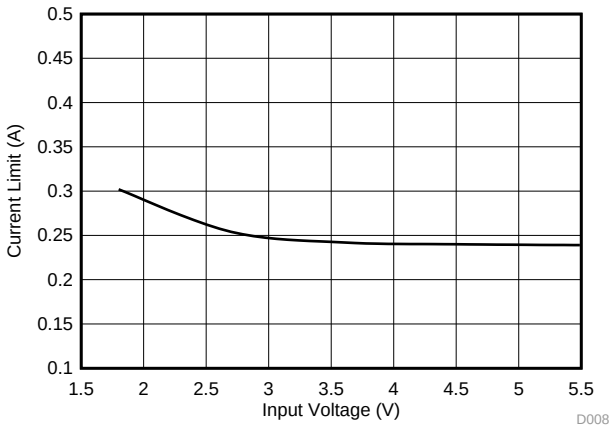
Figure 5. Current Limit vs V_{IN} with I_{LIM} = H



V_{IN}= 3.6 V T_J = –40°C to 125°C

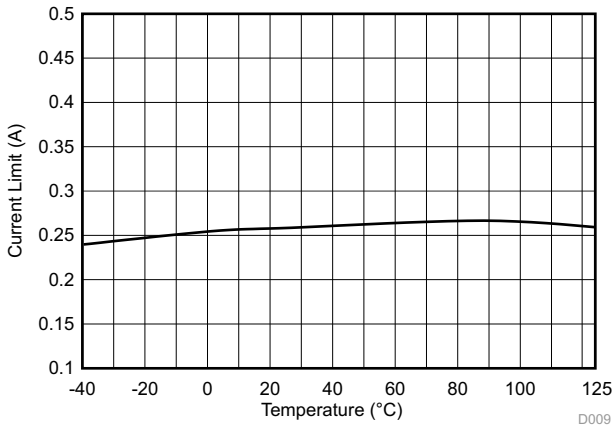
Figure 6. Current Limit vs Temperature with I_{LIM} = H

Typical Characteristics (continued)



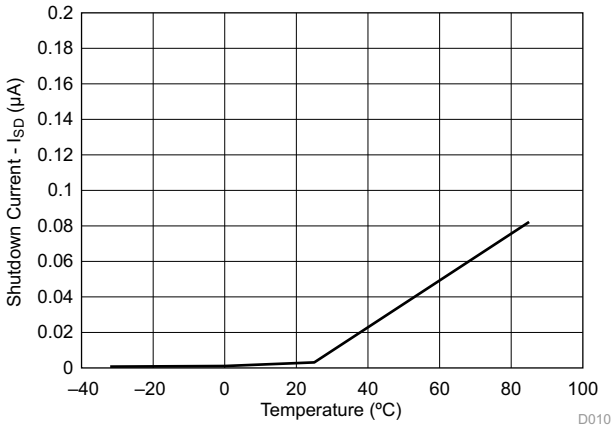
V_{IN}= 1.8 V to 5.5 V T_J = 25°C

Figure 7. Current Limit vs V_{IN} with I_{LIM} = L



V_{IN}= 3.6 V T_J = –40°C to 125°C

Figure 8. Current Limit vs Temperature with I_{LIM} = L



V_{IN}= 3.6 V into V_{IN} Pin T_J = –40°C to 85°C

Figure 9. Shutdown Current vs Temperature

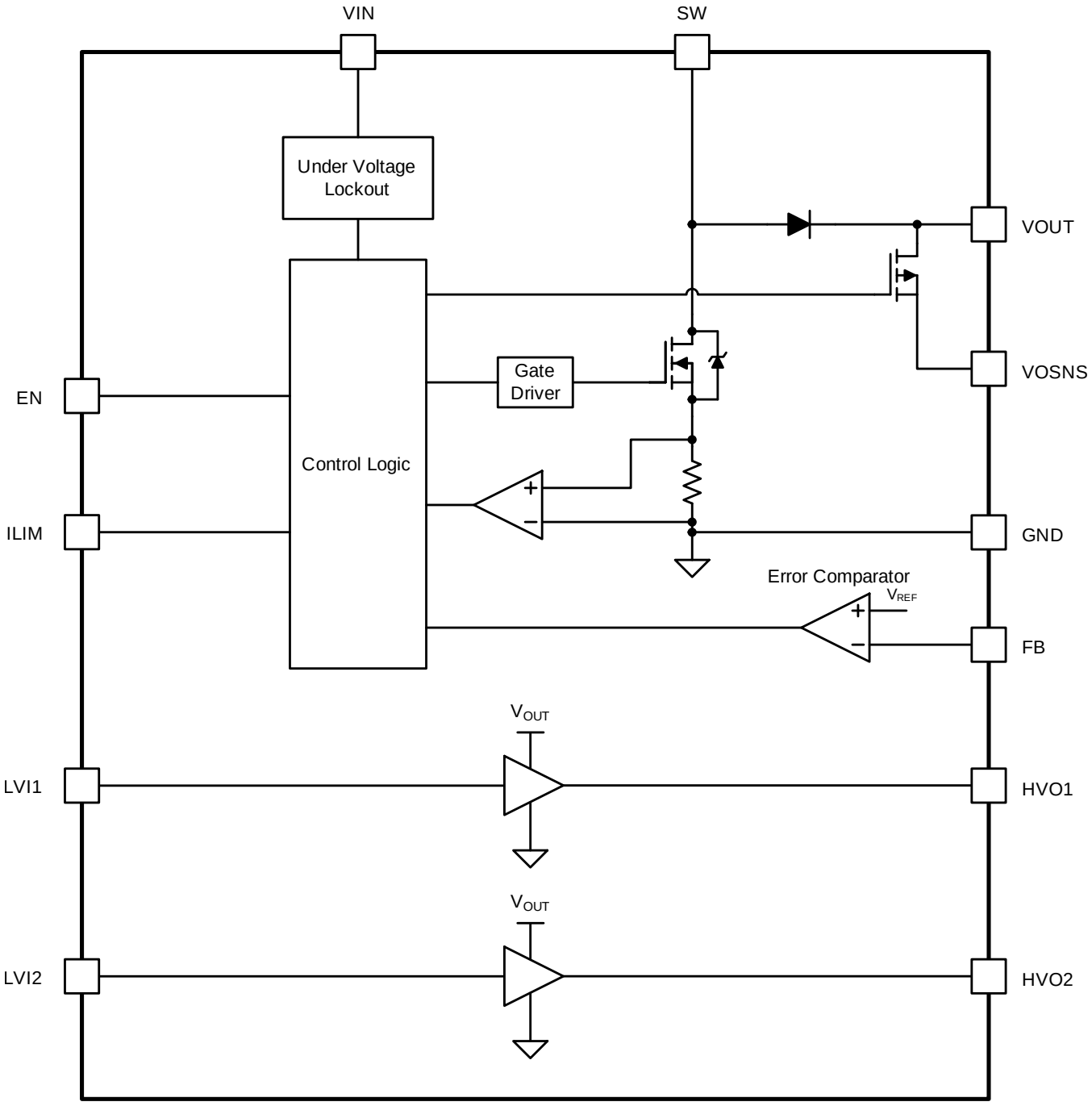
7 Detailed Description

7.1 Overview

The TPS61096 operates with an input voltage range of 1.8 V to 5.5 V and can generate output voltage up to 28 V. The device operates in a PFM peak current control scheme with selective peak current. This control scheme consumes very low quiescent current so that it is able to achieve high efficiency at light load condition.

The TPS61096 integrates two-channel low power level shifters to convert low voltage logic signals to output voltage for specific applications. It only consumes 1µA static current per channel and ensures very low static and dynamic power consumption across the entire output range.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Controller Circuit

The TPS61096 operates in a PFM with peak current control scheme. The converter monitors the output voltage through feedback pin. As soon as the feedback voltage falls below the reference voltage of typical 1 V, the internal switch turns on and the inductor current ramps up. The switch turns off as soon as the inductor current reaches the setting peak current limit. As the switch turns off, the internal power diode is forward biased and delivers the inductor current to the output. After the inductor current drops to zero, the TPS61096 compares the feedback voltage with the reference voltage. Once feedback voltage falls below the reference voltage, the switch turns on again. In this way, the TPS61096 regulates the output voltage at the target value.

Using this PFM peak current control scheme the converter operates in discontinuous conduction mode (DCM) where the switching frequency depends on the output current. This regulation scheme is inherently stable, allowing a wide selection range for the inductor and output capacitor.

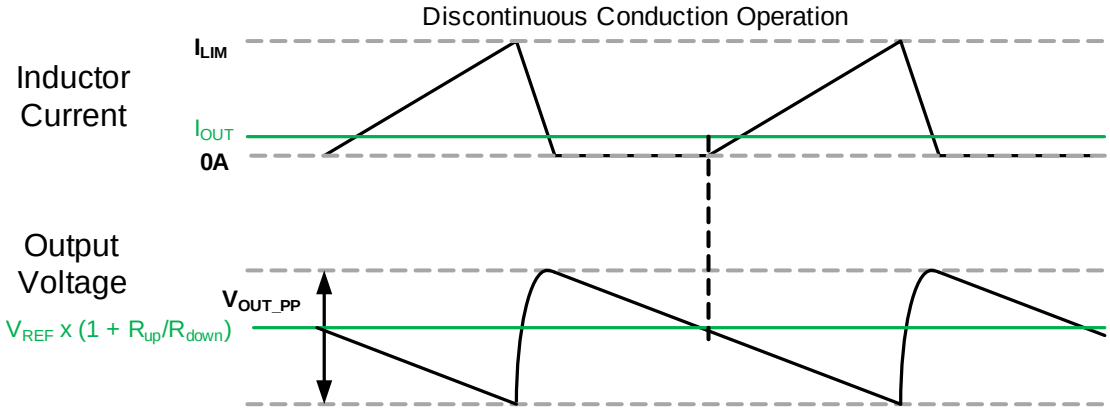


Figure 10. PFM Peak Current Control Operation

7.3.2 Current Limit Selection

The TPS61096 supports selectable current limit thresholds. If the ILIM pin is pulled logic high voltage, a high current limit (500 mA typ.) is selected; if the ILIM pin is connected to logic low voltage, a low current limit (250 mA typ.) is selected. With the low current limit threshold, the TPS61096 allows the use of small size external components, especially the inductor, for light load applications.

7.4 Device Functional Modes

7.4.1 Under-Voltage Lockout

An under-voltage lockout (UVLO) circuit stops the operation of the converter when the input voltage drops below the typical UVLO threshold of 1.3 V. A hysteresis of 200 mV is added so that the device cannot be enabled again until the input voltage goes up to 1.5 V. This function is implemented in order to prevent malfunctioning of the device when the input voltage is between 1.3 V and 1.5 V.

7.4.2 Enable and Disable

When the input voltage is above maximal UVLO rising threshold of 1.7 V and the EN pin is pulled high, the TPS61096 is enabled. When the EN pin is pulled low, the device stops switching, the TPS61096 goes into shutdown mode. In shutdown mode, less than 1-µA input current is consumed.

7.4.3 Soft Start

The TPS61096 begins soft start when the EN pin is pulled high. An internal soft-start circuit increases the peak inductor current limit to the final value within typical 1 ms. The soft-start function reduces the inrush current during startup.

7.4.4 Level Shifters

The TPS61096 contains two level shifter channels. Each channel features a logic-level input stage and a high voltage output stage powered from VOUT. The logic low input must be lower than 0.15 × Vin and logic high input must be higher than 0.8 × Vin. The level shifters have 200-µA sourcing and sinking capability, and are capable of generating up to 200 kHz pulses with up to 10pF capacitive load connected to the outputs.

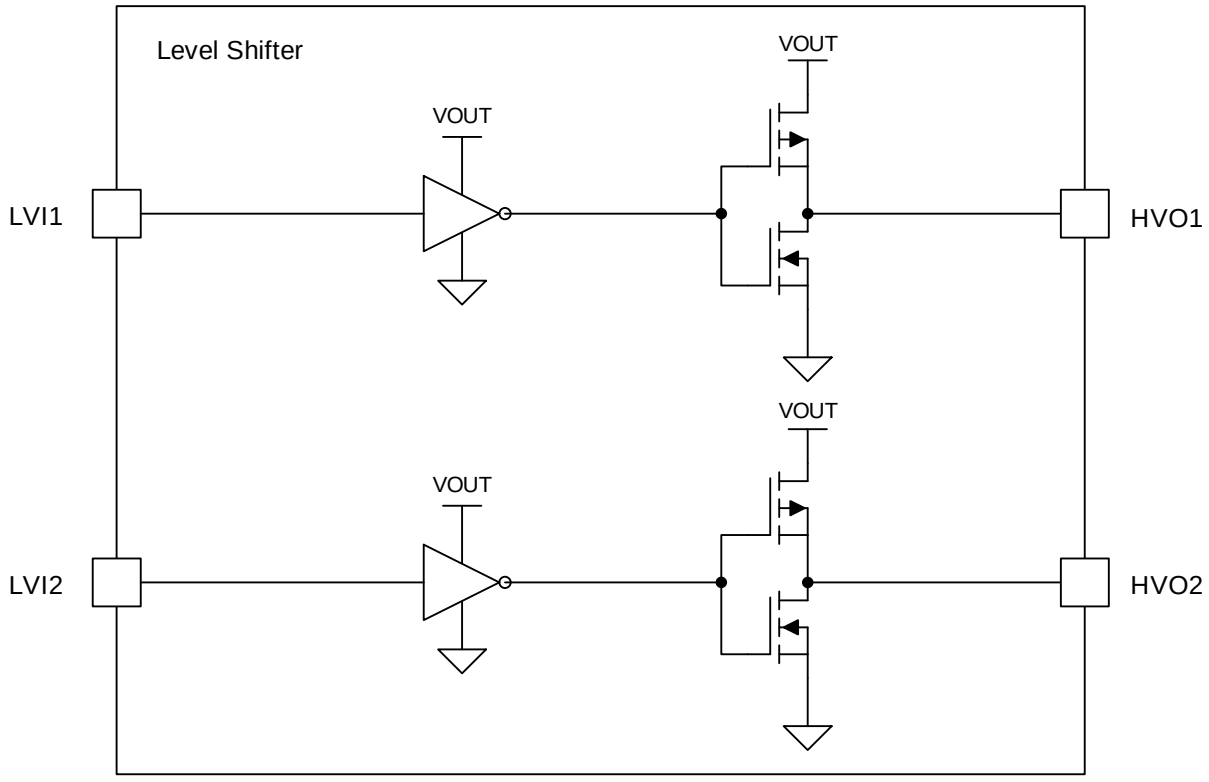


Figure 11. Level Shifter Schematic Illustration

Device Functional Modes (continued)

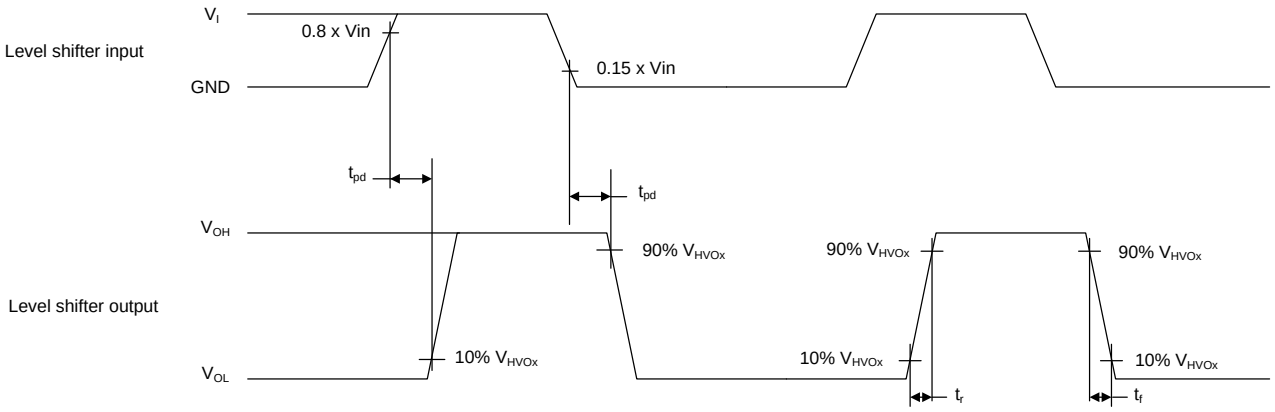


Figure 12. Level Shifter Timing Diagram

7.4.5 Over-voltage Protection

The TPS61096 has internal output over-voltage protection (OVP) function. When the output voltage exceeds the OVP threshold of 29.4 V, the device stops switching. Once the output voltage falls 0.8 V below the OVP threshold, the device resumes operating again.

7.4.6 Thermal Shutdown

The TPS61096 goes into thermal shutdown once the junction temperature exceeds 150°C. When the junction temperature drops below the thermal shutdown temperature threshold minus the hysteresis, typically 125°C, the device starts operating again.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS61096 is a high output voltage boost converter with ultra-low quiescent current. It is designed for products powered by either two-cell alkaline, or one cell Li-Ion or Li-polymer battery, for which high efficiency under light load condition is critical to achieve long battery life operation. It can also support selective inductor peak current. With lower current limit, the TPS61096 can reduce inductor ripple so as to reduce external components size for light load applications. With higher current limit, the TPS61096 can have higher output current capability to meet more application requirements.

The TPS61096 integrates two-channel low-power level shifters to convert low level signals to output voltage signals for specific applications.

8.2 Typical Application

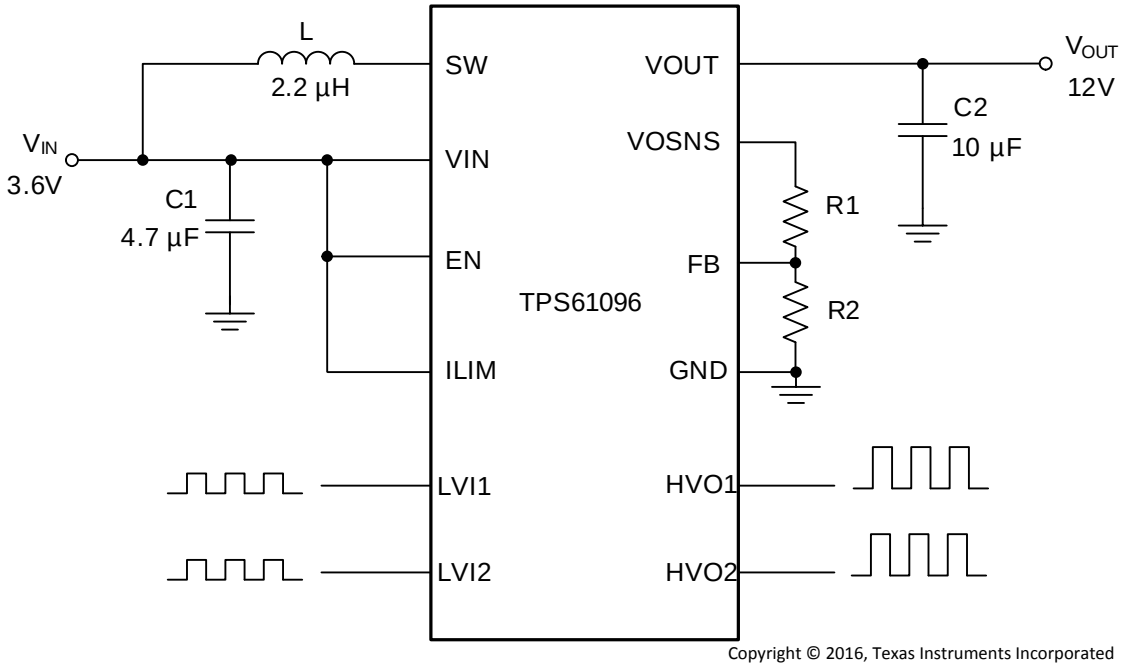


Figure 13. 12-V Pulse Generation From 3.6-V Input Voltage

8.2.1 Design Requirements

In this typical application, two channel 50-kHz pulse signals of 3.2 V amplitude are output from a controller, and the signals' amplitude is required to be converted. High efficiency under light load is required.

The TPS61096 converts the 3.6-V input voltage to 12-V output voltage first, and this 12-V output voltage provides bias to the integrated two level shifters. The level shifters outputs have no load so the boost converter always works in light load condition.

Table 1. TPS61096 Design Parameters

PARAMETER	EXAMPLE VALUES
Input voltage	3.6 V
Output voltage	12 V
Input pulse frequency	50 kHz
Input pulse duty cycle	50%
Input pulse amplitude	3.2 V
Output pulse frequency and duty cycle	Same as input pulse
Output pulse amplitude	12 V
Output load of level shifters	No load

8.2.2 Detailed Design Procedure

The following sections describe the selection process of the external components.

8.2.2.1 Programming the Output Voltage

By selecting the external resistor divider R1 and R2, as shown in Equation 1, the output voltage is programmed to the desired value. When the output voltage is regulated, the typical V_{REF} voltage at FB pin is 1.0 V.

$$V_{OUT} = V_{REF} \times \frac{R1 + R2}{R2} \quad (1)$$

For the best accuracy, the current following through R2 should be 100 times larger than FB pin leakage current. Changing R2 towards a lower value increases the robustness against noise injection while has little influence on efficiency at light load, because TPS61096 only samples FB voltage when it is lower than the reference. 110-kΩ and 10-kΩ resistors are selected for R1 and R2. High accuracy resistors are recommended for better output voltage accuracy.

8.2.2.2 Maximum Output Current

The maximum output capability of the TPS61096 is determined by the input voltage to output voltage ratio and the current limit of the boost converter. It can be estimated by Equation 2.

$$I_{OUT(max)} = \frac{V_{IN} \times I_{LIM} \times \eta}{2 \times V_{OUT}} \quad (2)$$

where

- V_{IN} is the input voltage
- V_{OUT} is the output voltage
- I_{LIM} is the peak current limit
- η is the power conversion efficiency

If an application requires high output current capability of the boost converter, ILIM pin should be tied to logic high voltage to enable a higher current limit. Minimum input voltage, maximum boost output voltage and minimum value of the selected current limit should be used as the worst case condition for the estimation.

In this example, the output load is only the bias current to the level shifters, so it will not reach the maximum output current value.

8.2.2.3 Inductor Selection

Because the PFM peak current control scheme is inherently stable, the inductor value does not affect the stability of the regulator. The selection of the inductor together with the nominal load current, input and output voltage of the application determines the switching frequency of the converter. Depending on the application, inductor values from 1.0 µH to 47 µH are recommended.

The inductor value determines the maximum switching frequency of the converter. Therefore, select the inductor value that ensures the maximum switching frequency at the converter maximum load current does not exceed the required maximum switching frequency. The maximum switching frequency is calculated by Equation 3:

$$f_{s(max)} = \frac{V_{IN} \times (V_{OUT} - \eta \times V_{IN})}{L \times V_{OUT} \times I_{LIM}} \quad (3)$$

where

- L is the selected inductor value

Choose the smaller one between $V_{IN(max)}$ and $\frac{\eta \times V_{OUT}}{2}$ to calculate the highest switching frequency across the entire input range.

The selected inductor should have a saturation current that is larger than the maximum peak current of the converter. Use the minimal value of selected current limit for this calculation.

Another important inductor parameter is the dc resistance. The lower the dc resistance, the higher the efficiency of the converter. Table 2 lists the recommended inductors for the TPS61096.

Table 2. Recommended Inductors

INDUCTANCE (µH)	ISAT (A)	DC RESISTANCE (mΩ)	PACKAGE SIZE	PART NUMBER	MANUFACTURER(1)
2.2	1.7	117	2.0 mm × 1.6 mm	DFE201610E-2R2M=P2	TOKO
2.2	1.5	106	3.2 mm × 2.5 mm	74479299222	Wurth
2.2	0.7	200	2.0 mm × 1.2 mm	74479775222A	Wurth

(1) See Third-Party Products disclaimer

8.2.2.4 Capacitor Selection

For best output and input voltage filtering, low ESR X5R or X7R ceramic capacitors are recommended.

The input capacitor minimizes input voltage ripple, suppresses input voltage spikes and provides a stable system rail for the device. An input capacitor value of 4.7 µF is normally recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. A ceramic capacitor placed as close as possible to the VIN and GND pins of the IC is recommended.

The selection of output capacitor determines the output voltage ripple. The default hysteresis window of Vout is 30mV, but due to the 10-µs internal comparator delay, output ripple gets larger as load gets heavier. The output ripple is calculated with Equation 4:

$$V_{RIPPLE} = \frac{I_{OUT} \times t_{delay}}{C_{OUT}} + 30\ mV \quad (4)$$

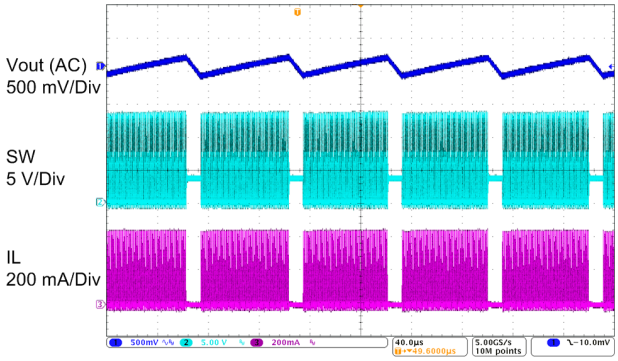
where

- V_{RIPPLE} refers to the output voltage ripple
- t_{delay} is the internal comparator delay time, typical value 10 µs
- C_{OUT} is effective output capacitance

For the output capacitor of VOUT pin, small ceramic capacitors are recommended. Place the output capacitor as close as possible to the VOUT and GND pins of the IC. If, for any reason, the application requires the use of large capacitors which cannot be placed close to the IC, the use of a small ceramic capacitor with a capacitance value of 1 µF in parallel to the large one is recommended. This small capacitor should be placed as close as possible to the VOUT and GND pins of the IC. The recommended typical output capacitor values are 10 µF (nominal value).

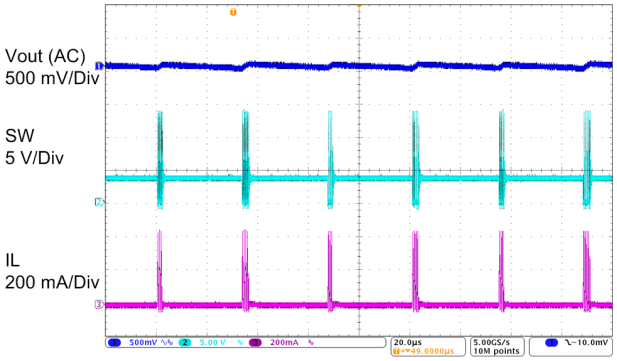
When selecting capacitors, the derating effect of the ceramic capacitor under bias should be considered. Choose the right nominal capacitance by checking the DC bias characteristics of the capacitor. In this example, GRM188R6YA106MA73D, a 10-µF ceramic capacitor with high effective capacitance value at DC biased condition, is selected for the VOUT rail. The performance is shown in the *Application Curves* section.

8.2.3 Application Curves



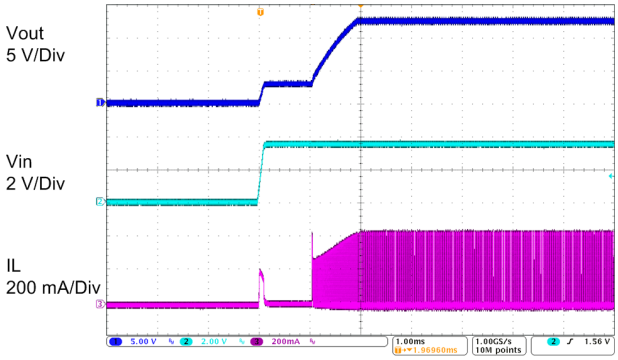
Vin=3.6 V, Vout=12 V, Iout=30 mA

Figure 14. Switching Waveform at Heavy Load



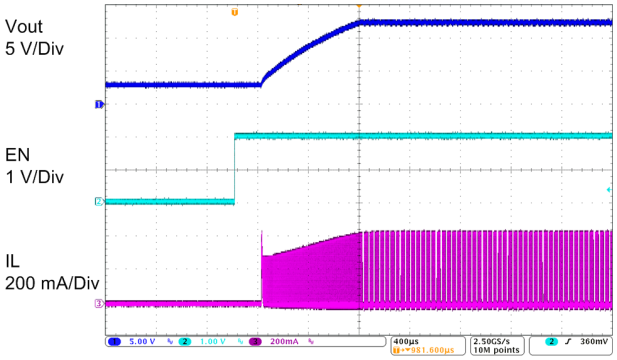
Vin=3.6 V, Vout=12 V, Iout=2 mA

Figure 15. Switching Waveform at Light Load



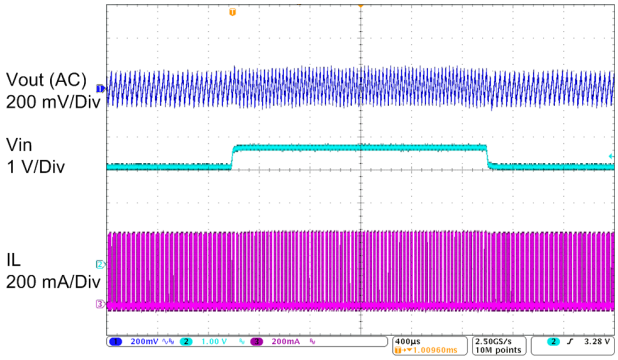
Vin=3.6 V, Vout=12 V, Iout=25 mA

Figure 16. Startup by VIN



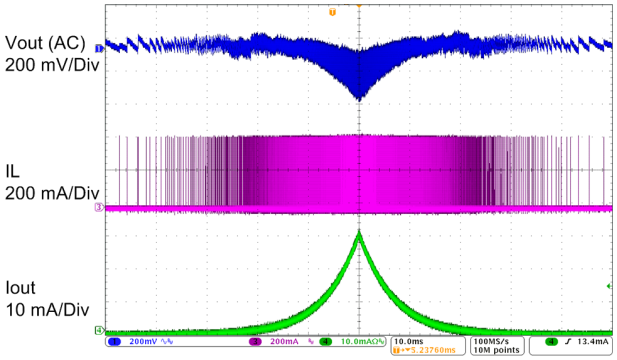
Vin=3.6 V, Vout=12 V, Iout=25 mA

Figure 17. Startup by EN



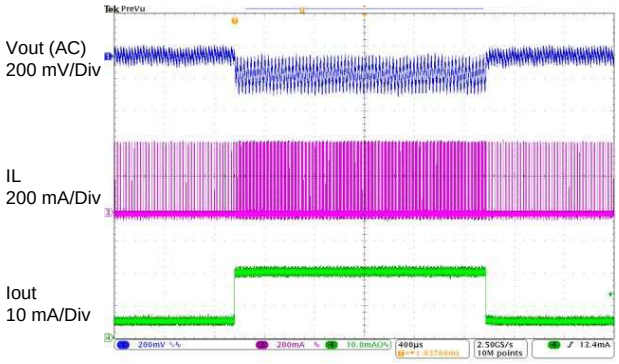
Vin=3.0 V to 3.6 V, Vout=12 V, Iout=20 mA

Figure 18. Line Transient



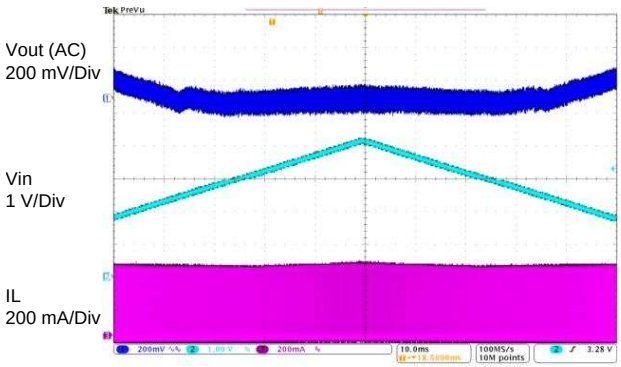
Vin=3.6 V, Vout=12 V, Iout=0 mA to 30 mA

Figure 19. Load Regulation



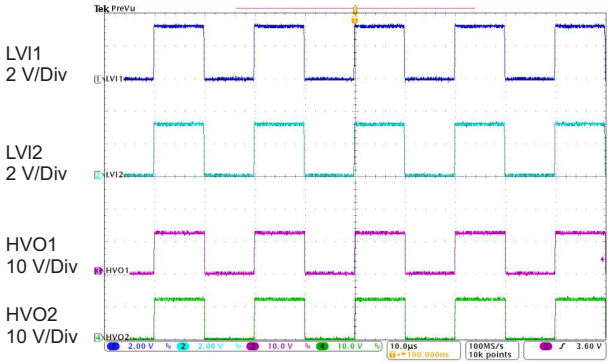
Vin=3.6 V, Vout=12 V, Iout=5 mA to 20 mA

Figure 20. Load Transient



Vin=1.8 V to 4.2 V, Vout=12 V, Iout=20 mA

Figure 21. Line Regulation



LVI1 = LVI2 = 3.2 V, HVO1 = HVO2 = 12 V

Figure 22. Level Shifters Function

9 Power Supply Recommendations

TPS61096 is designed to operate from an input voltage supply range between 1.8 V to 5.5 V. The power supply can be either two-cell alkaline, or one cell Li-Ion or Li-polymer battery. The input supply must be well regulated with the rating of TPS61096. If the input supply is located more than a few inches from the converter, a bulk capacitance may be required in addition to the ceramic bypass capacitors.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak current and high switching frequency. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground paths. The input and output capacitor, as well as inductor should be placed as close as possible to the IC.

10.2 Layout Example

A large ground plane on the bottom layer connects the ground pins of the components on the top layer through vias.

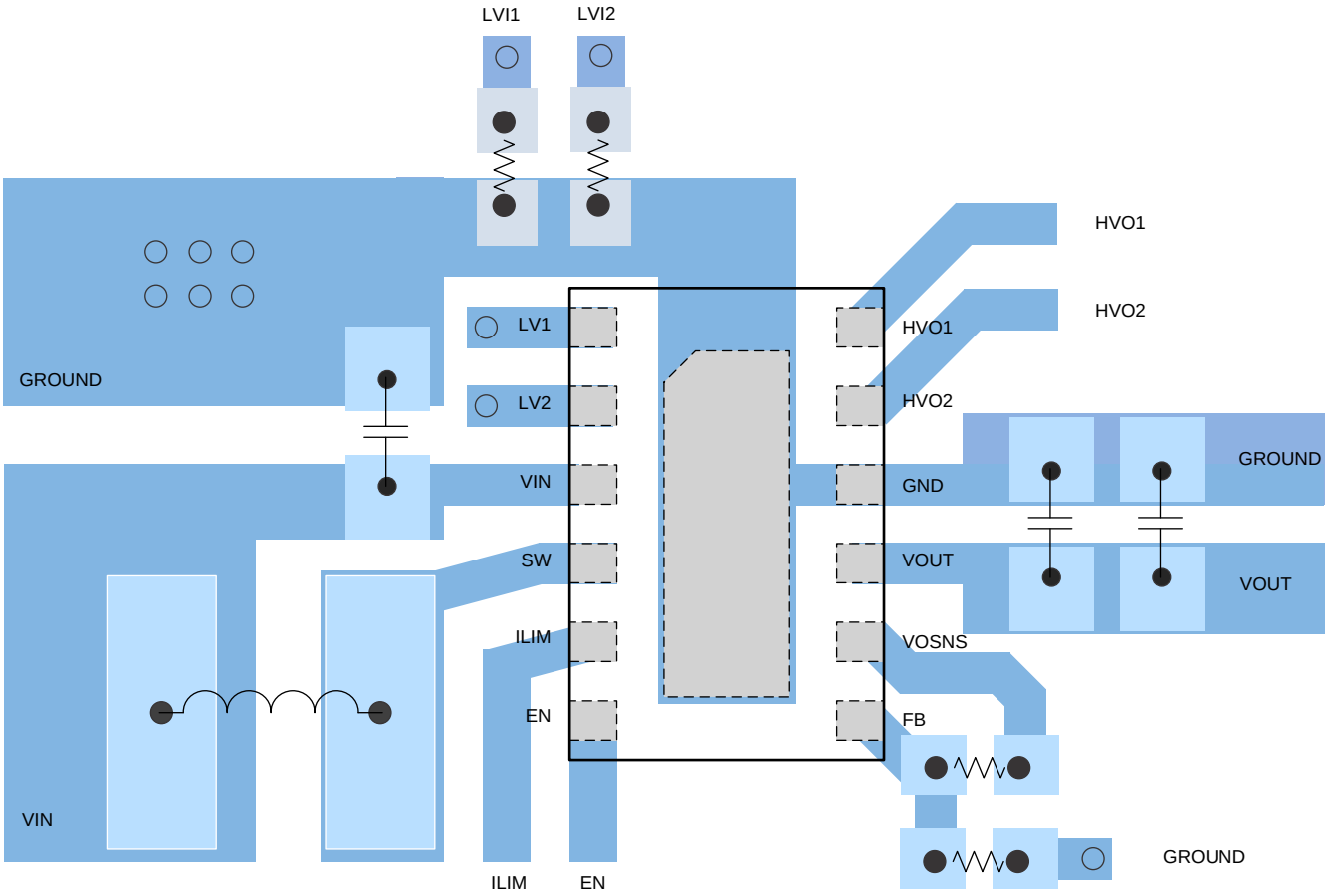


Figure 23. Example PCB Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

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11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61096DSSR	ACTIVE	WSON	DSS	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	S61096	Samples
TPS61096DSST	ACTIVE	WSON	DSS	12	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	S61096	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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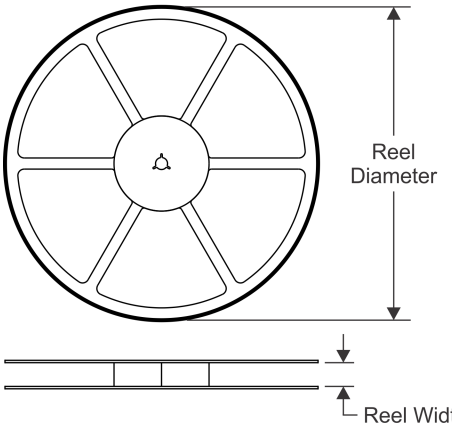
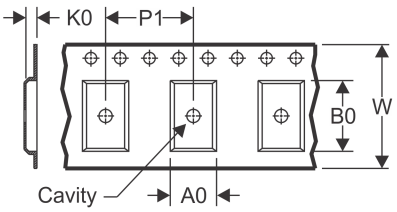
TAPE AND REEL INFORMATION

REEL DIMENSIONS

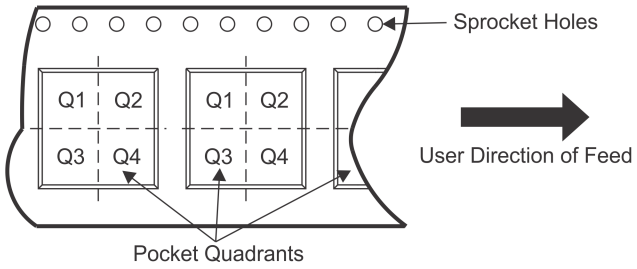


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

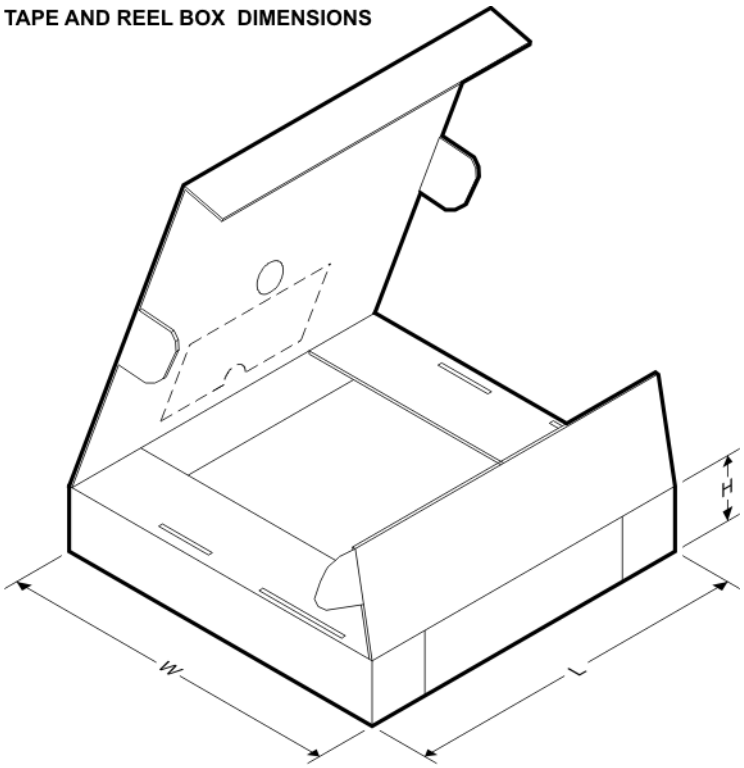
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61096DSSR	WSON	DSS	12	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS61096DSST	WSON	DSS	12	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

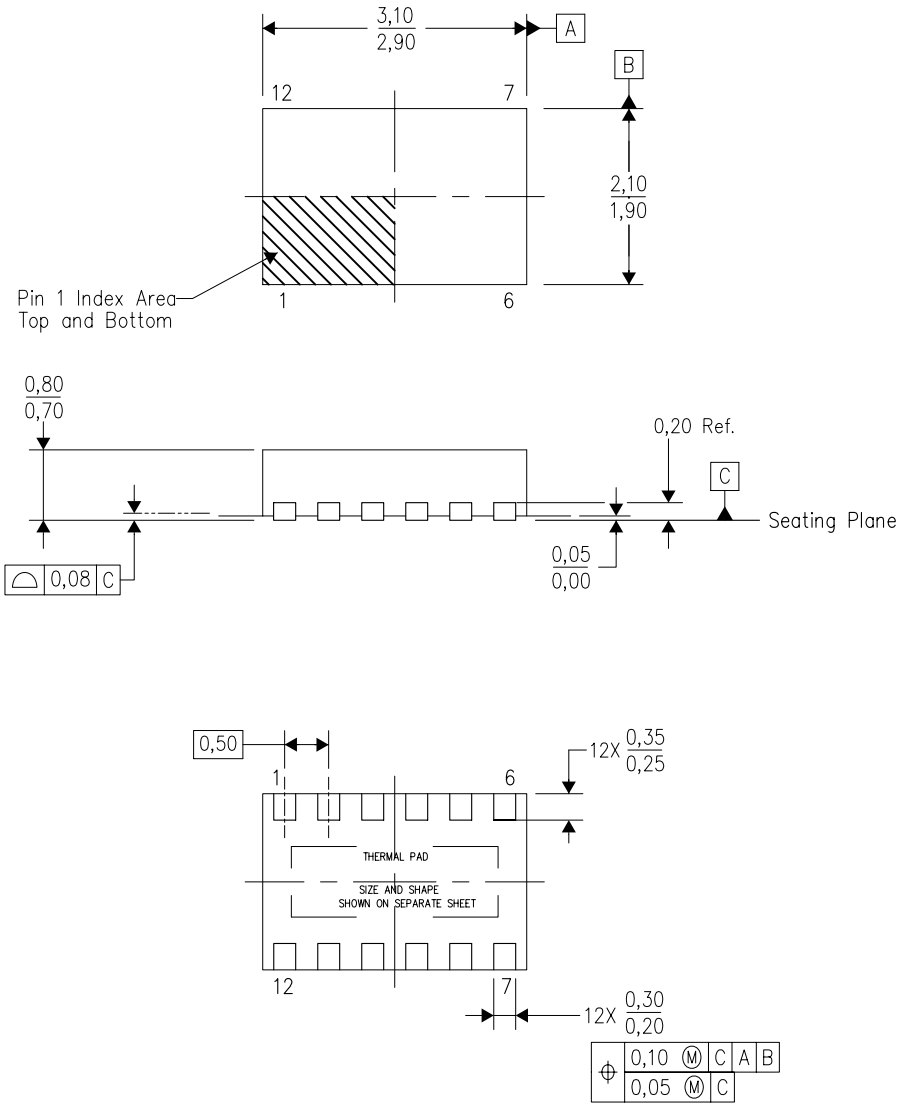
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61096DSSR	WSON	DSS	12	3000	210.0	185.0	35.0
TPS61096DSST	WSON	DSS	12	250	210.0	185.0	35.0

DSS (R–PWSON–N12) PLASTIC SMALL OUTLINE NO–LEAD



4209244/C 07/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

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