



Is Now Part of



**ON Semiconductor®**

To learn more about ON Semiconductor, please visit our website at

[www.onsemi.com](http://www.onsemi.com)

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## 74LVT162245 • 74LVTH162245

### Low Voltage 16-Bit Transceiver with 3-STATE Outputs and 25Ω Series Resistors in A Port Outputs

#### General Description

The LVT162245 and LVTH162245 contains sixteen non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The T/R inputs determine the direction of data flow through the device. The OE inputs disable both the A and B ports by placing them in a high impedance state.

The LVT162245 and LVTH162245 are designed with equivalent 25Ω series resistance in both the HIGH and LOW states on the A Port outputs. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

The LVTH162245 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These non-inverting transceivers are designed for low voltage (3.3V) V<sub>CC</sub> applications, but with the capability to provide a TTL interface to a 5V environment. The LVT162245 and LVTH162245 are fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

#### Features

- Input and output interface capability to systems at 5V V<sub>CC</sub>
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs (74LVTH162245), also available without bushold feature (74LVT162245).
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- A Port outputs include equivalent series resistance of 25Ω making external termination resistors unnecessary and reducing overshoot and undershoot
- A Port outputs source/sink ±12 mA.  
B Port outputs source/sink -32 mA/+64 mA
- Functionally compatible with the 74 series 162245
- Latch-up performance exceeds 500 mA
- ESD performance:  
Human-body model > 2000V  
Machine model > 200V  
Charged-device model > 1000V
- Also packaged in plastic Fine Pitch Ball Grid Array (FBGA)

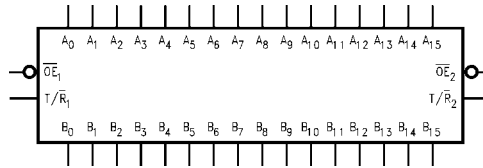
#### Ordering Code:

Order Number	Package Number	Package Description
74LVT162245G (Note 1)(Note 2)	BGA54A (Preliminary)	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
74LVT162245MEA (Note 2)	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74LVT162245MTD (Note 2)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
74LVTH162245G (Note 1)(Note 2)	BGA54A	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
74LVTH162245MEA	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide [TUBE]
74LVTH162245MEX	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide [TAPE and REEL]
74LVTH162245MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [TUBE]
74LVTH162245MTX	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [TAPE and REEL]

**Note 1:** Ordering code "G" indicates Trays.

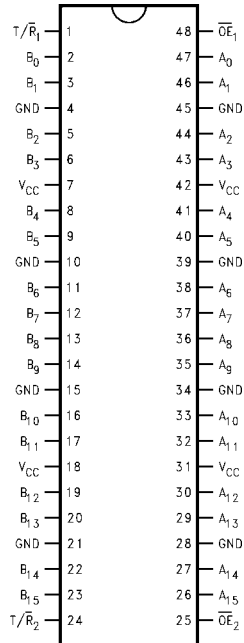
**Note 2:** Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Symbol

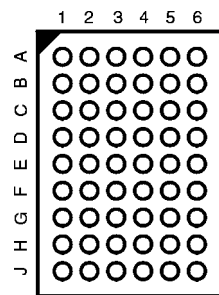


### Connection Diagrams

Pin Assignments for SSOP and TSSOP



Pin Assignment for FBGA



(Top Thru View)

### Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$T/\overline{R}_n$	Transmit/Receive Input
A <sub>0</sub> -A <sub>15</sub>	Side A Inputs/3-STATE Outputs
B <sub>0</sub> -B <sub>15</sub>	Side B Inputs/3-STATE Outputs
NC	No Connect

### FBGA Pin Assignments

	1	2	3	4	5	6
<b>A</b>	B <sub>0</sub>	NC	$T/\overline{R}_1$	$\overline{OE}_1$	NC	A <sub>0</sub>
<b>B</b>	B <sub>2</sub>	B <sub>1</sub>	NC	NC	A <sub>1</sub>	A <sub>2</sub>
<b>C</b>	B <sub>4</sub>	B <sub>3</sub>	V <sub>CC</sub>	V <sub>CC</sub>	A <sub>3</sub>	A <sub>4</sub>
<b>D</b>	B <sub>6</sub>	B <sub>5</sub>	GND	GND	A <sub>5</sub>	A <sub>6</sub>
<b>E</b>	B <sub>8</sub>	B <sub>7</sub>	GND	GND	A <sub>7</sub>	A <sub>8</sub>
<b>F</b>	B <sub>10</sub>	B <sub>9</sub>	GND	GND	A <sub>9</sub>	A <sub>10</sub>
<b>G</b>	B <sub>12</sub>	B <sub>11</sub>	V <sub>CC</sub>	V <sub>CC</sub>	A <sub>11</sub>	A <sub>12</sub>
<b>H</b>	B <sub>14</sub>	B <sub>13</sub>	NC	NC	A <sub>13</sub>	A <sub>14</sub>
<b>J</b>	B <sub>15</sub>	NC	$T/\overline{R}_2$	$\overline{OE}_2$	NC	A <sub>15</sub>

### Truth Tables

Inputs		Outputs
$\overline{OE}_1$	$T/\overline{R}_1$	
L	L	Bus B <sub>0</sub> -B <sub>7</sub> Data to Bus A <sub>0</sub> -A <sub>7</sub>
L	H	Bus A <sub>0</sub> -A <sub>7</sub> Data to Bus B <sub>0</sub> -B <sub>7</sub>
H	X	HIGH-Z State on A <sub>0</sub> -A <sub>7</sub> , B <sub>0</sub> -B <sub>7</sub>

Inputs		Outputs
$\overline{OE}_2$	$T/\overline{R}_2$	
L	L	Bus B <sub>8</sub> -B <sub>15</sub> Data to Bus A <sub>8</sub> -A <sub>15</sub>
L	H	Bus A <sub>8</sub> -A <sub>15</sub> Data to Bus B <sub>8</sub> -B <sub>15</sub>
H	X	HIGH-Z State on A <sub>8</sub> -A <sub>15</sub> , B <sub>8</sub> -B <sub>15</sub>

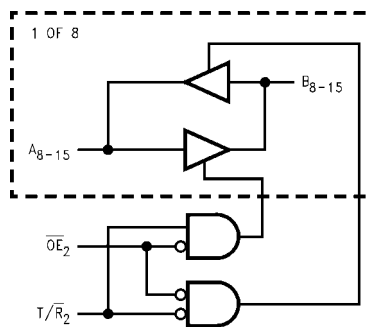
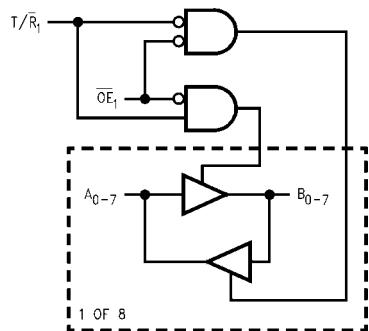
H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance

### Functional Description

The LVT162245 and LVTH162245 contain sixteen non-inverting bidirectional buffers with 3-STATE outputs. The device is byte controlled with each byte functioning identi-

cally, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

### Logic Diagrams



Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 3)				
Symbol	Parameter	Value	Conditions	Units
$V_{CC}$	Supply Voltage	-0.5 to +4.6		V
$V_I$	DC Input Voltage	-0.5 to +7.0		V
$V_O$	Output Voltage	-0.5 to +7.0	Output in 3-STATE	V
		-0.5 to +7.0	Output in HIGH or LOW State (Note 4)	
$I_{IK}$	DC Input Diode Current	-50	$V_I < GND$	mA
$I_{OK}$	DC Output Diode Current	-50	$V_O < GND$	mA
$I_O$	DC Output Current	64	$V_O > V_{CC}$ Output at HIGH State	mA
		128	$V_O > V_{CC}$ Output at LOW State	
$I_{CC}$	DC Supply Current per Supply Pin	$\pm 64$		mA
$I_{GND}$	DC Ground Current per Ground Pin	$\pm 128$		mA
$T_{STG}$	Storage Temperature	-65 to +150		$^{\circ}C$

### Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
$V_{CC}$	Supply Voltage	2.7	3.6	V
$V_I$	Input Voltage	0	5.5	V
$I_{OH}$	HIGH-Level Output Current	B Port	-32	mA
		A Port	-12	
$I_{OL}$	LOW-Level Output Current	B Port	64	mA
		A Port	12	
$T_A$	Free Air Operating Temperature	-40	+85	$^{\circ}C$
$\Delta t/\Delta V$	Input Edge Rate, $V_{IN} = 0.8V-2.0V$ , $V_{CC} = 3.0V$	0	10	ns/V

**Note 3:** Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

**Note 4:**  $I_O$  Absolute Maximum Rating must be observed.

### DC Electrical Characteristics

Symbol	Parameter	$V_{CC}$ (V)	$T_A = -40^{\circ}C$ to $+85^{\circ}C$		Units	Conditions	
			Min	Max			
$V_{IK}$	Input Clamp Diode Voltage	2.7		-1.2	V	$I_I = -18$ mA	
$V_{IH}$	Input HIGH Voltage	2.7-3.6	2.0		V	$V_O \leq 0.1V$ or	
$V_{IL}$	Input LOW Voltage	2.7-3.6		0.8	V	$V_O \geq V_{CC} - 0.1V$	
$V_{OH}$	Output HIGH Voltage	A Port	3.0	2.0	V	$I_{OH} = -12$ mA	
			2.7-3.6	$V_{CC}-0.2$	V	$I_{OH} = -100$ $\mu A$	
		B Port	2.7	2.4	V	$I_{OH} = -8$ mA	
			3.0	2.0	V	$I_{OH} = -32$ mA	
$V_{OL}$	Output LOW Voltage	A Port	3.0	0.8	V	$I_{OL} = 12$ mA	
			2.7	0.2	V	$I_{OL} = 100$ $\mu A$	
		B Port	2.7	0.5	V	$I_{OL} = 24$ mA	
			3.0	0.4		$I_{OL} = 16$ mA	
			3.0	0.5		$I_{OL} = 32$ mA	
			3.0	0.55		$I_{OL} = 64$ mA	
$I_{I(HOLD)}$ (Note 5)	Bushold Input Minimum Drive	3.0	75		$\mu A$	$V_I = 0.8V$	
			-75			$V_I = 2.0V$	
$I_{I(OD)}$ (Note 5)	Bushold Input Over-Drive Current to Change State	3.0	500		$\mu A$	(Note 6)	
			-500			(Note 7)	
$I_I$	Input Current	3.6		10	$\mu A$	$V_I = 5.5V$	
		Control Pins	3.6			$\pm 1$	$V_I = 0V$ or $V_{CC}$
			Data Pins	3.6			-5
$I_{OFF}$	Power Off Leakage Current	0		$\pm 100$	$\mu A$	$0V \leq V_I$ or $V_O \leq 5.5V$	

**DC Electrical Characteristics** (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C		Units	Conditions
			Min	Max		
I <sub>PU/PD</sub>	Power Up/Down 3-STATE Current	0–1.5V		±100	μA	V <sub>O</sub> = 0.5V to 3.0V V <sub>I</sub> = GND to V <sub>CC</sub>
I <sub>OZL</sub>	3-STATE Output Leakage Current	3.6		-5	μA	V <sub>O</sub> = 0.5V
I <sub>OZL</sub> (Note 5)	3-STATE Output Leakage Current	3.6		-5	μA	V <sub>O</sub> = 0.0V
I <sub>OZH</sub>	3-STATE Output Leakage Current	3.6		5	μA	V <sub>O</sub> = 3.0V
I <sub>OZH</sub> (Note 5)	3-STATE Output Leakage Current	3.6		5	μA	V <sub>O</sub> = 3.6V
I <sub>OZH</sub> <sup>+</sup>	3-STATE Output Leakage Current	3.6		10	μA	V <sub>CC</sub> < V <sub>O</sub> ≤ 5.5V
I <sub>CCH</sub>	Power Supply Current	3.6		0.19	mA	Outputs HIGH
I <sub>CCL</sub>	Power Supply Current	3.6		5	mA	Outputs LOW
I <sub>CCZ</sub>	Power Supply Current	3.6		0.19	mA	Outputs Disabled
I <sub>CCZ</sub> <sup>+</sup>	Power Supply Current	3.6		0.19	mA	V <sub>CC</sub> ≤ V <sub>O</sub> ≤ 5.5V, Outputs Disabled
ΔI <sub>CC</sub>	Increase in Power Supply Current (Note 8)	3.6		0.2	mA	One Input at V <sub>CC</sub> - 0.6V Other Inputs at V <sub>CC</sub> or GND

**Note 5:** Applies to Bushold versions only (74LVTH162245).

**Note 6:** An external driver must source at least the specified current to switch from LOW-to-HIGH.

**Note 7:** An external driver must sink at least the specified current to switch from HIGH-to-LOW.

**Note 8:** This is the increase in supply current for each input that is at the specified voltage level rather than V<sub>CC</sub> or GND.

**Dynamic Switching Characteristics** (Note 9)

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			Units	Conditions C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500Ω
			Min	Typ	Max		
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3		0.8		V	(Note 10)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3		-0.8		V	(Note 10)

**Note 9:** Characterized in SSOP package. Guaranteed parameter, but not tested.

**Note 10:** Max number of outputs defined as (n), n-1 data inputs are driven 0V to 3V. Output under test held LOW.

## AC Electrical Characteristics

Symbol	Parameter	T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500Ω				Units
		V <sub>CC</sub> = 3.3V ± 0.3V		V <sub>CC</sub> = 2.7V		
		Min	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay Data to A Port Output	1.0	4.0	1.0	4.6	ns
t <sub>PHL</sub>		1.0	3.7	1.0	4.1	
t <sub>PLH</sub>	Propagation Delay Data to B Port Output	1.0	3.5	1.0	3.9	ns
t <sub>PHL</sub>		1.0	3.5	1.0	3.9	
t <sub>PZH</sub>	Output Enable Time for A Port Output	1.0	5.3	1.0	6.3	ns
t <sub>PZL</sub>		1.0	5.6	1.0	7.2	
t <sub>PZH</sub>	Output Enable Time for B Port Output	1.0	4.6	1.0	5.4	ns
t <sub>PZL</sub>		1.0	5.3	1.0	6.9	
t <sub>PHZ</sub>	Output Disable Time for A Port Output	1.5	5.6	1.5	6.3	ns
t <sub>PLZ</sub>		1.5	5.5	1.5	5.5	
t <sub>PHZ</sub>	Output Disable Time for B Port Output	1.5	5.4	1.5	6.1	ns
t <sub>PLZ</sub>		1.5	5.1	1.5	5.4	
t <sub>OSSL</sub>	A Port Output to Output Skew (Note 11)		1.0		1.0	ns
t <sub>OSLH</sub>						
t <sub>OSSL</sub>	B Port Output to Output Skew (Note 11)		1.0		1.0	ns
t <sub>OSLH</sub>						

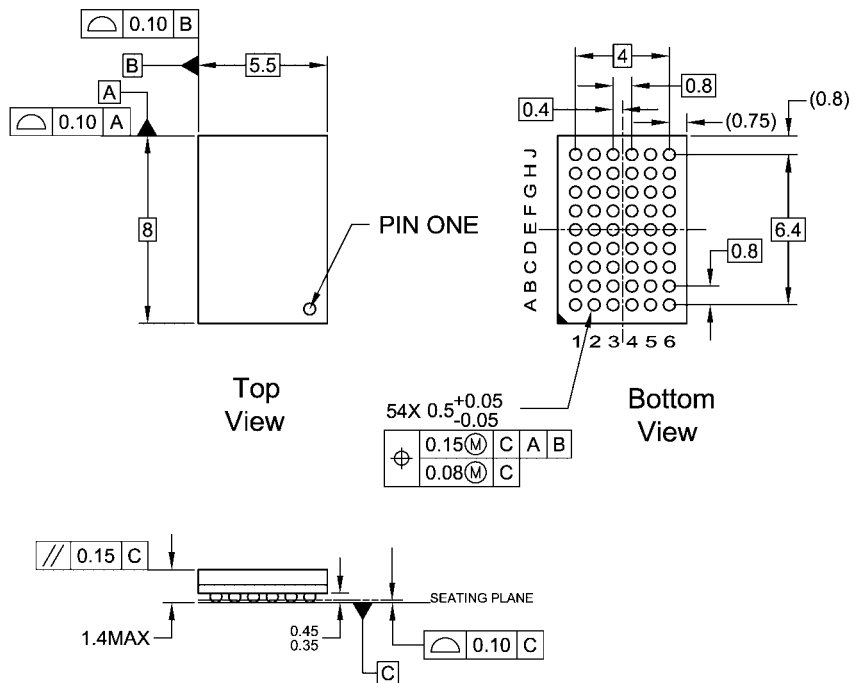
**Note 11:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSSL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>).

## Capacitance (Note 12)

Symbol	Parameter	Conditions	Typical	Units
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = 0V, V <sub>I</sub> = 0V or V <sub>CC</sub>	4	pF
C <sub>I/O</sub>	Input/Output Capacitance	V <sub>CC</sub> = 3.0V, V <sub>O</sub> = 0V or V <sub>CC</sub>	8	pF

**Note 12:** Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

**Physical Dimensions** inches (millimeters) unless otherwise noted



**NOTES:**

- A. THIS PACKAGE CONFORMS TO JEDEC M0-205
- B. ALL DIMENSIONS IN MILLIMETERS
- C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)  
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
- D. DRAWING CONFORMS TO ASME Y14.5M-1994

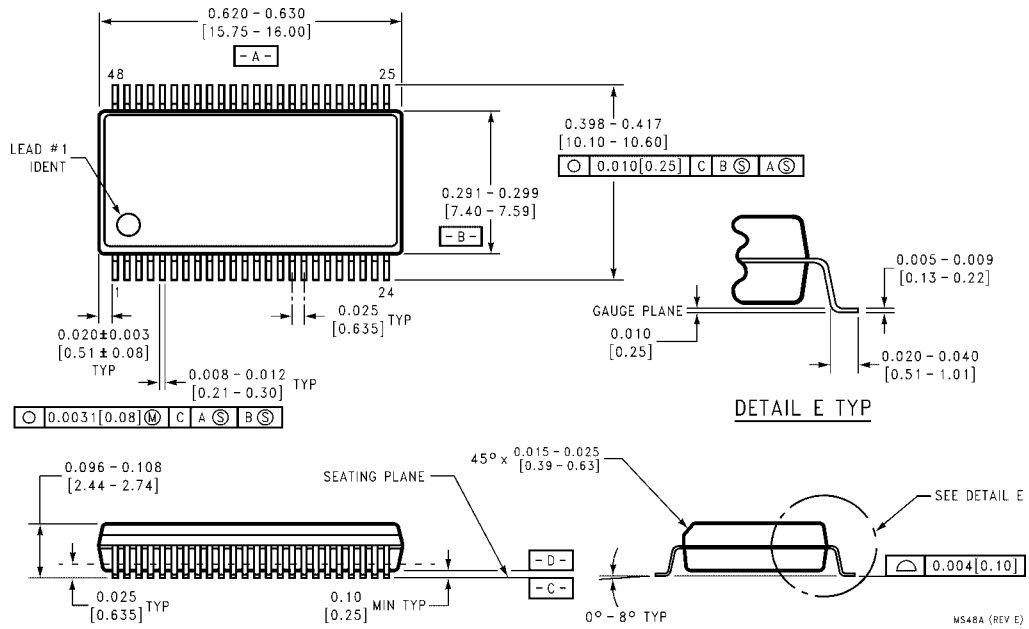
BGA54ArevD

**54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC M0-205, 5.5mm Wide  
Package Number BGA54A**



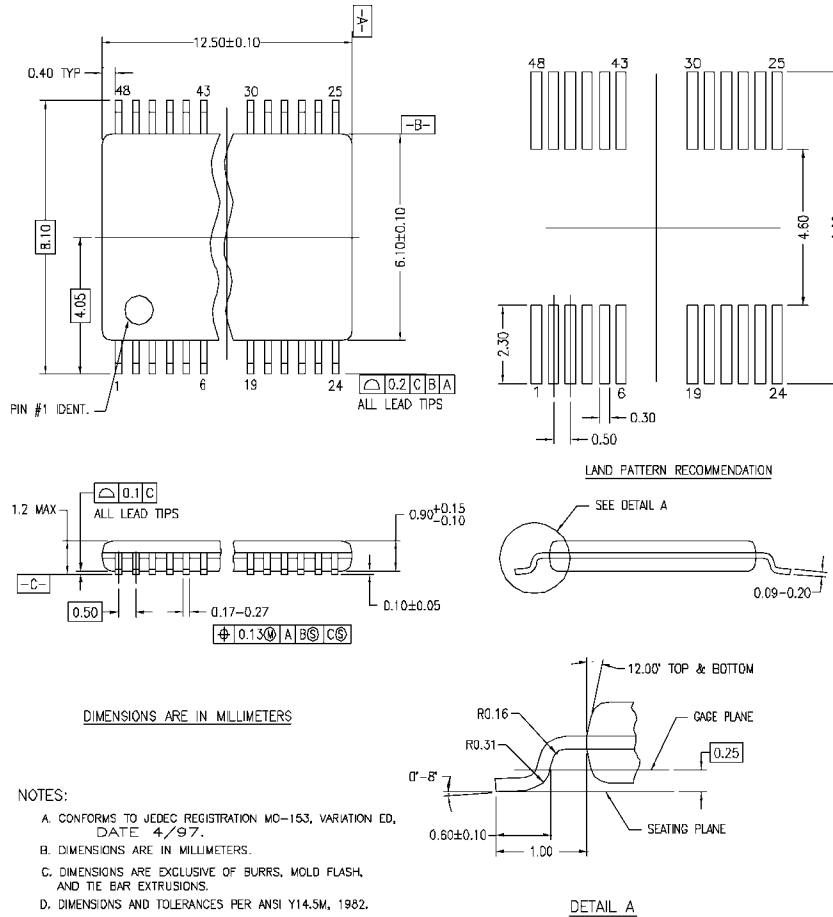
74LVT162245 • 74LVTH162245

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide  
Package Number MS48A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



- NOTES:
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION ED, DATE 4/97.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
  - D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48REVC

**48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD48**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)