Product/Process Change Notice - PCN 15_0178 Rev. -

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This notice is to inform you of a change that will be made to certain ADI products (see Appendix A) that you may have purchased in the last 2 years. **Any inquiries or requests with this PCN (additional data or samples) must be sent to ADI within 30 days of publication date.** ADI contact information is listed below.

PCN Title: ADV7619 Settings and Related Data Sheet Specification updates

Publication Date: 22-Sep-2015

Effectivity Date: 22-Sep-2015 *(the earliest date that a customer could expect to receive changed material)*

Revision Description:

Initial Release

Description Of Change

1. Configuration Setting Change:
The ADV7619 recommended setting scripts for video resolutions with a pixel clock of over 148.5MHz have been updated to incorporate the following writes:

; Added write 98 00 19 ; Set VID_STD
; Added write 98 01 05 ; Prim_Mode =101b HDMI-Comp
; Added write 98 DD 00 ; Default value
; Added write 98 E7 04 ; ADI Required Write

2. Datasheet Addition:

An additional clock duty cycle specification for video resolutions with a pixel clock of over 148.5MHz was added to the ADV7619 datasheet.

Specification: LLC Mark-Space Ratio
Time Descriptor: t9:t10
Description: Pixel clock > 148.5MHz
Minimum Spec: 40:60 % duty cycle
Maximum Spec: 60:40 % duty cycle

Reason For Change

In conjunction with the silicon, the ADV7619 recommended I2C settings are a critical element of an overall stable solution. This change is being made to improve the timing-related stability of the I2C settings at certain combinations of material, voltage and temperature.

The modification changes the clock path employed for video resolutions with a pixel clock of over 148.5MHz. It has been confirmed that the new clock path resolves the timing-related stability issues observed with the old clock path at certain combinations of material, voltage and temperature. The new clock path has a slightly higher level of clock duty cycle distortion, please see the above change description for the clock duty cycle specification.

Impact of the change (positive or negative) on fit, form, function & reliability

The following are the impacts of this change:

1. Application Software Change
Customers must add the new configuration settings into their application software to guarantee the most robust performance of ADV7619

2. Duty Cycle Ratio
Customers must analyse their application hardware to ensure that their setup and hold timing margin is still sufficient given the increased clock duty cycle.

Product Identification *(this section will describe how to identify the changed material)*

This change is effective from date code 1543

Summary of Supporting Information

The changes described above are reflected in the ADV7619 Rev. D data sheet.

Supporting Documents None

For questions on this PCN, please send an email to the regional contacts below or contact your local ADI sales representatives.					
Americas:	PCN_Americas@analog.com	**Europe:**	PCN_Europe@analog.com	**Japan:**	PCN_Japan@analog.com
				Rest of Asia:	PCN_ROA@analog.com

Appendix A - Affected ADI Models				
Added Parts On This Revision - Product Family / Model Number (2)				
ADV7619 / ADV7619KSVZ	ADV7619 / ADV7619KSVZ-P			

Appendix B - Revision History			
Rev	**Publish Date**	**Effectivity Date**	**Rev Description**
Rev. -	22-Sep-2015	22-Sep-2015	Initial Release