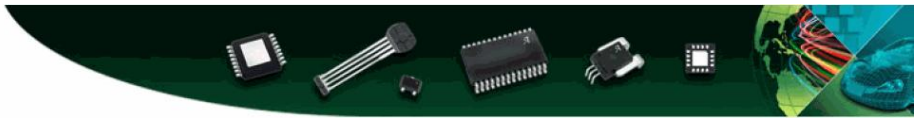


PCN Number: DEC2015
Chgnot.doc rev 13 1/14

Product/Process Change Notification (PCN)

Customer: Newark **Date: 12/18/15**

Customer Part # and/or Lot# affected: A4942GESTR-T & A4988SETTR-T

Originator: J.Hurley **Phone: 508-854-8491**

Duration of Change: Permanent [X] Temporary (explain) [ ]

Summary description of change: Part Change: [ ] Process Change: [X] Other: [ ]

1. The listed device will change wafer fab from Polar Semiconductor LLC (PSL), Bloomington, MN, USA, utilizing 8" ABCD5 technology to the existing wafer fab at United Microelectronics Corporation (UMC), Hsinshu, Taiwan utilizing 8" ABCD5 technology.

2. The listed device is assembled at Carsem Suzhou, China. Allegro MicroSystems will introduce UTAC Thai Limited, Chachoengsao, Thailand as a second assembly location.

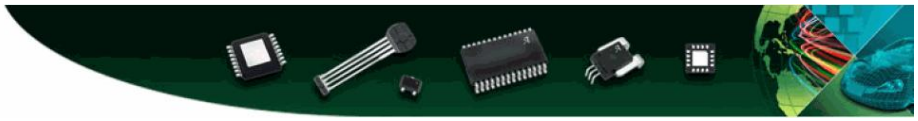
3. The listed device will change from final test at Allegro MicroSystems, Inc. Manila, Philippines (AMPI) to final test at Allegro MicroSystems Thailand Company, Ltd. located in Saraburi, Thailand (AMTC).

What is the part or process changing from (provide details)?

1. The device listed is manufactured at Polar Semiconductor LLC (PSL), Bloomington, MN, USA utilizing ABCD5 8" technology.

2. The device listed is assembled at Carsem Suzhou, China.

3. Allegro currently performs final test at Allegro MicroSystems, Inc. Manila, Philippines (AMPI).



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What is the part or process changing to (describe the anticipated impact of this change on form, fit and/or function)?

1. The listed device (s) will be manufactured at United Microelectronics Corporation (UMC), Hsinshu, Taiwan utilizing ABCD5 8" technology.

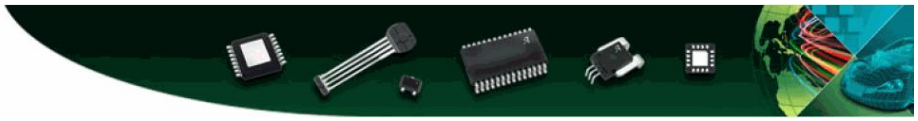
2. Allegro MicroSystems will add assembly at UTAC Thai Limited, Chachoengsao, Thailand This assembly location is already qualified for this package as a second assembly location.

3. Allegro will perform final test at Allegro MicroSystems Thailand Company, Ltd. located in Saraburi, Thailand, a wholly-owned integrated circuit test facility. The same make and model test equipment will be utilized and test site transfer buy off data will be on file for each device before production begins.

Note: Validation of equivalence within a specific application is at the discretion of the Customer

Is a PPAP update required? Yes [ ] No [X]

Is reliability testing required? Yes [X] No [ ]
(If Yes, refer to attached plan)
See UMC and UTAC QAFs below



Scope:
To qualify the UMC ABCD5 Fab process technology for commercial IC's.

Summary: The data below is the stresses performed for the UMC ABCD5 Fab process qualification. The UMC ABCD5 process qualification is considered to be passing all environmental stress evaluations per the Allegro MicroSystems, LLC. 900019 specification.

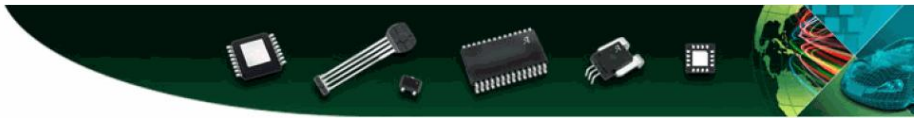
The UMC – ABCD5 Fab process technology meets and exceeds the qualification requirements required per JESD47 Stress Test Qualification for Integrated circuits.

Reference Qualification tracking numbers: 2982, 3030, and 3058

Detailed Data: *UMC –ABCD5*
Devices tested: *4950, 4942 and 4984*

Tests Summary

Stress	Test Method	Test Condition	Sample Size	# of Lots	Results
Preconditioning	J-STD-020	85°C/60% RH, (168 hrs)	231	3	0 Rejects
HAST	JESD22-A110	130°C/85% RH, (96 hrs)	77	2	0 Rejects
THB	JESD22-A101	85°C/85% RH, (1000 hrs)	77	3	0 Rejects
AC	JESD22-A102	121°C, 100% RH, (96 hrs)	77	3	0 Rejects
TC	JESD22-A104	-65°C to +150°C, (500, 1000 cycles)	77	2	0 Rejects
TC	JESD22-A104	-65°C to +175°C, (500, 1000 cycles)	77	1	0 Rejects
HTSL	JESD22-A103	150°C, (1000 hrs)	77	2	0 Rejects
HTOL	JESD22-A108	125°C, (1000 hrs)	77	3	0 Rejects
ELFR	AEC-Q100-008	125°C, (48 hrs)	800	3	0 Rejects
Wire Bond Pull	Mil-STD-883	Method 2011	5	3	Cpk > 1.67



Scope:
To qualify the UTAC assembly site using the QFN package for commercial IC's.

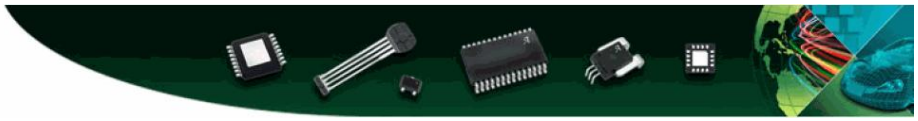
Summary:
This qualification is considered to be passing all environmental stress evaluations per the Allegro MicroSystems, LLC, 900019 Qualification specification for UTAC QFN 3x3, 4x4, 5x5 package family. Qualifications were performed using the 16, 20, 24, 28 and 32 lead QFN packages.

The QFN- Copper-Wire package manufactured at UTAC meets and exceeds the qualification requirements required per JESD47 Stress Test Qualification for Integrated circuits.

Reference Qualification tracking numbers: 2709, 2724, 2792, 2793, 2794, 2795, 2796

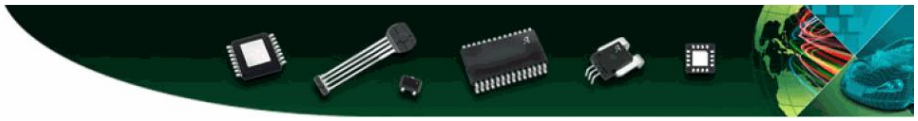
Detailed Data: *UTAC QFN Copper-Wire*

Package:	QFN, (square leadless exposed thermal pad) , 0.50 mm pitch
Assembly Location:	UTAC
Mold Compound:	G700LTD
Lead Finish:	100% Tin
Die Attach Material:	8600
Bond Wire:	Copper (CuPd)



Tests Summary

Stress	Test Method	Test Condition	Sample Size	Results	# of Lots
Preconditioning	J-STD-020 /JESD22-A113	85°C/60% RH, 168 hrs Peak Temp: 260C	(HAST, THB AC, TC samples)	0 rejects	7
HAST	JESD22-A110	130°C/85% RH 96, 192 hrs.	77	0 rejects	7
THB	JESD22-A101	85°C/85% RH 1000 hrs.	77	0 rejects	7
AC	JESD22-A102	121°C, 100% RH 96, 192 hrs.	77	0 rejects	7
TC	JESD22-A104	-65°C to +150°C 500, 1000 cycles	77	0 rejects	7
HTSL	JESD22-A103	150°C, 1000 hrs	77	0 rejects	4
Wire Bond Pull	Mil-STD-2011	Method 2011	5	Cpk > 1.67	7
HTOL	JESD22-A108	150°C, 1000 hrs	77	0 rejects	5
HTOL	JESD22-A108	125°C, 1000 hrs	77	0 rejects	2
ELFR	JESD22-A104	150°C, 48 hrs	800	0 rejects	5
ELFR	JESD22-A104	125°C, 48 hrs	800	0 rejects	2
Solderability	JESD22-B102		15	0 rejects > 95% Lead Coverage	7
Wire Bond Shear			30	Cpk > 1.67	7
Wire Pull Strength			30	Cpk > 1.67	7
Die Shear			30	Cpk > 1.67	7
Wire Sweep			10	Cpk > 1.67	7
Physical Dimensions			5	Cpk > 1.67	7



Expected completion date for internal qualification: Complete

Expected PPAP availability date: N/A

Target implementation date: March 2016

Estimated date of first shipment: April 2016

Expected sample availability date: Available Upon Request

Customer Approval Required:	**Yes**	☐	**Date Required:**
	No	X	**Notification Only**

Please note: It is our intention to inform our customer of changes as early as possible. Under Allegro's procedure for product/process change notification, Allegro strives, based on its technical judgment, to provide notification of significant changes that may affect form, fit or function. However, as Allegro cannot ensure evaluation of product/process changes for each and every application; the customer retains responsibility to validate the impact of a change on its application suitability. If samples are needed for validation of a change, requests may be made via the contact information provided herein. Please contact your Account Manager or local Sales contact for any questions. We would kindly request your consideration so we can meet our target date for implementation. Unless both parties agree to extend the implementation date, this change will be implemented as scheduled.

Customer comments/Conditions of Acceptance:

Approved by: Date: Title:

cc: Allegro Sales/Marketing/Quality