CHANGE NOTIFICATION

Linear Technology Corporation
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(408) 432-1900

April 14, 2015

Dear Sir/Madam: PCN# 041415

Subject: Notification of Change to LT3955 Datasheet

Please be advised that Linear Technology Corporation has made a minor change to the LT3955 product datasheet to improve manufacturing yield and better center the parametric distribution within specification range. The changes are shown on the attached page of the marked up datasheet. There was no change in form, fit, function, quality or reliability of the product. The product shipped after June 14, 2015 will be tested to the new limits.

Should you have any further questions or concerns please contact your local Linear Technology Sales person or you may contact me at 408-432-1900 ext. 2077, or by e-mail at JASON.HU@LINEAR.COM. If I do not hear from you by June 14, 2015, we will consider this change to be approved by your company.

Sincerely,

Jason Hu
Quality Assurance Engineer

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 24V, EN/UVLO = 24V, CTRL = 2V, PWM = 5V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SYNC Input High			1.5			V
Linear Regulator						
$INTV_{CC}$ Regulation Voltage	10V ≤ V_{IN} ≤ 60V	●	7.60	7.85	8.05	V
$INTV_{CC}$ Maximum Operating Voltage			8.1			V
$INTV_{CC}$ Minimum Operating Voltage					4.5	V
Dropout (V_{IN} – $INTV_{CC}$)	I_{INTVCC} = –10mA, V_{IN} = 7V			390		mV
$INTV_{CC}$ Undervoltage Lockout		●	3.9	4.1	4.4	V
$INTV_{CC}$ Current Limit	8V ≤ V_{IN} ≤ 60V, $INTV_{CC}$ = 6V		30	36	42	mA
$INTV_{CC}$ Current in Shutdown	EN/UVLO = 0V, $INTV_{CC}$ = 8V			8	13	µA
Logic Inputs/Outputs						
EN/UVLO Threshold Voltage Falling		●	1.180	1.220	1.260	V
EN/UVLO Rising Hysteresis				40		mV
EN/UVLO Input Low Voltage	I_{VIN} Drops Below 1µA				0.4	V
EN/UVLO Pin Bias Current Low	EN/UVLO = 1.15V		1.7	2.2	2.7	µA
EN/UVLO Pin Bias Current High	EN/UVLO = 1.33V			10	100	nA
$\overline{VMODE}$ Output Low	$I_{\overline{VMODE}}$ = 1mA				200	mV
$\overline{VMODE}$ Pin Leakage	FB = 0V, $\overline{VMODE}$ = 12V			0.1	5	µA
PWM Pin Signal Generator						
PWM Falling Threshold		●	0.78	0.83	0.88	V
PWM Threshold Hysteresis (V_{PWMHYS})	$I_{DIM/SS}$ = 0µA		0.35	0.47	0.6	V
PWM Pull-Up Current (I_{PWMUP})	PWM = 0.7V, $I_{DIM/SS}$ = 0µA		6	7.5	9	µA
PWM Pull-Down Current (I_{PWMDN})	PWM = 1.5V, $I_{DIM/SS}$ = 0µA		68	88	110	µA
PWM Fault-Mode Pull-Down Current	$INTV_{CC}$ = 3.6V			1.5		mA
PWMOUT Duty Ratio for PWM Signal Generator (Note 5)	$I_{DIM/SS}$ = –6.5µA $I_{DIM/SS}$ = 0µA $I_{DIM/SS}$ = 21.5µA $I_{DIM/SS}$ = 52µA		3.1 ~~6.8~~ 6.2 40 95	4.1 7.9 48 96.5	5.2 9.2 56 98	% % % %
PWMOUT Signal Generator Frequency	PWM = 47nF to GND, $I_{DIM/SS}$ = 0µA		170	300	390	Hz
PWMOUT Driver						
PWMOUT Driver Output Rise Time (t_r)	C_L = 560pF			35		ns
PWMOUT Driver Output Fall Time (t_f)	C_L = 560pF			35		ns
PWMOUT Output Low (V_{OL})	PWM = 0V				0.05	V
PWMOUT Output High (V_{OH})			$INTV_{CC}$ – 0.05			V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Do not apply a positive or negative voltage or current source to PWMOUT pin, otherwise permanent damage may occur.

Note 3: The LT3955E is guaranteed to meet performance specifications from the 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3955I is guaranteed over the full –40°C to 125°C operating junction temperature range.

Note 4: The LT3955 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature when overtemperature protection is active. Continuous operation above the specified maximum junction temperature may impair device reliability.

Note 5: PWMOUT Duty Ratio is calculated:

Duty = $I_{PWMUP}/(I_{PWMUP} + I_{PWMDN})$