CHANGE NOTIFICATION

Linear Technology Corporation
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August 11, 2015

Dear Sir/Madam: PCN# 081115

Subject: Notification of Change to LTC3129, LTC3129-1 Datasheet

Please be advised that Linear Technology Corporation has made a minor change to the LTC3129 and LTC3129-1 product datasheets to facilitate improvement in our manufacturing yield. The changes are shown on the attached pages of the marked up datasheet. There was no change made to the die. The product shipped after October 12, 2015 will be tested to the new limits.

Should you have any further questions or concerns please contact your local Linear Technology Sales person or you may contact me at 408-432-1900 ext. 2077, or by e-mail at jason.hu@linear.com. If I do not hear from you by October 12, 2015, we will consider this change to be approved by your company.

Sincerely,

Jason Hu
Quality Assurance Engineer

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). Unless otherwise noted, V_{IN} = 12V, V_{OUT} = 5V.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Start-Up Voltage		●		2.25	2.42	V
Input Voltage Range	V_{CC} > 2.42V (Back-Driven)	●	1.92		15	V
V_{IN} UVLO Threshold (Rising)	V_{CC} > 2.42V (Back-Driven)	●	1.8	1.9	2.0	V
V_{IN} UVLO Hysteresis		●	80	100	130	mV
Output Voltage Adjust Range		●	1.4		15.75	V
Feedback Voltage		●	1.151	1.175	1.199	V
Feedback Input Current	FB = 1.25V			0.1	10	nA
Quiescent Current (V_{IN}) – Shutdown	RUN = 0V, Including Switch Leakage			10	100	nA
Quiescent Current (V_{IN}) UVLO	Either V_{IN} or V_{CC} Below Their UVLO Threshold, or RUN Below the Threshold to Enable Switching			1.9	3	µA
Quiescent Current – Burst Mode Operation	Measured on V_{IN}, FB > 1.25V PWM = 0V, RUN = V_{IN}			1.3	2.0	µA
N-Channel Switch Leakage on V_{IN} and V_{OUT}	SW1 = 0V, V_{IN} = 15V SW2 = 0V, V_{OUT} = 15V RUN = 0V			10	50	nA
N-Channel Switch On-Resistance	V_{CC} = 4V			0.75		Ω
Inductor Average Current Limit	V_{OUT} > UV Threshold (Note 4) V_{OUT} < UV Threshold (Note 4)	● ●	220 80	275 130	350 200	mA mA
Inductor Peak Current Limit	(Note 4)	●	400	500	680	mA
Maximum Boost Duty Cycle	FB = 1.10V. Percentage of Period SW2 is Low in Boost Mode (Note 7)	●	85	89	95	%
Minimum Duty Cycle	FB = 1.25V. Percentage of Period SW1 is High in Buck Mode (Note 7)	●			0	%
Switching Frequency	PWM = V_{CC}	●	1.0	1.2	1.4	MHz
SW1 and SW2 Minimum Low Time	(Note 3)			90		ns
MPPC Voltage		●	1.12	1.175	1.22	V
MPPC Input Current	MPPC = 5V			1	10	nA
RUN Threshold to Enable V_{CC}		●	0.5	0.9	1.15	V
RUN Threshold to Enable Switching (Rising)	V_{CC} > 2.4V	●	1.16	1.22	1.28	V
RUN (Switching) Threshold Hysteresis			50	80	120	mV
RUN Input Current	RUN = 15V			1	10	nA
PWM Input High		●	1.6			V
PWM Input Low		●			0.5	V
PWM Input Current	PWM = 5V			0.1	1	µA
Soft-Start Time				3		ms
V_{CC} Voltage	V_{IN} > 4.85V	●	3.4	4.1	4.7	V
V_{CC} Dropout Voltage (V_{IN} – V_{CC})	V_{IN} = 3.0V, Switching V_{IN} = 2.0V (V_{CC} in UVLO)			35 0	60 2	mV mV
V_{CC} UVLO Threshold (Rising)		●	2.1	2.25	2.42	V
V_{CC} UVLO Hysteresis				60		mV
V_{CC} Current Limit	V_{CC} = 0V	●	4	20	~~40~~ 60	mA
V_{CC} Back-Drive Voltage (Maximum)		●			5.5	V
V_{CC} Input Current (Back-Driven)	V_{CC} = 5.5V (Switching)			2	4	mA
V_{CC} Leakage to V_{IN} if V_{CC} > V_{IN}	V_{CC} = 5.5V, V_{IN} = 1.8V, Measured on V_{IN}			–27		µA
V_{OUT} UV Threshold (Rising)		●	0.95	1.15	1.35	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A = 25°C$ (Note 2). Unless otherwise noted, $V_{IN} = 12V$, $V_{OUT} = 5V$.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC} UVLO Threshold (Rising)		●	2.1	2.25	2.42	V
V_{CC} UVLO Hysteresis				60		mV
V_{CC} Current Limit	$V_{CC} = 0V$	●	4	20	~~40~~ 60	mA
V_{CC} Back-Drive Voltage (Maximum)		●			5.5	V
V_{CC} Input Current (Back-Driven)	$V_{CC} = 5.5V$ (Switching)			2	4	mA
V_{CC} Leakage to V_{IN} if $V_{CC}>V_{IN}$	$V_{CC} = 5.5V$, $V_{IN} = 1.8V$, Measured on V_{IN}			–27		µA
V_{OUT} UV Threshold (Rising)		●	0.95	1.15	1.35	V
V_{OUT} UV Hysteresis				150		mV
V_{OUT} Current – Shutdown	RUN = 0V, $V_{OUT} = 15V$ Including Switch Leakage			10	100	nA
V_{OUT} Current – Sleep	PWM = 0V, $V_{OUT} \geq V_{REG}$			$V_{OUT}/27$		µA
V_{OUT} Current – Active	PWM = V_{CC}, $V_{OUT} = 15V$ (Note 4)			5	9	µA
PGOOD Threshold, Falling	Referenced to Programmed V_{OUT} Voltage		–5.5	–7.5	–10	%
PGOOD Hysteresis	Referenced to Programmed V_{OUT} Voltage			2.5		%
PGOOD Voltage Low	$I_{SINK} = 1mA$			250	300	mV
PGOOD Leakage	PGOOD = 15V			1	50	nA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3129-1 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3129E-1 is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3129I-1 is guaranteed over the full –40°C to 125°C operating junction temperature range. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA}),$$

where θ_{JA} (in °C/W) is the package thermal impedance.

Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated thermal package thermal resistance and other environmental factors.

Note 3: Specification is guaranteed by design and not 100% tested in production.

Note 4: Current measurements are made when the output is not switching.

Note 5: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

Note 6: Failure to solder the exposed backside of the package to the PC board ground plane will result in a much higher thermal resistance.

Note 7: Switch timing measurements are made in an open-loop test configuration. Timing in the application may vary somewhat from these values due to differences in the switch pin voltage during non-overlap durations when switch pin voltage is influenced by the magnitude and duration of the inductor current.

Note 8: Voltage transients on the switch pin(s) beyond the DC limits specified in the Absolute Maximum Ratings are non-disruptive to normal operation when using good layout practices as described elsewhere in the data sheet and Application Notes and as seen on the product demo board.