NSS60200L

60 V, 4.0 A, Low $V_{CE(sat)}$ PNP Transistor

ON Semiconductor's e^2PowerEdge family of low $V_{CE(sat)}$ transistors are miniature surface mount devices featuring ultra low saturation voltage ($V_{CE(sat)}$) and high current gain capability. These are designed for use in low voltage, high speed switching applications where affordable efficient energy control is important.

Typical applications are DC−DC converters and power management in portable and battery powered products such as cellular and cordless phones, PDAs, computers, printers, digital cameras and MP3 players. Other applications are low voltage motor controls in mass storage products such as disc drives and tape drives. In the automotive industry they can be used in air bag deployment and in the instrument cluster. The high current gain allows e^2PowerEdge devices to be driven directly from PMU's control outputs, and the Linear Gain (Beta) makes them ideal components in analog amplifiers.

Features

- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	V_{CEO}	−60	Vdc
Collector-Base Voltage	V_{CBO}	−80	Vdc
Emitter-Base Voltage	V_{EBO}	−7.0	Vdc
Collector Current − Continuous	I_C	−2.0	A
Collector Current − Peak	I_{CM}	−4.0	A

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D (Note 1)	460 3.7	mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$ (Note 1)	270	°C/W
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D (Note 2)	540 4.3	mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$ (Note 2)	230	°C/W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. FR−4 @ 100 mm^2, 1 oz. copper traces.
2. FR−4 @ 500 mm^2, 1 oz. copper traces.

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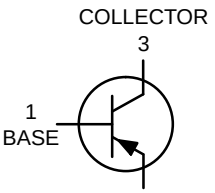
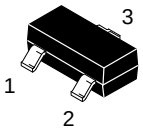
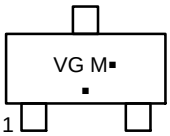
−60 VOLTS, 4.0 AMPS PNP LOW $V_{CE(sat)}$ TRANSISTOR EQUIVALENT $R_{DS(on)}$ 80 mΩ





SOT−23 (TO−236)
CASE 318
STYLE 6

MARKING DIAGRAM



VG = Specific Device Code
M = Date Code*
▪ = Pb−Free Package
(Note: Microdot may be in either location)
*Date Code orientation and/or overbar may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
NSS60200LT1G	SOT−23 (Pb−Free)	3000/Tape & Reel
NSV60200LT1G	SOT−23 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Breakdown Voltage (I_C = −10 mAdc, I_B = 0)	$V_{(BR)CEO}$	−60	–	–	Vdc
Collector−Base Breakdown Voltage (I_C = −0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	−80	–	–	Vdc
Emitter−Base Breakdown Voltage (I_E = −0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	−7.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = −60 Vdc, I_E = 0)	I_{CBO}	–	–	−0.1	μAdc
Emitter Cutoff Current (V_{EB} = −6.0 Vdc)	I_{EBO}	–	–	−0.1	μAdc
ON CHARACTERISTICS					
DC Current Gain (Note 3) (I_C = −10 mA, V_{CE} = −2.0 V) (I_C = −500 mA, V_{CE} = −2.0 V) (I_C = −1.0 A, V_{CE} = −2.0 V) (I_C = −2.0 A, V_{CE} = −2.0 V)	h_{FE}	 150 150 100 100	 – 300 – –	 – – – –	
Collector−Emitter Saturation Voltage (Note 3) (I_C = −0.1 A, I_B = −0.010 A) (I_C = −1.0 A, I_B = −0.100 A) (I_C = −1.0 A, I_B = −0.010 A) (I_C = −2.0 A, I_B = −0.200 A)	$V_{CE(sat)}$	 – – – –	 −0.017 −0.095 −0.180 −0.170	 −0.030 −0.120 −0.270 −0.220	V
Base−Emitter Saturation Voltage (Note 3) (I_C = −1.0 A, I_B = −0.010 A)	$V_{BE(sat)}$	–	–	−0.900	V
Base−Emitter Turn−on Voltage (Note 3) (I_C = −1.0 A, V_{CE} = −2.0 V)	$V_{BE(on)}$	–	–	−0.850	V
Cutoff Frequency (I_C = −100 mA, V_{CE} = −5.0 V, f = 100 MHz)	f_T	100	–	–	MHz
Input Capacitance (V_{EB} = 0.5 V, f = 1.0 MHz)	Cibo	–	–	325	pF
Output Capacitance (V_{CB} = 3.0 V, f = 1.0 MHz)	Cobo	–	–	62	pF
SWITCHING CHARACTERISTICS					
Delay (V_{CC} = −30 V, I_C = 750 mA, I_{B1} = 15 mA)	t_d	–	–	60	ns
Rise (V_{CC} = −30 V, I_C = 750 mA, I_{B1} = 15 mA)	t_r	–	–	120	ns
Storage (V_{CC} = −30 V, I_C = 750 mA, I_{B1} = 15 mA)	t_s	–	–	400	ns
Fall (V_{CC} = −30 V, I_C = 750 mA, I_{B1} = 15 mA)	t_f	–	–	130	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulsed Condition: Pulse Width = 300 msec, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

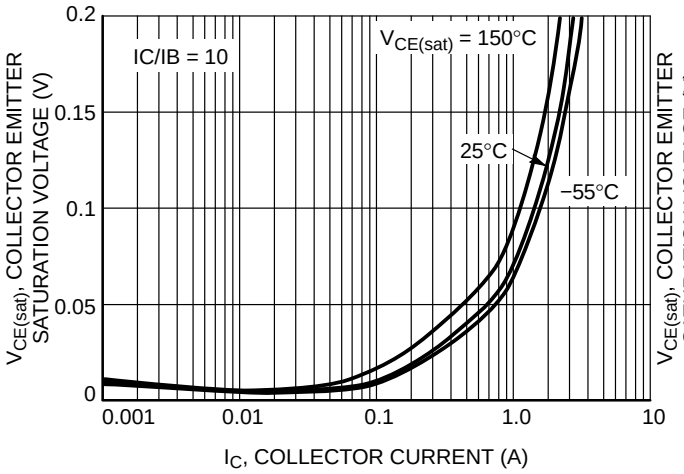


Figure 1. Collector Emitter Saturation Voltage vs. Collector Current

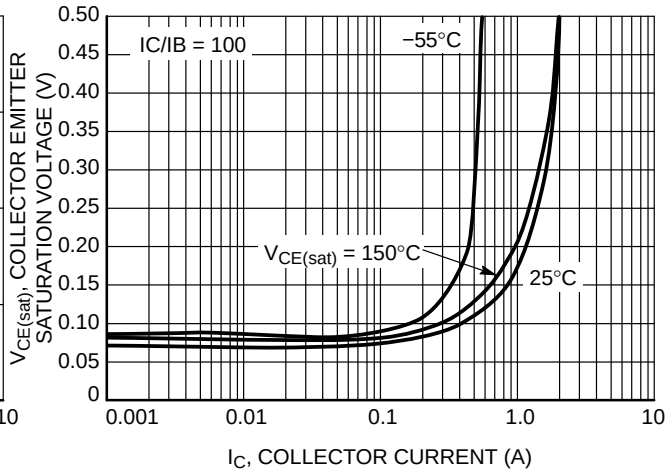


Figure 2. Collector Emitter Saturation Voltage vs. Collector Current

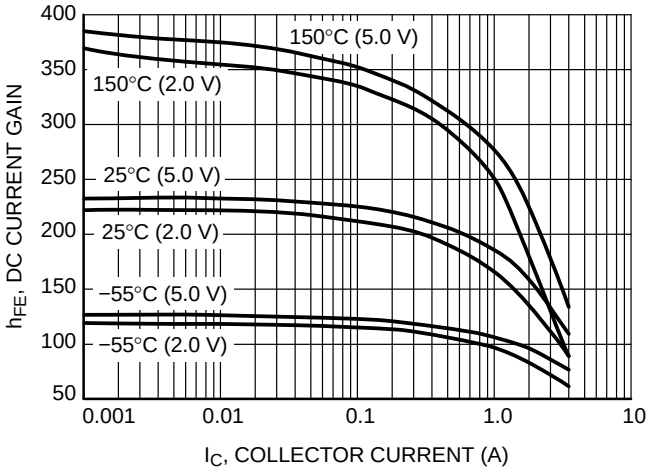


Figure 3. DC Current Gain vs. Collector Current

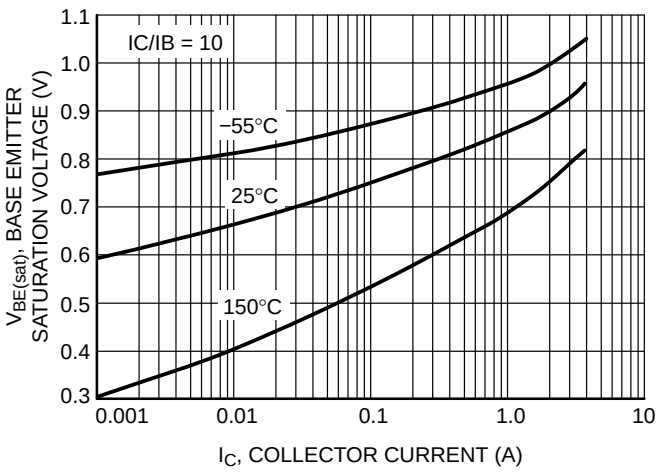


Figure 4. Base Emitter Saturation Voltage vs. Collector Current

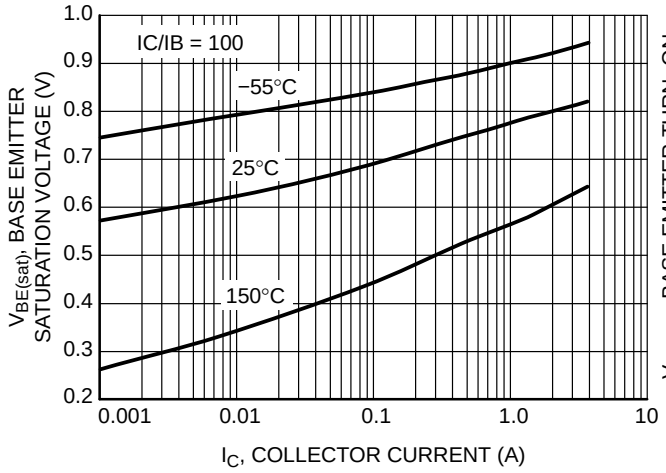


Figure 5. Base Emitter Saturation Voltage vs. Collector Current

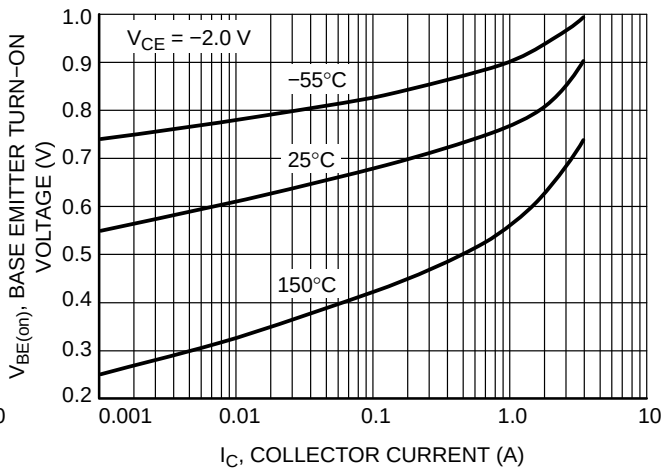


Figure 6. Base Emitter Turn−On Voltage vs. Collector Current

TYPICAL CHARACTERISTICS

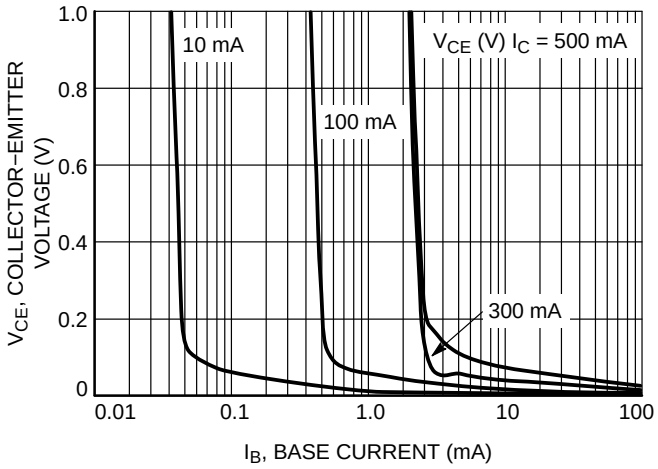


Figure 7. Saturation Region

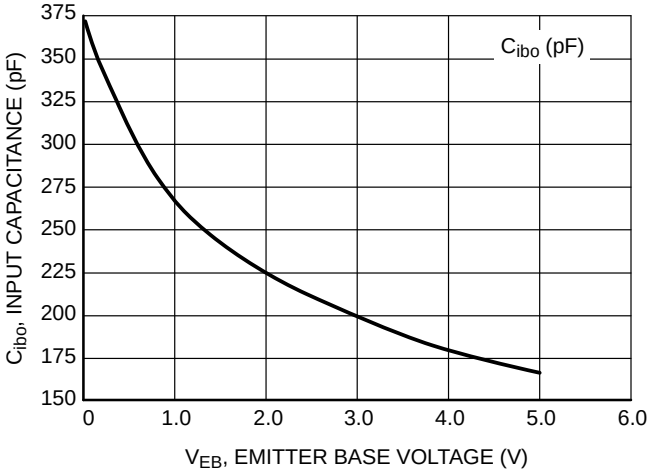


Figure 8. Input Capacitance

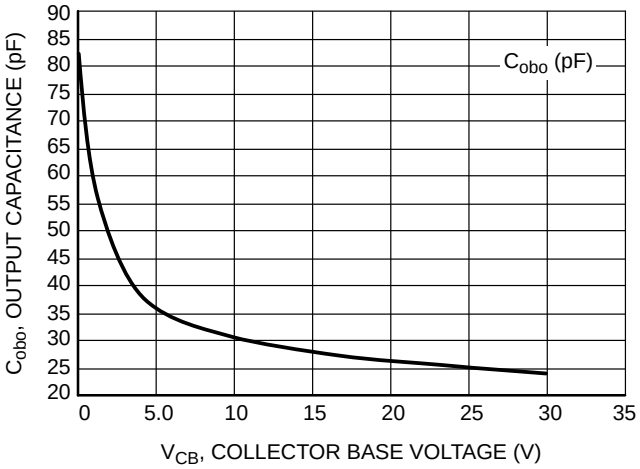


Figure 9. Output Capacitance

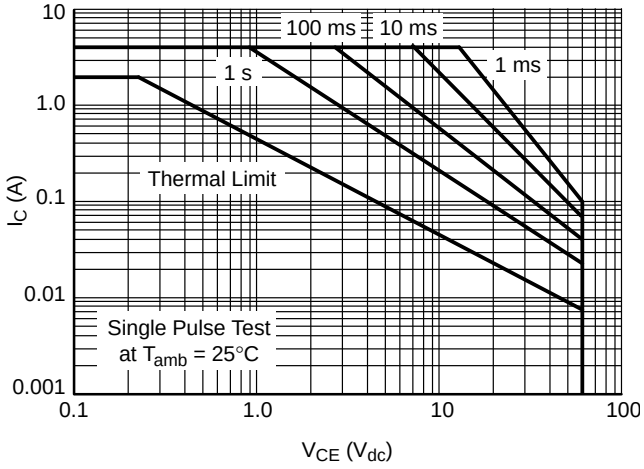
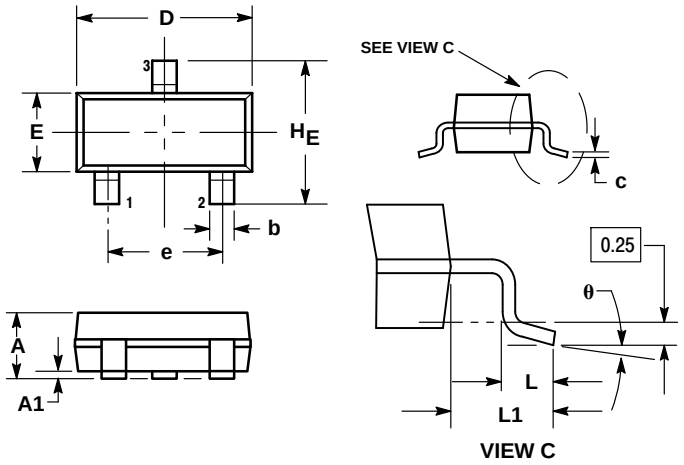


Figure 10. Safe Operating Area

PACKAGE DIMENSIONS

SOT−23 (TO−236)
CASE 318−08
ISSUE AP

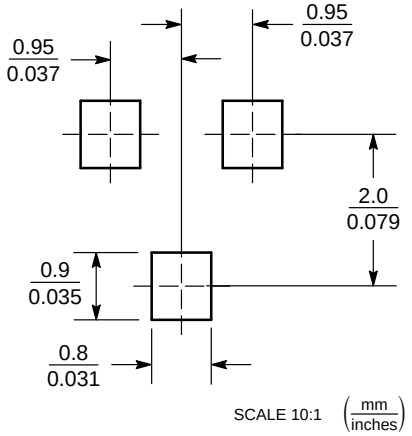


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.40	2.64	0.083	0.094	0.104
θ	0°	−−−	10°	0°	−−−	10°

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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