



Is Now Part of



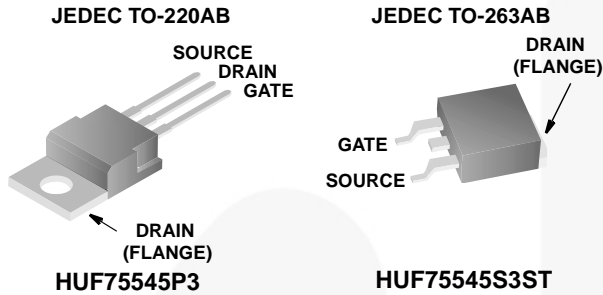
**ON Semiconductor®**

To learn more about ON Semiconductor, please visit our website at  
[www.onsemi.com](http://www.onsemi.com)

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

**N-Channel UltraFET Power MOSFET**  
**80 V, 75 A, 10 mΩ**

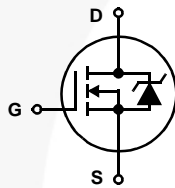
**Packaging**



**Features**

- Ultra Low On-Resistance
  - $r_{DS(ON)} = 0.010\Omega$ ,  $V_{GS} = 10V$
- Simulation Models
  - Temperature Compensated PSPICE® and SABER™ Electrical Models
  - Spice and SABER Thermal Impedance Models
  - [www.fairchildsemi.com](http://www.fairchildsemi.com)
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

**Symbol**



**Ordering Information**

PART NUMBER	PACKAGE	BRAND
HUF75545P3	TO-220AB	75545P
HUF75545S3ST	TO-263AB	75545S

**Absolute Maximum Ratings**  $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

	HUF75545P3, HUF75545S3ST	UNITS
Drain to Source Voltage (Note 1) . . . . .	$V_{DSS}$	80 V
Drain to Gate Voltage ( $R_{GS} = 20k\Omega$ ) (Note 1) . . . . .	$V_{DGR}$	80 V
Gate to Source Voltage . . . . .	$V_{GS}$	$\pm 20$ V
Drain Current		
Continuous ( $T_C = 25^\circ\text{C}$ , $V_{GS} = 10V$ ) (Figure 2) . . . . .	$I_D$	75 A
Continuous ( $T_C = 100^\circ\text{C}$ , $V_{GS} = 10V$ ) (Figure 2) . . . . .	$I_D$	73 A
Pulsed Drain Current . . . . .	$I_{DM}$	Figure 4
Pulsed Avalanche Rating . . . . .	UIS	Figure 6
Power Dissipation . . . . .	$P_D$	270 W
Derate Above $25^\circ\text{C}$ . . . . .		1.8 W/ $^\circ\text{C}$
Operating and Storage Temperature . . . . .	$T_J, T_{STG}$	-55 to 175 $^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s. . . . .	$T_L$	300 $^\circ\text{C}$
Package Body for 10s, See Techbrief TB334. . . . .	$T_{pkg}$	260 $^\circ\text{C}$

NOTES:

1.  $T_J = 25^\circ\text{C}$  to  $150^\circ\text{C}$ .

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Product reliability information can be found at <http://www.fairchildsemi.com/products/discrete/reliability/index.html>

For severe environments, see our Automotive HUFA series.

All Fairchild semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

## HUF75545P3, HUF75545S3S

### Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
<b>OFF STATE SPECIFICATIONS</b>							
Drain to Source Breakdown Voltage	$BV_{DSS}$	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$ (Figure 11)	80	-	-	V	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 75\text{V}$ , $V_{GS} = 0\text{V}$	-	-	1	$\mu\text{A}$	
		$V_{DS} = 70\text{V}$ , $V_{GS} = 0\text{V}$ , $T_C = 150^\circ\text{C}$	-	-	250	$\mu\text{A}$	
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA	
<b>ON STATE SPECIFICATIONS</b>							
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$ (Figure 10)	2	-	4	V	
Drain to Source On Resistance	$r_{DS(ON)}$	$I_D = 75\text{A}$ , $V_{GS} = 10\text{V}$ (Figure 9)	-	0.0082	0.010	$\Omega$	
<b>THERMAL SPECIFICATIONS</b>							
Thermal Resistance Junction to Case	$R_{\theta JC}$	TO-220 and TO-263	-	-	0.55	$^\circ\text{C/W}$	
Thermal Resistance Junction to Ambient	$R_{\theta JA}$		-	-	62	$^\circ\text{C/W}$	
<b>SWITCHING SPECIFICATIONS (<math>V_{GS} = 10\text{V}</math>)</b>							
Turn-On Time	$t_{ON}$	$V_{DD} = 40\text{V}$ , $I_D = 75\text{A}$ $V_{GS} = 10\text{V}$ , $R_{GS} = 2.5\Omega$	-	-	210	ns	
Turn-On Delay Time	$t_{d(ON)}$		-	14	-	ns	
Rise Time	$t_r$		-	125	-	ns	
Turn-Off Delay Time	$t_{d(OFF)}$		-	40	-	ns	
Fall Time	$t_f$		-	90	-	ns	
Turn-Off Time	$t_{OFF}$		-	-	195	ns	
<b>GATE CHARGE SPECIFICATIONS</b>							
Total Gate Charge	$Q_{g(TOT)}$	$V_{GS} = 0\text{V}$ to $20\text{V}$	$V_{DD} = 40\text{V}$ , $I_D = 75\text{A}$ , $I_{g(REF)} = 1.0\text{mA}$ (Figure 13)	-	195	235	nC
Gate Charge at 10V	$Q_{g(10)}$	$V_{GS} = 0\text{V}$ to $10\text{V}$		-	105	125	nC
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0\text{V}$ to $2\text{V}$		-	6.8	8.2	nC
Gate to Source Gate Charge	$Q_{gs}$			-	15	-	nC
Gate to Drain "Miller" Charge	$Q_{gd}$			-	43	-	nC
<b>CAPACITANCE SPECIFICATIONS</b>							
Input Capacitance	$C_{ISS}$	$V_{DS} = 25\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$ (Figure 12)	-	3750	-	pF	
Output Capacitance	$C_{OSS}$		-	1100	-	pF	
Reverse Transfer Capacitance	$C_{RSS}$		-	350	-	pF	

### Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	$V_{SD}$	$I_{SD} = 75\text{A}$	-	-	1.25	V
		$I_{SD} = 35\text{A}$	-	-	1.00	V
Reverse Recovery Time	$t_{rr}$	$I_{SD} = 75\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	100	ns
Reverse Recovered Charge	$Q_{RR}$	$I_{SD} = 75\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	300	nC

Typical Performance Curves

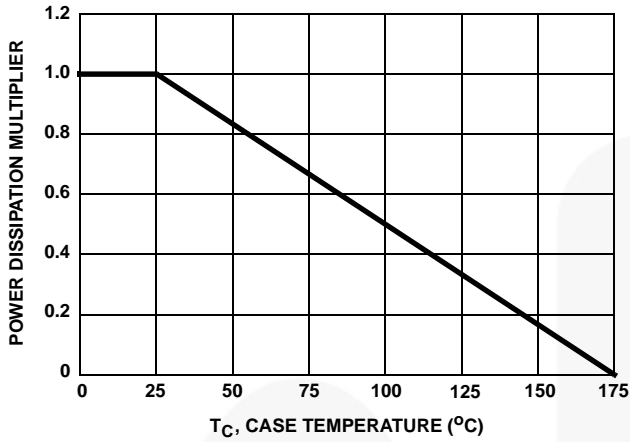


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

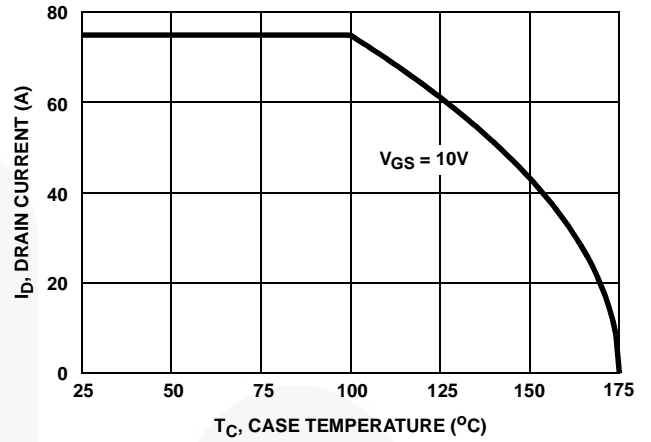


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

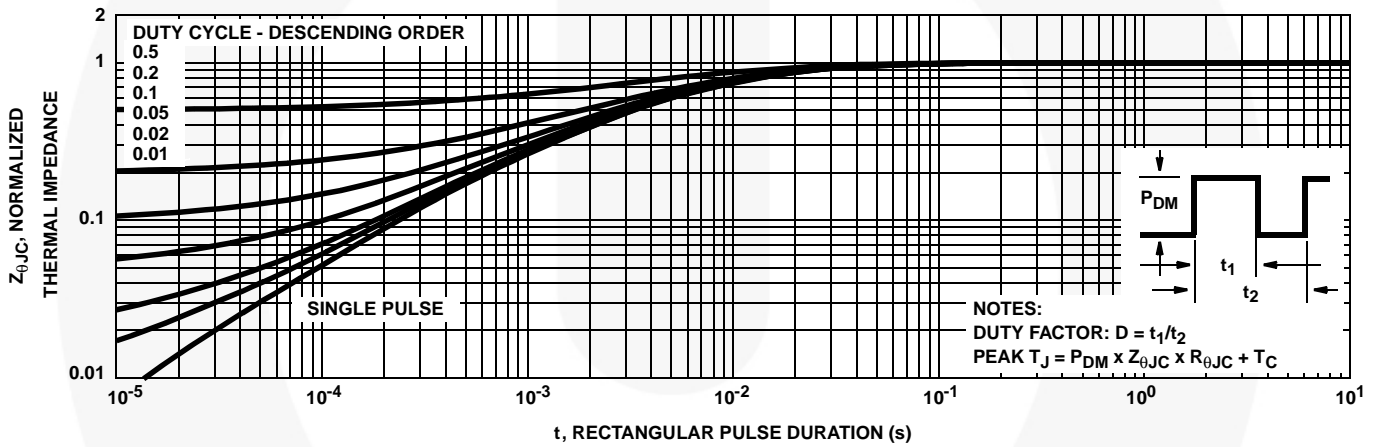


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

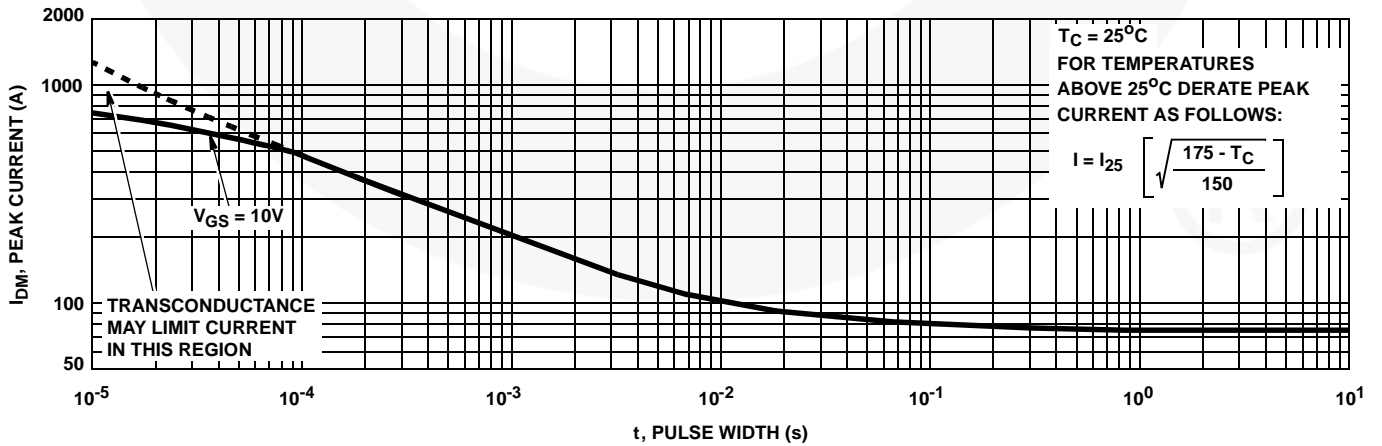


FIGURE 4. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)

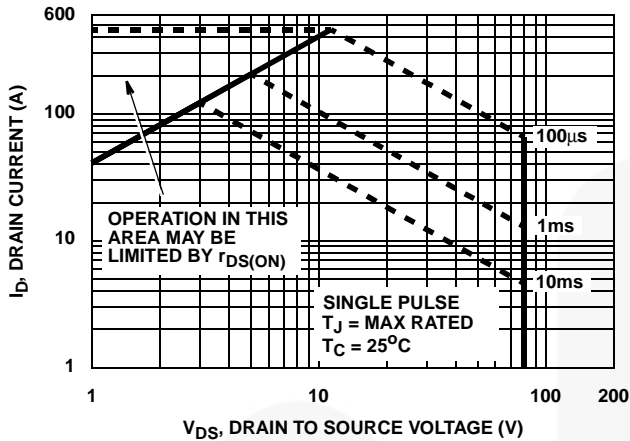
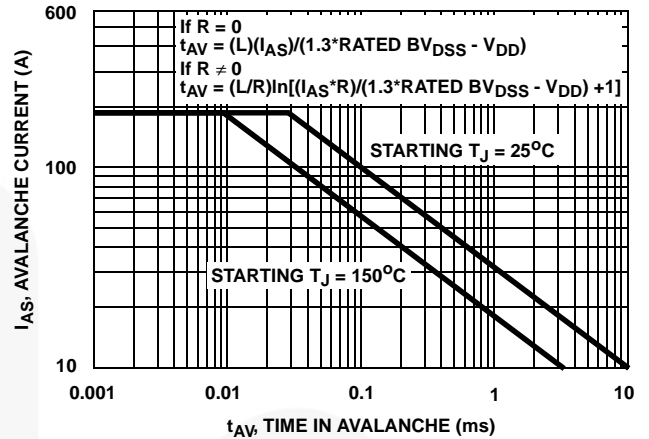


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

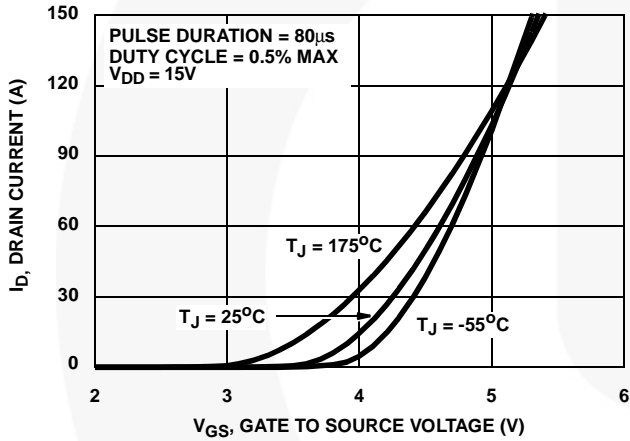


FIGURE 7. TRANSFER CHARACTERISTICS

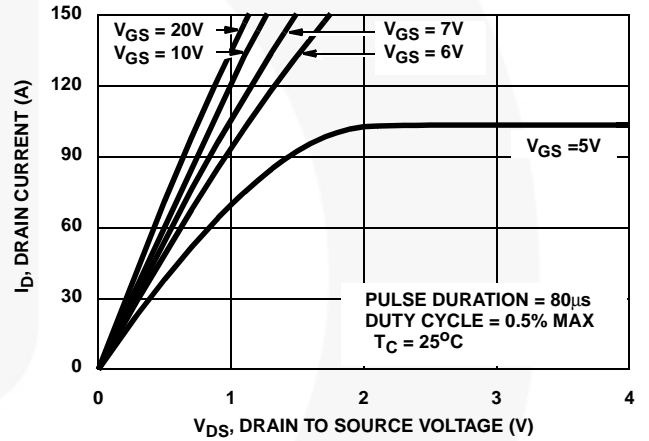


FIGURE 8. SATURATION CHARACTERISTICS

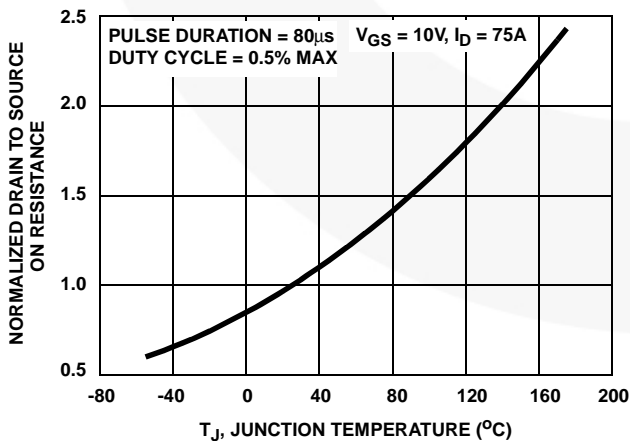


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

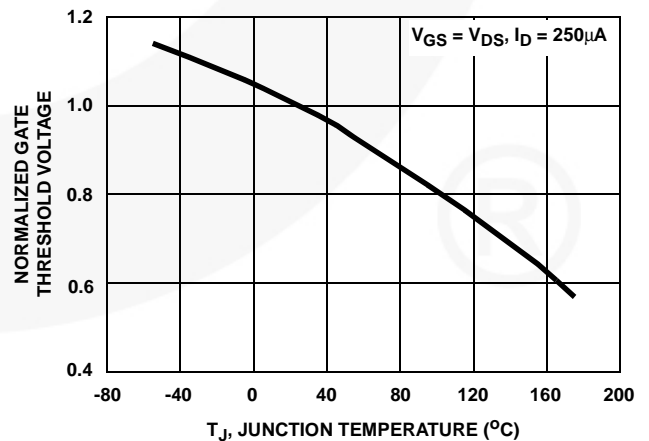


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

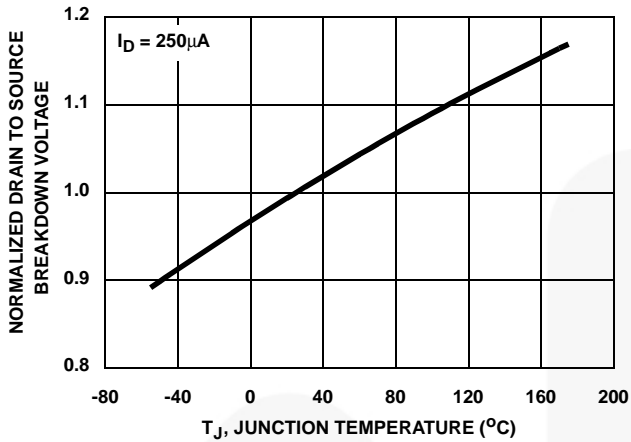


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

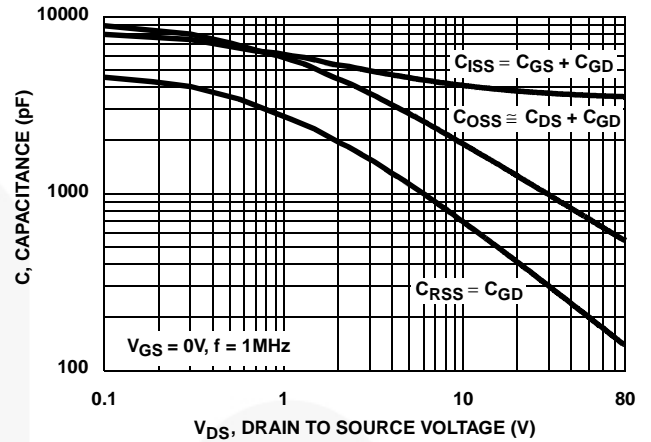
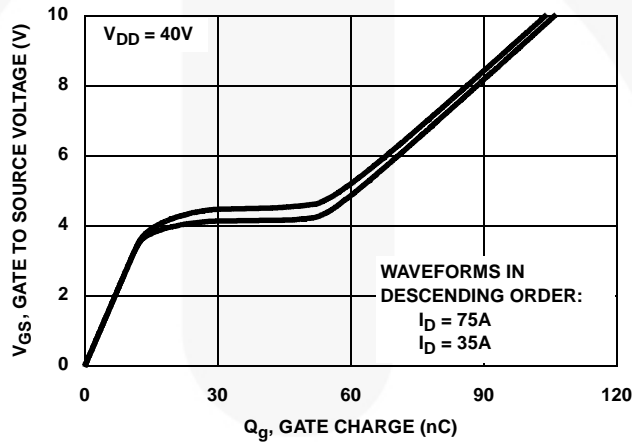


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

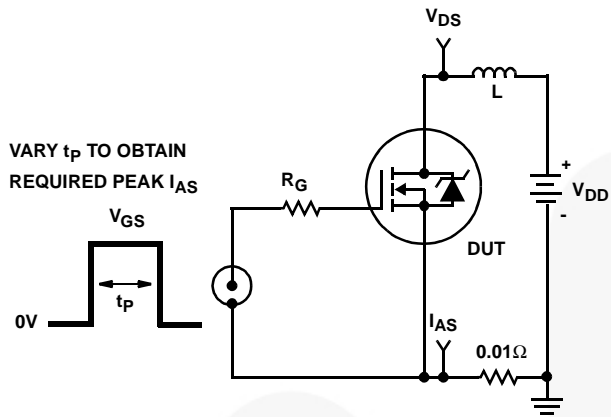


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

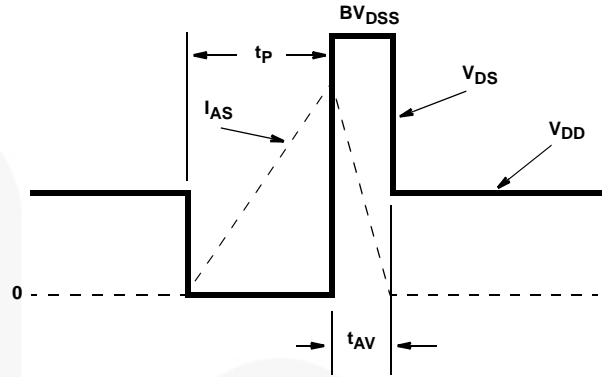


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

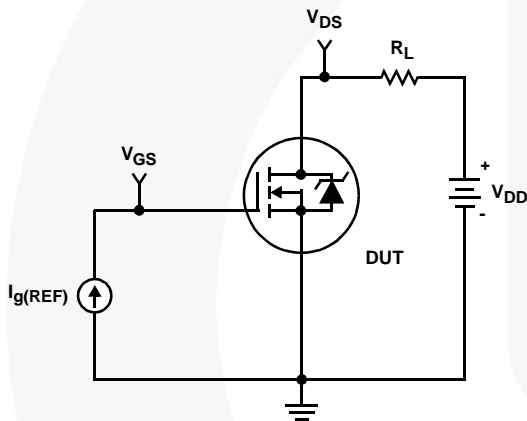


FIGURE 16. GATE CHARGE TEST CIRCUIT

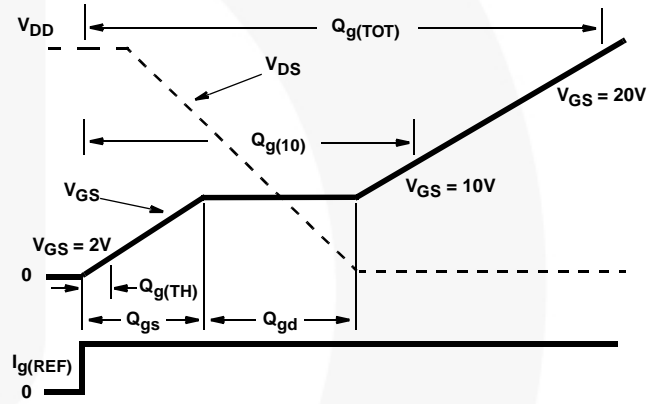


FIGURE 17. GATE CHARGE WAVEFORMS

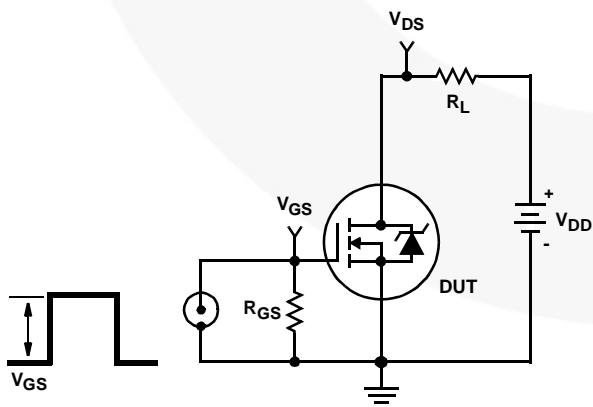


FIGURE 18. SWITCHING TIME TEST CIRCUIT

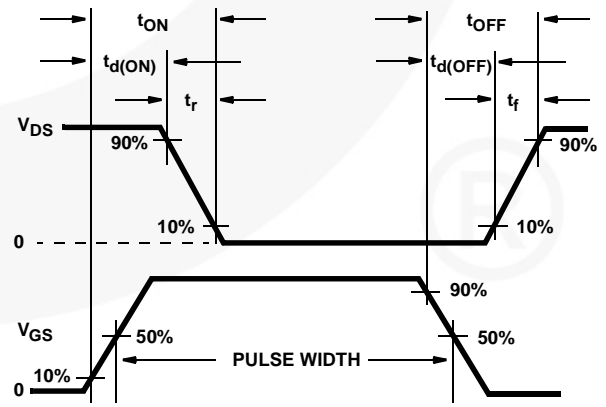


FIGURE 19. SWITCHING TIME WAVEFORM

# HUF75545P3, HUF75545S3S

## PSPICE Electrical Model

.SUBCKT HUF75545 2 1 3 ; rev 21 May 1999

CA 12 8 5.4e-9  
 CB 15 14 5.3e-9  
 CIN 6 8 3.4e-9

DBODY 7 5 DBODYMOD  
 DBREAK 5 11 DBREAKMOD  
 DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 87.4  
 EDS 14 8 5 8 1  
 EGS 13 8 6 8 1  
 ESG 6 10 6 8 1  
 EVTHRES 6 21 19 8 1  
 EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1.0e-9  
 LGATE 1 9 5.1e-9  
 LSOURCE 3 7 4.4e-9

MMED 16 6 8 8 MMEDMOD  
 MSTRO 16 6 8 8 MSTROMOD  
 MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1  
 RDRAIN 50 16 RDRAINMOD 4.80e-3  
 RGATE 9 20 0.87  
 RLDRAIN 2 5 10  
 RLGATE 1 9 51  
 RLSOURCE 3 7 44  
 RSLC1 5 51 RSLCMOD 1e-6  
 RSLC2 5 50 1e3  
 RSOURCE 8 7 RSOURCEMOD 1.6e-3  
 RVTHRES 22 8 RVTHRESMOD 1  
 RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD  
 S1B 13 12 13 8 S1BMOD  
 S2A 6 15 14 13 S2AMOD  
 S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

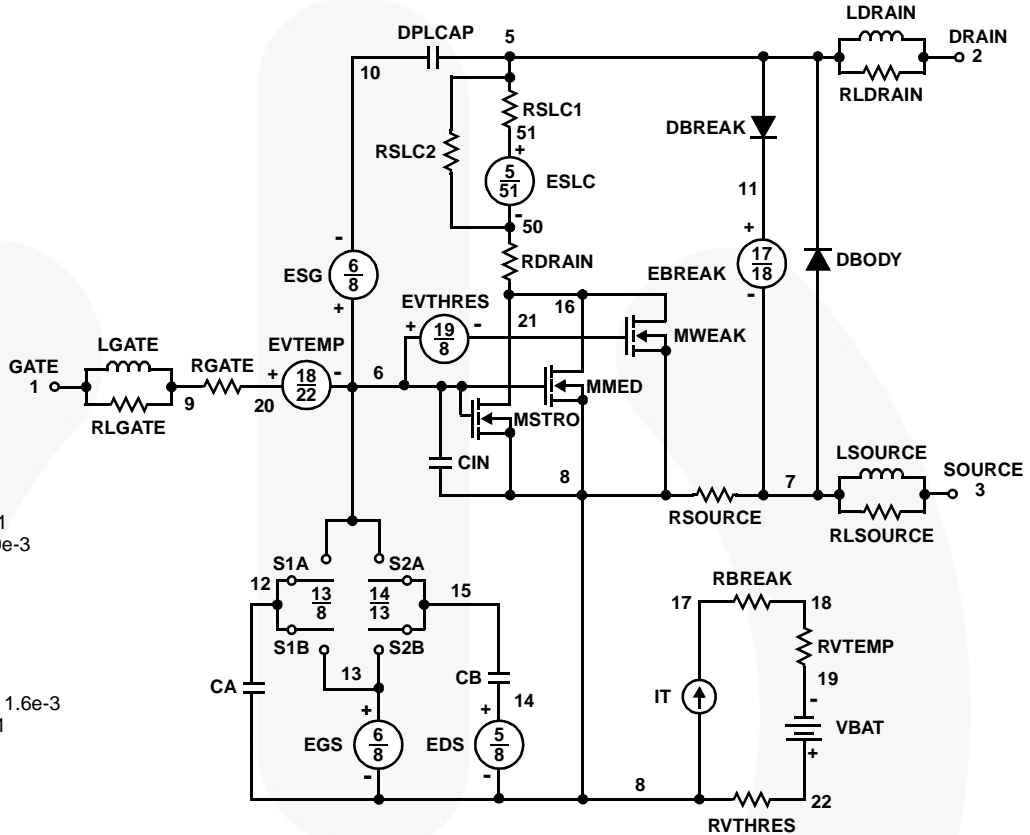
ESLC 51 50 VALUE=((V(5,51)/ABS(V(5,51)))^(PWR(V(5,51))/(1e-6\*320),3)))

.MODEL DBODYMOD D (IS = 3.6e-12 RS = 2.1e-3 TRS1 = 1.5e-3 TRS2 = 5.1e-6 CJO = 4.6e-9 TT = 3.3e-8 M = 0.55)  
 .MODEL DBREAKMOD D (RS = 2.3e-1 TRS1 = 0 TRS2 = -1.8e-5)  
 .MODEL DPLCAPMOD D (CJO = 4.8e-9 IS = 1e-30 N = 10 VJ = 1 M = 0.8)  
 .MODEL MMEDMOD NMOS (VTO = 3.04 KP = 6 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 0.87)  
 .MODEL MSTROMOD NMOS (VTO = 3.5 KP = 105 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)  
 .MODEL MWEAKMOD NMOS (VTO = 2.65 KP = 0.12 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 8.7)  
 .MODEL RBREAKMOD RES (TC1 = 1.3e-3 TC2 = -1e-6)  
 .MODEL RDRAINMOD RES (TC1 = 9e-3 TC2 = 2.8e-5)  
 .MODEL RSLCMOD RES (TC1 = 1.53e-3 TC2 = 2e-5)  
 .MODEL RSOURCEMOD RES (TC1 = 1e-3 TC2 = 1e-6)  
 .MODEL RVTHRESMOD RES (TC1 = -2.3e-3 TC2 = -1.2e-5)  
 .MODEL RVTEMPMOD RES (TC1 = -2.9e-3 TC2 = 5e-7)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -5 VOFF = -3)  
 .MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3 VOFF = -5)  
 .MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.5 VOFF = 0.5)  
 .MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.5 VOFF = -1.5)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.





**SABER Electrical Model**

REV 21 may 1999

template huf75545 n2,n1,n3  
electrical n2,n1,n3

```
{
var i iscl
d..model dbodymod = (is = 3.6e-12, cjo = 4.6e-9, tt = 3.3e-8, m = 0.55)
d..model dbreakmod = ()
d..model dplcapmod = (cjo = 4.8e-9, is = 1e-30, vj=1.0, m = 0.8 )
m..model mmedmod = (type=_n, vto = 3.04, kp = 6, is = 1e-30, tox = 1)
m..model mstrongmod = (type=_n, vto = 3.5, kp = 105, is = 1e-30, tox = 1)
m..model mweakmod = (type=_n, vto = 2.65, kp = 0.12, is = 1e-30, tox = 1)
sw_vcsp..model s1amod = (ron = 1e-5, roff = 0.1, von = -5, voff = -3)
sw_vcsp..model s1bmod = (ron = 1e-5, roff = 0.1, von = -3, voff = -5)
sw_vcsp..model s2amod = (ron = 1e-5, roff = 0.1, von = -1.5, voff = 0.5)
sw_vcsp..model s2bmod = (ron = 1e-5, roff = 0.1, von = 0.5, voff = -1.5)

```

```
c.ca n12 n8 = 5.4e-9
c.cb n15 n14 = 5.3e-9
c.cin n6 n8 = 3.4e-9

```

```
d.dbody n7 n71 = model=dbodymod
d.dbreak n72 n11 = model=dbreakmod
d.dplcap n10 n5 = model=dplcapmod

```

```
i.it n8 n17 = 1

```

```
l.l drain n2 n5 = 1e-9
l.l gate n1 n9 = 5.1e-9
l.l source n3 n7 = 4.4e-9

```

```
m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

```

```
res.rbreak n17 n18 = 1, tc1 = 1.3e-3, tc2 = -1e-6
res.rbody n71 n5 = 2.1e-3, tc1 = 1.5e-3, tc2 = 5.1e-6
res.rdbreak n72 n5 = 2.3e-1, tc1 = 0, tc2 = -1.8e-5
res.rdrain n50 n16 = 4.8e-3, tc1 = 9e-3, tc2 = 2.8e-5
res.rgate n9 n20 = 0.87
res.rldrain n2 n5 = 10
res.rlgate n1 n9 = 51
res.rlsource n3 n7 = 44
res.rslc1 n5 n51 = 1e-6, tc1 = 1.53e-3, tc2 = 2e-5
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 1.6e-3, tc1 = 1e-3, tc2 = 1e-6
res.rvtemp n18 n19 = 1, tc1 = -2.9e-3, tc2 = 5e-7
res.rvthres n22 n8 = 1, tc1 = -2.3e-3, tc2 = -1.2e-5

```

```
spe.ebreak n11 n7 n17 n18 = 87.4
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1

```

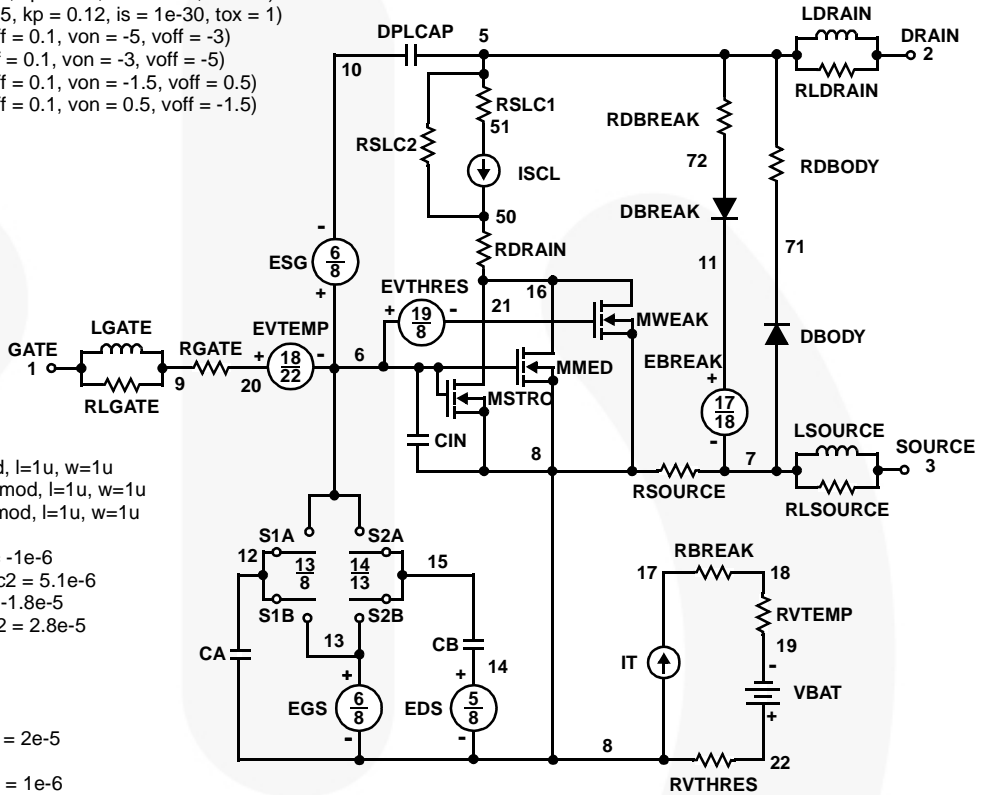
```
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

```

```
v.vbat n22 n19 = dc=1

```

```
equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = (((v(n5,n51))/(1e-9+abs(v(n5,n51))))*(abs(v(n5,n51))*1e6/320)** 3)
}
}
```



**SPICE Thermal Model**

REV 21 May 1999

HUF75545T

CTHERM1 th 6 6.4e-3  
 CHERM2 6 5 3.0e-2  
 CHERM3 5 4 1.4e-2  
 CHERM4 4 3 1.6e-2  
 CHERM5 3 2 5.5e-2  
 CHERM6 2 tl 1.5

RHERM1 th 6 3.2e-3  
 RHERM2 6 5 8.1e-3  
 RHERM3 5 4 2.3e-2  
 RHERM4 4 3 1.3e-1  
 RHERM5 3 2 1.8e-1  
 RHERM6 2 tl 3.8e-2

**SABER Thermal Model**

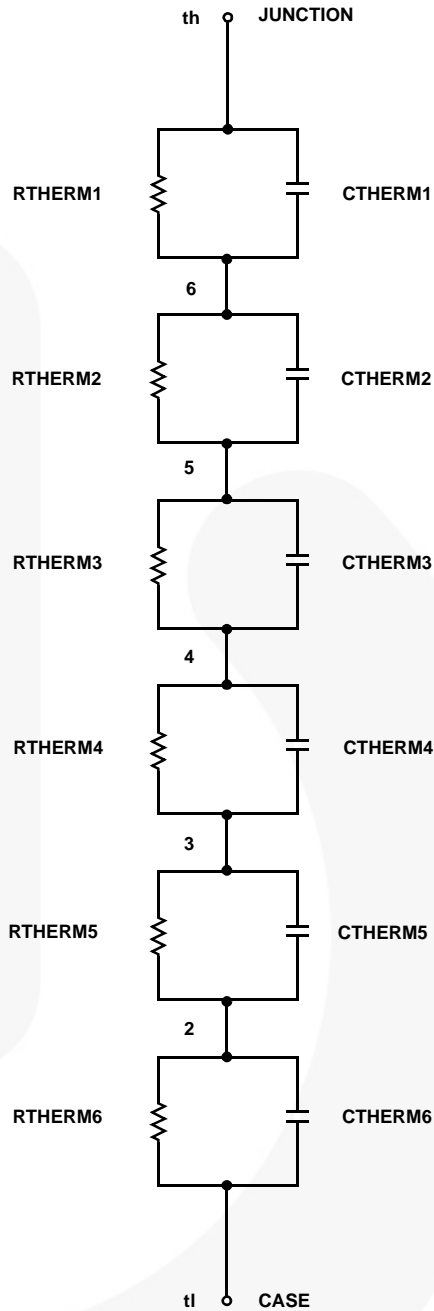
SABER thermal model HUF75545T

template thermal\_model th tl  
 thermal\_c th, tl

```
{
ctherm.ctherm1 th 6 = 6.4e-3
ctherm.ctherm2 6 5 = 3.0e-2
ctherm.ctherm3 5 4 = 1.4e-2
ctherm.ctherm4 4 3 = 1.6e-2
ctherm.ctherm5 3 2 = 5.5e-2
ctherm.ctherm6 2 tl = 1.5

```


```
rtherm.rtherm1 th 6 = 3.2e-3
rtherm.rtherm2 6 5 = 8.1e-3
rtherm.rtherm3 5 4 = 2.3e-2
rtherm.rtherm4 4 3 = 1.3e-1
rtherm.rtherm5 3 2 = 1.8e-1
rtherm.rtherm6 2 tl = 3.8e-2
}
```





## TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

- |   |   |                                       |                  |
|---|---|---------------------------------------|------------------|
| AccuPower™  | F-PFS™  | PowerTrench®                          | Sync-Lock™       |
| AX-CAP®*  | FRFET®  | PowerXS™                              | SYSTEM GENERAL®* |
| BitSiC™   | Global Power Resource™                          | Programmable Active Droop™            | TinyBoost®       |
| Build it Now™   | GreenBridge™                                    | QFET®                                 | TinyBuck®        |
| CorePLUS™   | Green FPS™                                      | QS™                                   | TinyCalc™        |
| CorePOWER™  | Green FPS™ e-Series™                            | Quiet Series™                         | TinyLogic®       |
| CROSSVOLT™  | Gmax™   | RapidConfigure™                       | TINYOPTO™        |
| CTL™  | GTO™  | Saving our world, 1mW/W/kW at a time™ | TinyPower™       |
| Current Transfer Logic™   | IntelliMAX™                                     | SignalWise™                           | TinyPWM™         |
| DEUXPEED®   | ISOPLANAR™                                      | SmartMax™                             | TinyWire™        |
| Dual Cool™  | Marking Small Speakers Sound Louder and Better™ | SMART START™                          | TranSiC™         |
| EcoSPARK®   | MegaBuck™                                       | Solutions for Your Success™           | TriFault Detect™ |
| EfficientMax™   | MICROCOPPLER™                                   | SPM®                                  | TRUECURRENT®*    |
| ESBC™   | MicroFET™                                       | STEALTH™                              | μSerDes™         |
|  | MicroPak™                                       | SuperFET®                             | UHC®             |
| Fairchild®  | MicroPak2™                                      | SuperSOT™-3                           | Ultra FRFET™     |
| Fairchild Semiconductor®  | MillerDrive™                                    | SuperSOT™-6                           | UniFET™          |
| FACT Quiet Series™  | MotionMax™                                      | SuperSOT™-8                           | VCX™             |
| FACT®   | mWSaver®  | SupreMOS®                             | VisualMax™       |
| FAST®   | OptoHiT™  | SyncFET™                              | VoltagePlus™     |
| FastvCore™  | OPTOLOGIC®                                      |                                       | XS™              |
| FETBench™   | OPTOPLANAR®                                     |                                       |                  |
| FPS™  |   |                                       |                  |

\*Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

## DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

## LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used here in:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
- A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, [www.Fairchildsemi.com](http://www.Fairchildsemi.com), under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufactures of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed application, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address and warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. 166