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# F DN358P

## Single P-Channel, Logic Level, PowerTrench® MOSFET

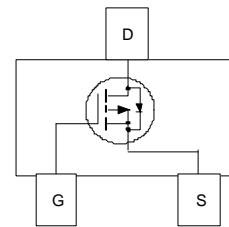
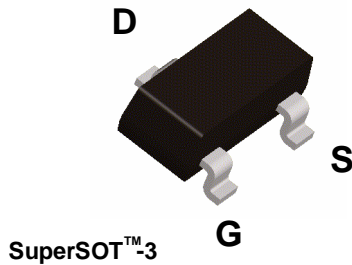
### General Description

This P-Channel Logic Level MOSFET is produced using Fairchild Semiconductor advanced Power Trench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

These devices are well suited for portable electronics applications: load switching and power management, battery charging circuits, and DC/DC conversion.

### Features

- -1.5 A, -30 V.  $R_{DS(ON)} = 125\text{ m}\Omega @ V_{GS} = -10\text{ V}$   
 $R_{DS(ON)} = 200\text{ m}\Omega @ V_{GS} = -4.5\text{ V}$
- Low gate charge (4 nC typical)
- High performance trench technology for extremely low  $R_{DS(ON)}$ .
- High power version of industry Standard SOT-23 package. Identical pin-out to SOT-23 with 30% higher power handling capability.



### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	-30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current – Continuous (Note 1a) – Pulsed	-1.5	A
		-5	
$P_D$	Power Dissipation for Single Operation (Note 1a) (Note 1b)	0.5	W
		0.46	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	250	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	75	$^\circ\text{C/W}$

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
358	F DN358P	7"	8mm	3000 units

## Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-22		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
		$V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^\circ\text{C}$			-10	
$I_{GSSF}$	Gate–Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate–Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA

### On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-1	-1.9	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		4		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = -10\text{ V}, I_D = -1.5\text{ A}$		105	125	m $\Omega$
		$V_{GS} = -10\text{ V}, I_D = -1.5\text{ A}, T_J = 125^\circ\text{C}$		148	210	
		$V_{GS} = -4.5\text{ V}, I_D = -1.2\text{ A}$		161	200	
$I_{D(on)}$	On–State Drain Current	$V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	-5			A
$g_{FS}$	Forward Transconductance	$V_{DS} = -5\text{ V}, I_D = -1.5\text{ A}$		3.5		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		182		pF
$C_{oss}$	Output Capacitance			56		pF
$C_{rss}$	Reverse Transfer Capacitance			26		pF

### Switching Characteristics (Note 2)

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = -15\text{ V}, I_D = -0.5\text{ A},$ $V_{GS} = -10\text{ V}, R_{GEN} = 6\ \Omega$		5	10	ns
$t_r$	Turn–On Rise Time			13	23	ns
$t_{d(off)}$	Turn–Off Delay Time			12	21	ns
$t_f$	Turn–Off Fall Time			2	4	ns
$Q_g$	Total Gate Charge	$V_{DS} = -15\text{ V}, I_D = -1.5\text{ A},$ $V_{GS} = -10\text{ V}$		4	5.6	nC
$Q_{gs}$	Gate–Source Charge			0.8		nC
$Q_{gd}$	Gate–Drain Charge			0.8		nC

### Drain–Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain–Source Diode Forward Current			-0.42		A
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -0.42\text{ A}$ (Note 2)		-0.76	-1.2	V

#### Notes:

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $250^\circ\text{C/W}$  when mounted on a  $0.02\text{ in}^2$  pad of 2 oz. copper.



b)  $270^\circ\text{C/W}$  when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$

## Typical Characteristics

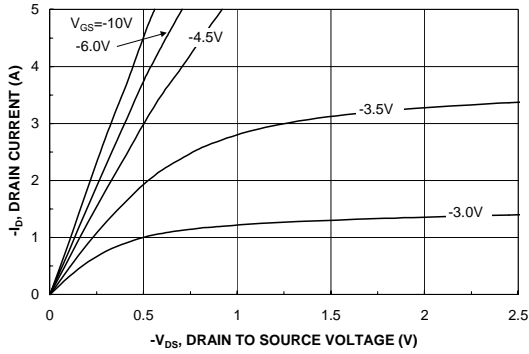


Figure 1. On-Region Characteristics.

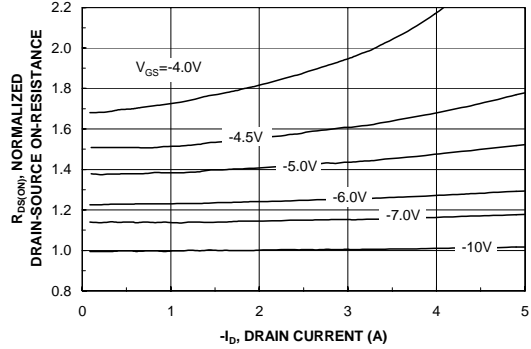


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

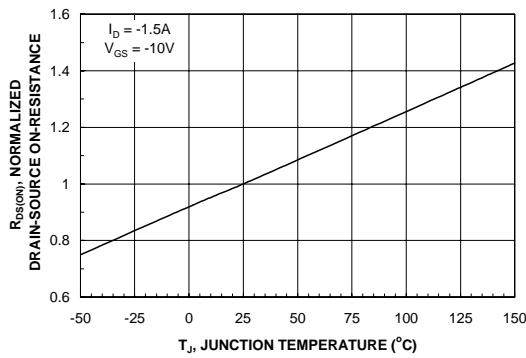


Figure 3. On-Resistance Variation with Temperature.

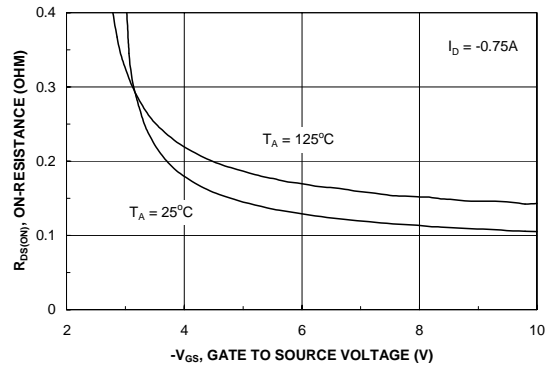


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

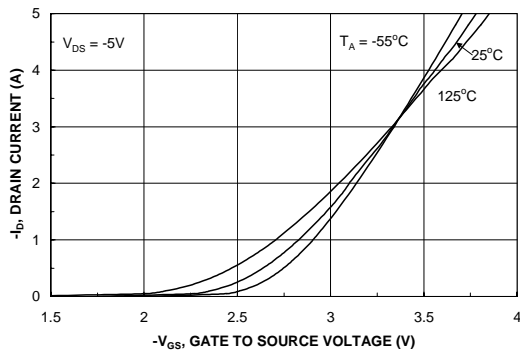


Figure 5. Transfer Characteristics.

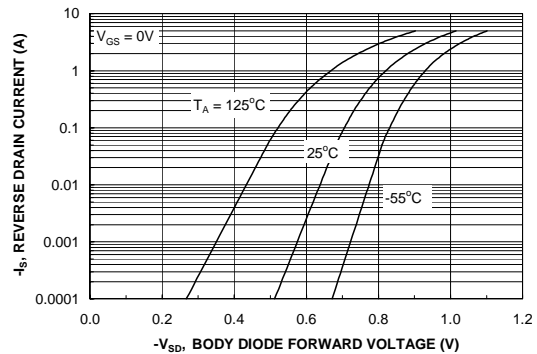


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## Typical Characteristics

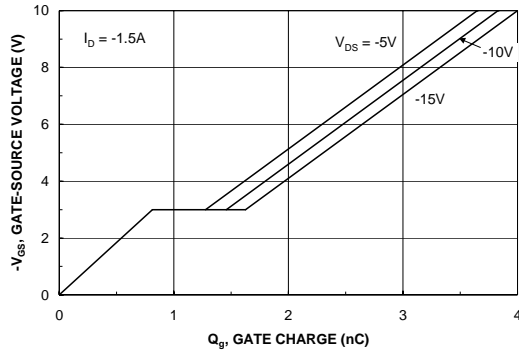


Figure 7. Gate Charge Characteristics.

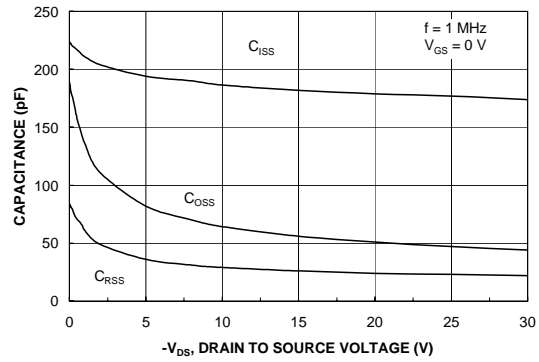


Figure 8. Capacitance Characteristics.

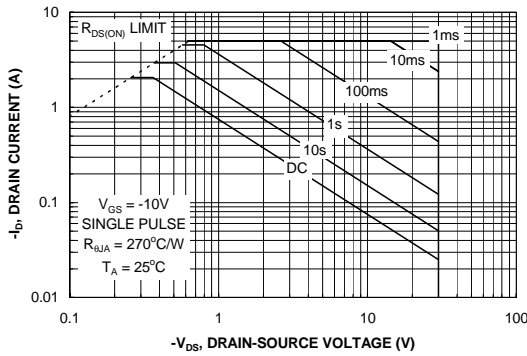


Figure 9. Maximum Safe Operating Area.

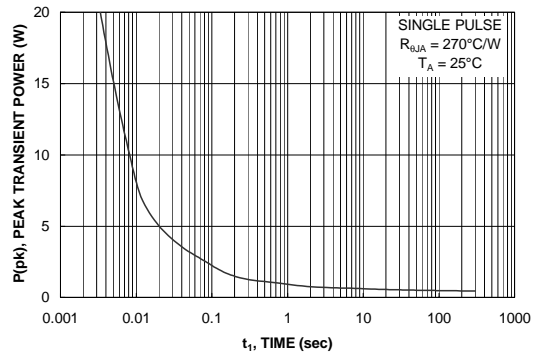


Figure 10. Single Pulse Maximum Power Dissipation.

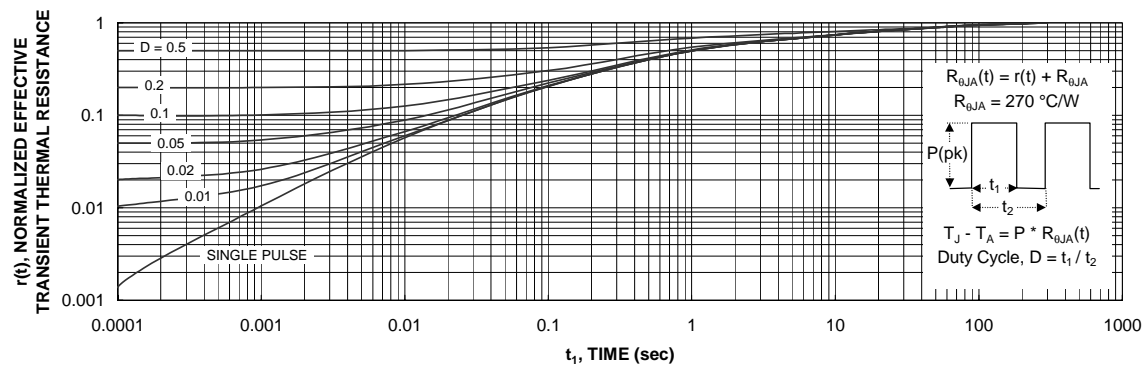


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

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