

Is Now Part of



ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at <u>www.onsemi.com</u>

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor dates sheds, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor dates sheds and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights of others. ON Semiconductor products are not designed, intended, or authorized for use on similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor and its officers, employees, subsidiaries, affliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out or i, directly or indirectly, any lay bed ON Semiconductor and its officers, employees, ween if such claim alleges that ON Semiconductor was negligent regarding the d

March 2011

FXLP34 Single Bit Uni-Directional Translator

Features

SEMICONDUCTOR

- 1.0V to 3.6V V_{CC} Supply Voltage
- Converts Any Voltage (1.0V to 3.6V) to (1.0V to 3.6V)
- 4.6V Tolerant Inputs and Outputs
- t_{PD}:
 - 4ns Typical for 3.0V to 3.6V V_{CC}
- Power-Off High Impedance Inputs and Outputs
- Static Drive (I_{OH}/I_{OL}):
 ±2.6mA at 3.00V V_{CC}
- Uses Proprietary Quiet Series™ Noise / EMI Reduction Circuitry
- Ultra-Small MicropakTM Leadless Packages
- Ultra-Low Dynamic Power

Ordering Information

Description

The FXLP34 is a single translator with two separate supply voltages: V_{CC1} for input translation voltages and V_{CC} for output translation voltages. The FXLP34 is part of Fairchild's Ultra Low Power (ULP) series of products. This device operates with VCC values from 1.0V to 3.6V, and is intended for use in portable applications that require ultra low power consumption.

The internal circuit is composed of a minimum of buffer stages, to enable ultra low dynamic power.

The FXLP34 is uniquely designed for optimized power and speed, and is fabricated with an advanced CMOS technology to achieve high-speed operation while maintaining low CMOS power dissipation.

-			
Part Number	Top Mark	Package	Packing Method
FXLP34P5X	X34	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3000 Units on Tape & Reel
FXLP34L6X	Х3	6-Lead MicroPak™, 1.00mm Wide	5000 Units on Tape & Reel
FXLP34FHX	ХЗ	6-Lead, MicroPak2, 1x1mm Body, .35mm Pitch	5000 Units on Tape & Reel

Micropak[™] and Quiet Series[™] are trademarks of Fairchild Semiconductor Corporation.

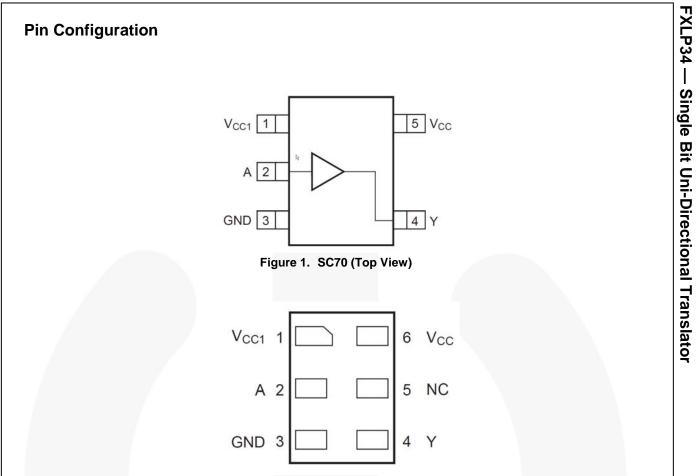


Figure 2. MicroPak[™] (Top Through View)

Pin Definitions

Pin # SC70	Pin # MicroPak™	Name	Description
1	1	V _{CC1}	Input Translation Voltage
2	2 2		Input
3	3 3		Ground
4	4 4		Output
	5		No Connect
5	6	V _{cc}	Output Translation Voltage

Truth Table

Inputs	Outputs
A	Y
L	L
Н	Н

H = Logic Level HIGH

L = Logic Level Low

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parame	eter	Min.	Max.	Unit	
V _{CC} , V _{CC1}	Supply Voltage		-0.5	+4.6	V	
V _{IN}	DC Input Voltage		-0.5	+4.6	V	
N		HIGH or LOW State ⁽¹⁾	-0.5	V _{CC} +0.5V	V	
V _{OUT}	DC Output Voltage	V _{CC} =0V	-0.5	+4.6	V	
I _{IK}	DC Input Diode Current	V _{IN} < 0		-50	mA	
	DC Output Diada Current	V _{OUT} < 0V		-50	mA	
I _{OK}	DC Output Diode Current	$V_{OUT} > V_{CC}$		+50	IIIA	
I _{OH} /I _{OL}	DC Output Source/Sink Curre	ent		±50	mA	
I _{CC} or I _{GND}	DC V _{CC} or Ground Current pe	er Supply Pin		±100	mA	
T _{STG}	Storage Temperature Range		-65	150	°C	
		SC70-6		180		
PD	Power Dissipation at +85°C	MicroPak™-6		130	mW	
		MicroPak2 [™] -6		120		
ESD	Human Body Model, JEDEC:JESD22-A114			4000	V	
ESD	Charge Device Model, JEDE	C:JESD22-C101		2000	V	

Note:

1. I_o Absolute Maximum Rating must be observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit	
V _{CC} , V _{CC1}	Supply Voltage		1.0	3.6	V	
V _{IN}	Input Voltage		0	3.6	V	
V		HIGH or LOW State	0	V _{CC}	v	
V _{OUT}	Output Voltage	V _{CC} =0V	0	3.6	v	
		V _{CC} =3.0 to 3.6V		±2.6		
		V _{CC} =2.3 to 2.7V		±2.1		
1 /1	Output Current in L	V _{CC} =1.65 to 1.95V		±1.5	mA	
I _{OH} /I _{OL}	Output Current in I _{OH} /I _{OL}	V _{CC} =1.40 to 1.60V		±1.0		
		V _{CC} =1.10 to 1.30V		±0.5		
		V _{CC} =1.0V		±20	μA	
T _A	Operating Temperature, Free Air		-40	+85	°C	
		SC70-6		425	°C/W	
θ_{JA}	Thermal Resistance	MicroPak™-6		500		
		MicroPak2 [™] -6		560		

Note:

2. Unused inputs must be held HIGH or LOW. They may not float.

.	-				T _A =+	-25°C	T _A =-40 t	o +85°C	
Symbol	Parameter	ameter Condition	V _{cc} (V)	V _{CC1} (V)	Min.	Max.	Min.	Max.	Uni
				1.0	$0.65 \text{ x V}_{\text{CCI}}$		$0.65 \text{ x V}_{\text{CCI}}$		
				1.10≤V _{CC1} ≤1.30	0.65 x V _{CCI}		$0.65 \text{ x V}_{\text{CCI}}$		
	HIGH Level			1.40≤V _{CC1} ≤1.60	0.65 x V _{CCI}		0.65 x V _{CCI}		
VIH	Input (V _{CC1})		1.0 to 3.6	1.65≤V _{CC1} ≤1.95	0.65 x V _{CCI}		0.65 x V _{CCI}		V
				2.30≤V _{CC1} ≤2.70	1.6		1.6		
				3.00≤V _{CC1} ≤3.60	2.1		2.1		
				1.0		$0.35 \text{ x V}_{\text{CCI}}$		$0.35 \text{ x V}_{\text{CCI}}$	
	V _{IL} LOW Level			1.10≤V _{CC1} ≤1.30		$0.35 \text{ x V}_{\text{CCI}}$		$0.35 \text{ x V}_{\text{CCI}}$	
				1.40≤V _{CC1} ≤1.60		0.35 x V _{CCI}		$0.35 \times V_{CCI}$	۱.,
V _{IL}			1.0 to 3.6	1.65≤V _{CC1} ≤1.95		0.35 x V _{CCI}		0.35 x V _{CCI}	V
				2.30≤V _{CC1} ≤2.70		0.7		0.7	
			3.00≤V _{CC1} ≤3.60		0.9		0.9		
			1.0		V _{cc} -0.1		V _{cc} -0.1		
		3/2	1.10≤V _{CC1} ≤1.30		V _{cc} -0.1		V _{cc} -0.1		
V _{он} HIGH Lev Output (V			1.40≤V _{CC1} ≤1.60		V _{cc} -0.1		V _{cc} -0.1		
		I _{ОН} =-20µА	1.65≤V _{CC1} ≤1.95	1.0 to 3.6	V _{cc} -0.1		V _{cc} -0.1		
			2.30≤V _{CC1} ≤2.70		V _{cc} -0.1		V _{cc} -0.1		
	HIGH Level		3.00≤V _{CC1} ≤3.60		V _{cc} -0.1		V _{cc} -0.1		v
	Output (V _{CC})	I _{OH} =-0.5mA	1.10≤V _{CC1} ≤1.30		0.75 x V _{cc}		0.70 x V _{cc}		
		I _{OH} =-1.0mA	1.40≤V _{CC1} ≤1.60		1.07		0.99		1
		I _{OH} =-1.5mA	1.65≤V _{CC1} ≤1.95	1.0 to 3.6	1.24		1.22		
		I _{он} =-2.1mA	2.30≤V _{CC1} ≤2.70		1.95		1.87		
		I _{он} =-2.6mA	3.00≤V _{CC1} ≤3.60		2.61		2.55		
			1.0			0.1		0.1	
			1.10≤V _{CC1} ≤1.30			0.1		0.1	
		I _{OL} =20µA	1.40≤V _{CC1} ≤1.60	1.0 to 3.6		0.1		0.1	
			1.65≤V _{CC1} ≤1.95			0.1		0.1	
	LOW Level		2.30≤V _{CC1} ≤2.70			0.1		0.1	
V _{OL}	Output	I _{OL} =0.5mA	1.10≤V _{CC1} ≤1.30			0.30 x V _{cc}		0.30 x V _{cc}	V
		I _{OL} =1.0mA	1.40≤V _{CC1} ≤1.60			0.31		0.37	
		I _{OL} =1.5mA	1.65≤V _{CC1} ≤ 1.95	1.0 to 3.6		0.31		0.35	
		I _{OL} =2.1mA	2.30≤V _{CC1} ≤2.70			0.31		0.33	
		I _{OL} =2.6mA	3.00≤V _{CC1} ≤3.60			0.31		0.33	
I _{IN}	Input Leakage Current	$\begin{array}{l} 0 \leq V_{\text{IN}} \\ \leq 3.60 \end{array}$		1.0 to 3.6		±0.1		±1.0	μA
I _{OFF}	Power Off Leakage Current	$\begin{array}{l} 0 \leq (V_{\text{IN}}, V_{\text{O}}) \\ \leq 3.60 \end{array}$	0	0		1.0		5.0	μA
I _{cc}	Quiescent Supply Current	V _{IN} =V _{CC} or GND	1.0 to 3.6	1.0 to 3.6		0.9		5.0	μA

Continued on the following page...

0	Demonster	O an all the m	V 00		T _A =+25°0	C	T _A =-40 1	to +85°C	11	F 1
Symbol	Parameter	Condition	V _{CC1} (V)	Min.	Тур.	Max.	Min.	Max.	Unit	Figure
		anslation $R_L=1M\Omega$	1.0		26.0					Figure 3, Figure 4
			1.10 to 1.30	15.0	25.0	38.1	12.0	43.3		
	Propagation Delay Output		1.40 to 1.60	14.0	24.0	36.7	11.0	42.0		
t _{PHL} , t _{PLH}	Translation		1.65 to 1.95	13.0	23.0	36.0	10.0	41.4	ns	
	V _{CC} (V)=1.0		2.30 to 2.70	12.0	22.0	35.5	9.0	40.9		
			3.00 to 3.60	11.0	21.0	35.5	8.0	40.6		
			1.0		18.0					
	Dreneration		1.10 to 1.30	8.0	15.0	23.2	6.0	41.0		
	Propagation Delay Output	ay Output $C_{L}=10pF$, nslation $R_{L}=1M\Omega$	1.40 to 1.60	7.5	14.0	21.7	5.5	39.1		Figure 3, Figure 4
t _{PHL} , t _{PLH}	Translation		1.65 to 1.95	7.0	13.0	20.9	5.0	32.3	ns	
	V _{CC} (V)=1.2		2.30 to 2.70	6.5	12.0	20.4	4.5	29.6		
			3.00 to 3.60	6.0	12.0	20.2	4.0	29.4		
Г			1.0		14.0					
	Decession		1.10 to 1.30	5.0	11.0	16.3	4.0	20.6		
	Propagation Delay Output	$C_{L}=10pF$,	1.40 to 1.60	4.8	10.0	14.8	3.5	19.3		Figure 3
t _{PHL} , t _{PLH}	Translation $V_{CC}(V)=1.5$	$R_L=1M\Omega$	1.65 to 1.95	4.5	9.0	14.1	3.0	18.7	ns	Figure 4
		_{CC} (V)=1.5	2.30 to 2.70	4.0	8.0	13.5	2.5	18.0		
			3.00 to 3.60	3.5	8.0	13.3	2.0	17.8		
			1.0		13.0				-	Figure 3,
	Propagation		1.10 to 1.30	4.0	9.0	13.5	3.0	17.5		
	Delay Output	C _L =10pF,	1.40 to 1.60	3.5	8.0	12.0	2.5	16.3		
t _{PHL} , t _{PLH}	Translation	$R_L=1M\Omega$	1.65 to 1.95	3.0	7.0	11.3	2.0	15.6	ns	Figure 4
	V _{CC} (V)=1.8		2.30 to 2.70	2.5	6.0	10.7	1.5	15.0		
			3.00 to 3.60	2.5	6.0	10.5	1.0	14.7		
			1.0		12.0					
	Dropogation		1.10 to 1.30	3.0	7.0	10.9	2.5	14.3		
	Propagation Delay Output	C _L =10pF,	1.40 to 1.60	2.5	6.0	9.4	2.0	13.1		Figure 3
t _{PHL} , t _{PLH}	Translation	$R_L=1M\Omega$	1.65 to 1.95	2.0	5.0	8.6	1.5	11.4	ns	Figure 4
	V _{CC} (V)=2.5		2.30 to 2.70	1.5	4.0	8.0	1.0	10.8		
			3.00 to 3.60	1.5	4.0	7.8	1.0	10.5		
			1.0		11.0					
	Propagation		1.10 to 1.30	3.0	6.0	10.1	2.0	13.8		
	Propagation Delay Output	C _L =10pF,	1.40 to 1.60	2.5	5.0	8.2	1.5	10.5		Figure 3
t _{PHL} , t _{PLH}	Translation	ranslation $R_L=1M\Omega$	1.65 to 1.95	2.0	4.0	7.4	1.0	9.9	ns	Figure 4
	V _{CC} (V)=3.3		2.30 to 2.70	1.0	3.0	6.8	1.0	9.2		
			3.00 to 3.60	1.0	3.0	6.6	1.0	9.0	1	

Continued on the following page...

	Devenueter	Condition	V 00		T _A =+25°	C	T _A =-40 1	to +85°C	11	Figure	
Symbol	Parameter	Condition	V _{CC1} (V)	Min.	Тур.	Max.	Min.	Max.	– Unit	Figure	
	Drananation		1.0		28.0					Figure 3,	
			1.10 to 1.30	16.0	27.0	43.0	12.0	44.8			
	Propagation Delay Output	C _L =15pF,	1.40 to 1.60	15.0	26.0	41.6	11.0	43.6			
t _{PHL} , t _{PLH}	Translation	$R_L=1M\Omega$	1.65 to 1.95	14.0	25.0	40.9	10.0	47.9	ns	Figure 4	
	V _{CC} (V)=1.0		2.30 to 2.70	13.0	24.0	40.5	9.0	47.5			
			3.00 to 3.60	12.0	23.0	40.4	8.0	41.4			
			1.0		19.0						
	Dropogation		1.10 to 1.30	9.0	16.0	24.6	8.0	43.1	ns		
	Propagation Delay Output		1.40 to 1.60	8.5	15.0	23.1	7.5	42.2		Figure 3	
t _{PHL} , t _{PLH}	Translation	$R_L=1M\Omega$	1.65 to 1.95	8.0	14.0	22.4	7.0	31.4	ns	Figure 4	
	V _{CC} (V)=1.2		2.30 to 2.70	7.5	13.0	21.8	6.5	30.7			
					3.00 to 3.60	7.0	13.0	21.6	6.0	30.5	
			1.0		15.0						
	Dresservitier	opagation	1.10 to 1.30	6.0	12.0	17.2	5.5	21.5		Figure 3,	
	Delay Output	C _L =15pF,	1.40 to 1.60	5.8	11.0	15.7	5.0	20.3			
t _{PHL} , t _{PLH}	Translation	$R_L=1M\Omega$	1.65 to 1.95	5.5	10.0	14.9	4.5	19.6	ns	Figure 4	
	V _{CC} (V)=1.5		2.30 to 2.70	5.0	9.0	14.3	4.0	18.9			
			3.00 to 3.60	4.5	.0	14.2	3.5	18.7			
			1.0		14.0				- ns	Figure 3, Figure 4	
	Drananation		1.10 to 1.30	5.0	8.0	14.2	5.5	18.2			
	Propagation Delay Output	C _L =15pF,	1.40 to 1.60	4.5	7.0	12.7	4.0	17.0			
t _{PHL} , t _{PLH}	Translation	$R_L=1M\Omega$	1.65 to 1.95	4.0	6.0	11.9	3.5	16.3			
	V _{CC} (V)=1.8		2.30 to 2.70	3.5	5.0	11.3	3.0	15.7			
			3.00 to 3.60	3.5	5.0	11.2	2.5	14.4			
			1.0		12.0						
	Dresservitier		1.10 to 1.30	4.0	7.0	11.3	3.5	14.9			
	Propagation Delay Output	C _L =15pF,	1.40 to 1.60	3.5	6.0	9.8	3.0	13.6		Figure 3	
t _{PHL} , t _{PLH}	Translation	$R_L=1M\Omega$	1.65 to 1.95	3.0	5.0	9.1	2.5	12.0	ns	Figure 4	
	V _{CC} (V)=2.5		2.30 to 2.70	2.5	4.0	8.5	2.0	11.3			
			3.00 to 3.60	2.5	4.0	8.3	2.0	11.1			
			1.0		11.0					T	
	Dropogation		1.10 to 1.30	3.0	6.0	10.5	2.0	14.2			
	Propagation Delay Output	C _L =15pF,	1.40 to 1.60	2.5	5.0	8.6	1.5	11.0		Figure 3	
PHL, PLH	Translation	$R_L=1M\Omega$	1.65 to 1.95	2.0	4.0	7.8	1.0	10.3	ns	Figure 3, Figure 4	
	V _{CC} (V)=3.3		2.30 to 2.70	1.5	3.0	7.2	1.0	9.7			
			3.00 to 3.60	1.5	3.0	7.0	1.0	9.4			

Continued on the following page...

	Parameter	Condition	V 00		T _A =+25°	C	T _A =-40 t	to +85°C	11	F ierra		
Symbol		Condition	V _{CC1} (V)	Min.	Тур.	Max.	Min.	Max.	Unit	Figure		
			1.0		34.0							
	Dropogation		1.10 to 1.30	19.0	32.0	48.6	15.0	55.5				
	Propagation Delay Output	C _L =30pF,	1.40 to 1.60	18.0	31.0	47.1	14.0	52.3		Figure 3,		
t _{PHL} , t _{PLH}	Translation	$R_L=1M\Omega$	1.65 to 1.95	17.0	30.0	46.4	13.0	50.6	ns	Figure 4		
	V _{CC} (V)=1.0		2.30 to 2.70	16.0	29.0	45.9	12.0	49.2				
			3.00 to 3.60	15.0	28.0	45.8	10.0	49.1				
			1.0		22.0							
	Dreneration		1.10 to 1.30	11.0	19.0	29.0	10.0	46.5				
	Propagation Delay Output		1.40 to 1.60	10.0	18.0	27.5	9.0	42.6		Figure 3		
t _{PHL} , t _{PLH}	Translation	$R_L=1M\Omega$	1.65 to 1.95	9.0	17.0	26.7	8.0	36.7	ns –	Figure 4		
	$V_{CC}(V)=1.2$		2.30 to 2.70	8.5	16.0	26.1	7.0	36.0				
			3.00 to 3.60	8.0	16.0	26.0	6.0	35.9				
			1.0		16.0					Figure 3,		
	Description		1.10 to 1.30	6.0	13.0	19.8	5.5	25.3				
	Propagation Delay Output	C _L =30pF,	1.40 to 1.60	5.8	12.0	18.3	5.0	23.0				
t _{PHL} , t _{PLH}	Translation	$R_L=1M\Omega$	1.65 to 1.95	5.5	11.0	17.6	4.5	22.4	ns	Figure 4		
	V _{CC} (V)=1.5		2.30 to 2.70	5.0	10.0	17.0	4.0	21.7				
			3.00 to 3.60	4.5	9.0	16.8	3.5	21.5				
		ppagation lay Output $C_L=30pF$,	1.0		15.0				- ns	Figure 3, Figure 4		
			1.10 to 1.30	5.0	11.0	16.2	5.5	20.4				
	Propagation Delay Output		1.40 to 1.60	4.5	10.0	14.7	4.0	19.2				
t _{PHL} , t _{PLH}	Translation	$R_L=1M\Omega$	1.65 to 1.95	4.0	9.0	13.9	3.5	18.5				
	V _{CC} (V)=1.8		2.30 to 2.70	3.5	8.0	13.3	3.0	17.9				
			3.00 to 3.60	3.5	8.0	13.1	2.5	17.6				
			1.0		13.0							
			1.10 to 1.30	4.0	8.0	12.7	3.5	15.9				
	Propagation Delay Output	C _L =30pF,	1.40 to 1.60	3.5	7.0	11.2	3.0	14.3		Figure 3		
t _{PHL} , t _{PLH}	Translation	$R_L=1M\Omega$	1.65 to 1.95	3.0	6.0	10.5	2.5	13.6	ns	Figure 4		
	V _{CC} (V)=2.5		2.30 to 2.70	2.5	5.0	9.9	2.0	12.8		1		
			3.00 to 3.60	2.5	5.0	9.7	2.0	12.5				
			1.0		12.0							
			1.10 to 1.30	3.0	8.0	11.7	2.0	15.0				
	Propagation Delay Output	C∟=30pF,	1.40 to 1.60	2.5	7.0	9.8	1.5	12.2		Figure 3, Figure 4		
t _{PHL} , t _{PLH}	Translation	$R_L=1M\Omega$	1.65 to 1.95	2.0	6.0	8.9	1.0	11.5	ns			
V		V _{cc} (V)=3.3			2.30 to 2.70	1.5	5.0	8.3	1.0	10.7		
			3.00 to 3.60	1.5	5.0	8.1	1.0	10.4				

Capacitance

Symbol	Parameter	Conditions	V _{cc} / V _{cc1} (V)	T _A =+25°C Typical	Units
CIN	Input Capacitance			2	pF
C _{I/O}	Input/Output Capacitance			4	pF
C _{PD}	Power Dissipation Capacitance	$V_{\text{I}}\text{=}0V$ or $V_{\text{CC1}}\text{, f}\text{=}10MHz\text{, }V_{\text{CC}}\text{ / }V_{\text{CC1}}\text{=}3.6V$	1.0 to 3.60	8	pF

Translator Power-up Sequence Recommendations

To ensure that the system does not experience unnecessary I_{CC} current draw, bus contention, or oscillations during power-up; adhere to the following guidelines. This device is designed with the output pin(s) supplied by V_{CC} and the input pin(s) supplied by V_{CC1} . The first recommendation is to begin by powering up the input side of the device with V_{CC1} . The Input pin(s) should be ramped with or ahead of V_{CC1} or held LOW. This guards against bus contentions and oscillations as

all inputs and the input V_{CC1} are powered at the same time. The output V_{CC} can then be powered to the target voltage level to which the device will translate. The output pin(s) then translate to logic levels dictated by the output V_{CC} levels.

Upon completion of these steps, the device can be configured for the desired operation. Following these steps helps prevent possible damage to the translator device as well as other system components.

AC Loadings and Waveforms

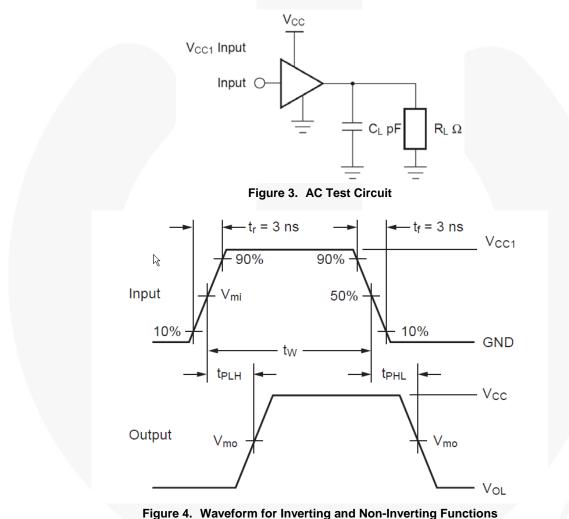


Table 1.	AC Load Table	
Taple I.	AC LOAD TADIE	

Symbol		V _{cc}							
Symbol	3.3V ±0.3V	2.5V ±0.2V	1.8V ±0.15V	1.5V ±0.10V	1.2V ±0.10V	1.0V			
V _{mi}	1.5V	V _{CC1} /2							
V _{mo}	1.5V	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _C C/2	V _{CC} /2			

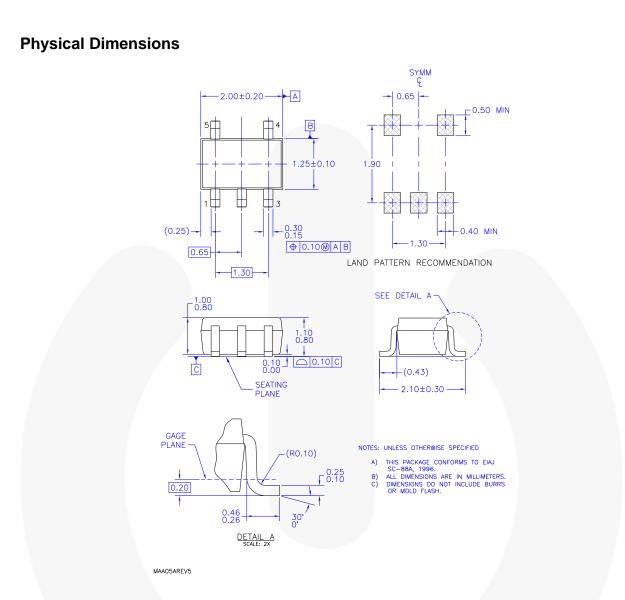


Figure 5. 5-Lead, SC70, EIAJ SC-88a, 1.25mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings: <u>http://www.fairchildsemi.com/packaging/</u>.

Tape and Reel Specifications

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications: <u>http://www.fairchildsemi.com/products/analog/pdf/sc70-5_tr.pdf</u>.

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
	Leader (Start End)	125 (Typical)	Empty	Sealed
P5X	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

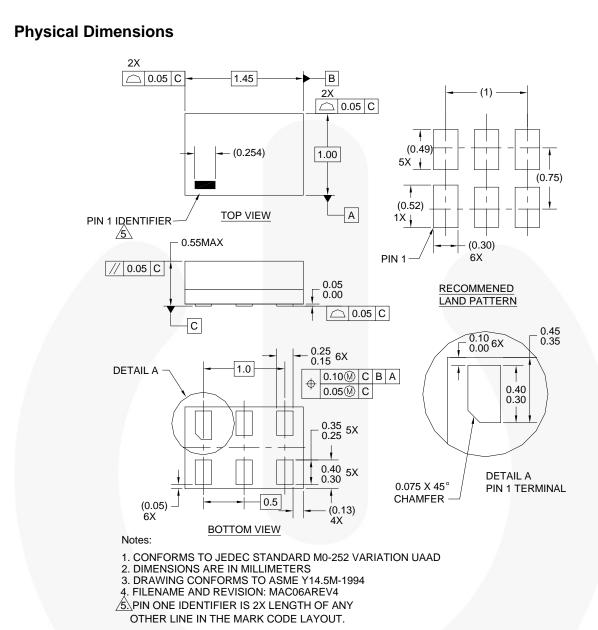


Figure 6. 6-Lead, MicroPak[™], 1.0mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings: <u>http://www.fairchildsemi.com/packaging/</u>.

Tape and Reel Specification

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications: <u>http://www.fairchildsemi.com/products/logic/pdf/micropak_tr.pdf</u>.

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
	Leader (Start End)	125 (Typical)	Empty	Sealed
L6X	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed



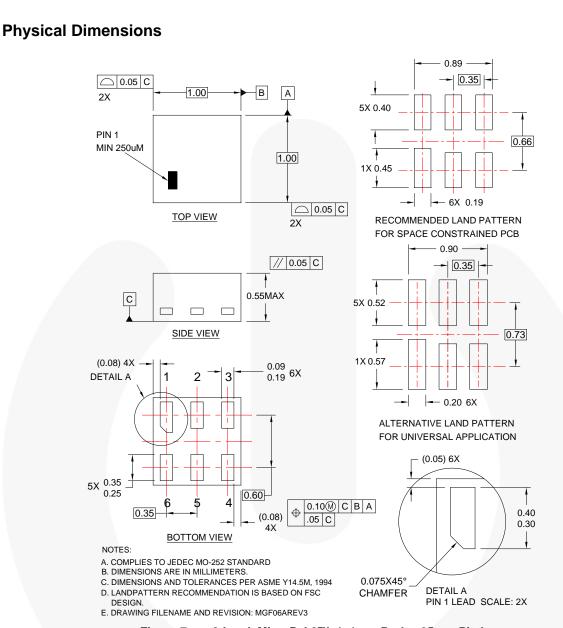


Figure 7. 6-Lead, MicroPak2™, 1x1mm Body, .35mm Pitch

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings: <u>http://www.fairchildsemi.com/packaging/</u>.

Tape and Reel Specification

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications: <u>http://www.fairchildsemi.com/packaging/MicroPAK2_6L_tr.pdf</u>.

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
	Leader (Start End)	125 (Typical)	Empty	Sealed
FHX	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed



TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

F-PFS™ AccuPower™ FREET® Auto-SPM™ AX-CAPTM* Build it Novv™ Green FPS™ CorePLUS™ Gmax™ CorePOWER™ **GTO™** CROSSVOLT IntelliMAX™ CTL™ Current Transfer Logic™ DEUXPEED[®] ISOPLANAR[™] MegaBuck™ Dual Cool™ EcoSPARK® MicroEET* EfficientMax™ MicroPak™ ESBC™ MicroPak2™ B MillerDrive™ MotionMax™ Fairchild Motion-SPM™ Fairchild Semiconductor® mWSaver™ FACT Quiet Series™ OptoHiT™ FACT **OPTOLOGIC®** FAST[®] **OPTOPLANAR®** FastvCore™ **FETBench™** FlashWriter®*

Global Power Resource^{s#} Green FPS™ e-Series™ MICROCOUPLER™

Power-SPM™ PowerTrench[®] PowerXS™ Programmable Active Droop™ OFFT OST# Quiet Series™ RapidConfigure™ Saving our world, 1mW/W/kW at a time™ SignalWise™ SmartMax™ SMART START™ SPM® STEALTH™ SuperFET SuperSOT™-3 SuperSOT™-6 SuperSOT™-8 SupreMOS® SyncFET™ Sync-Lock™

The Power Franchise® The Right Technology for Your Success™

wer franchise TinyBoost™ TinyBuck™ TinyCalc™ TinyLogic[®] TINYOPTOM TinyPower™ TinyPVvM™ TinyWire™ TriFault Detect™ TRUECURRENT®* uSerDes™

UHC Ultra FRFET™ UniFET™ VCXTM VisualMax™ XSTM

* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

PDP SPM™

DISCLAIMER

FPS™

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN, FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

GENERAL SYSTEM

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein

- 1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user
- 2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formati∨e / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.