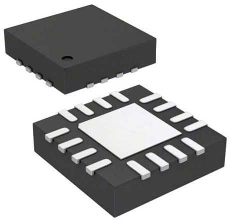
STSPIN240

Low voltage dual brush DC motor driver

Datasheet - production data



QFN 3x3 (16-pin)

Features

- Operating voltage from 1.8 to 10 V
- Maximum output current 1.3 A_{rms}
- $R_{DS(ON)}$ HS + LS = 0.4 Ω typ.
- Current control with programmable off-time
- Full protection set
  - Non-dissipative overcurrent protection
  - Short-circuit protection
  - Thermal shutdown
- Energy saving and long battery life with standby consumption less than 80 nA

Applications

Battery-powered DC motor applications such as:

- Toys
- Portable printers
- Robotics
- Point of sale (POS) devices
- Portable medical equipment
- Healthcare and wellness devices (shavers and toothbrushes)

Description

The STSPIN240 is a dual brush DC motor driver integrating a low $R_{DS(ON)}$ power stage in a small QFN 3x3 package.

Both the full-bridges implement an independent PWM current controller with fixed OFF time.

The device is designed to operate in battery-powered scenarios and can be forced into a zero-consumption state allowing a significant increase in battery life.

The device offers a complete set of protection features including overcurrent, overtemperature and short-circuit protection.

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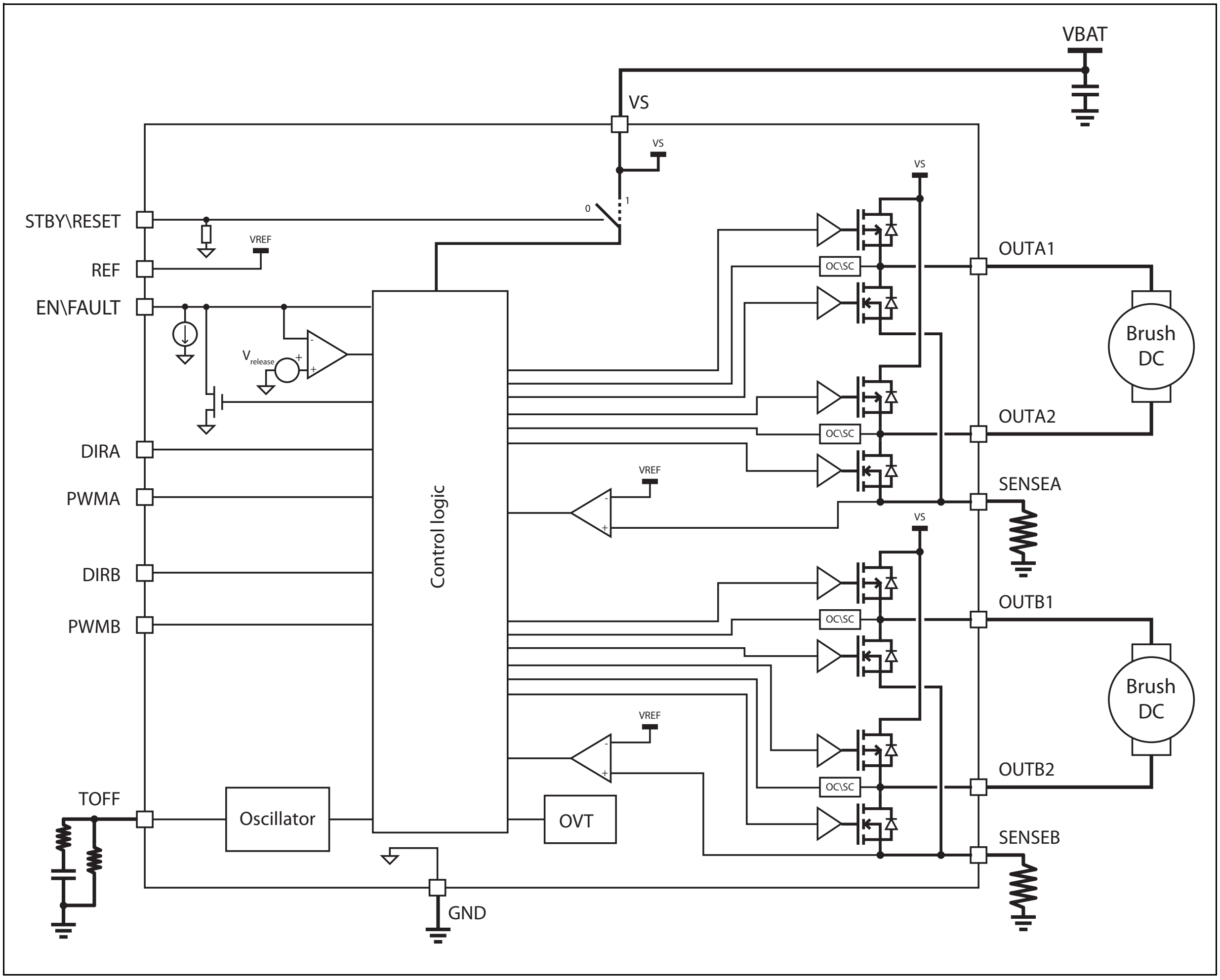
1 Block diagram

Figure 1. Block diagram



2 Electrical data

2.1 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Test condition	Value	Unit
V_S	Supply voltage		-0.3 to 11	V
V_{IN}	Logic input voltage		-0.3 to 5.5	V
V_{OUT} - V_{SENSE}	Output to sense voltage drop		up to 12	V
V_S - V_{OUT}	Supply to output voltage drop		up to 12	V
V_{SENSE}	Sense pins voltage		-1 to 1	V
V_{REF}	Reference voltage input		-0.3 to 1	V
$I_{OUT,RMS}$	Continuous power stage output current (each bridge)		1.3	A_{rms}
$T_{j,OP}$	Operative junction temperature		-40 to 150	°C
$T_{j,STG}$	Storage junction temperature		-55 to 150	°C

2.2 Recommended operating conditions

Table 2. Recommended operating conditions

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_S	Supply voltage		1.8		10	V
V_{IN}	Logic input voltage		0		5	V
V_{REF}	Reference voltage input		0.1		0.5	V

2.3 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(JA)}$	Thermal resistance junction to ambient	TBD	°C/W

2.4 ESD protections

Table 4. ESD protection ratings

Symbol	Parameter	Test condition	Class	Value	Unit
HBM	Human body model	Conforming to ANSI/ESDA/JEDEC JS-001-2014	2	2	kV
CDM	Charge device model	Conforming to ANSI/ESDA/JEDEC JS-002-2014	C2a	500	V

3 Electrical characteristics

Testing conditions: V_S = 5 V, T_j = 25 °C unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply						
$V_{Sth(ON)}$	V_S turn-on voltage	V_S rising from 0 V	1.45	1.65	1.79	V
$V_{Sth(OFF)}$	V_S turn-off voltage	V_S falling from 5 V	1.3	1.45	1.65	V
$V_{Sth(HYS)}$	V_S hysteresis voltage			180		mV
I_S	V_S supply current	No commutations, EN = 0 R_{OFF} = 160 kΩ		960	1300	µA
		No commutations, EN = 1 R_{OFF} = 160 kΩ		1500	1950	µA
$I_{S,STBY}$	V_S standby current	STBY = 0 V		10	80	nA
V_{STBYL}	Standby low logic level input voltage				0.9	V
V_{STBYH}	Standby high logic level input voltage		1.48			V
Power stage						
$R_{DS(ON)HS+LS}$	Total on resistance HS + LS	V_S = 10 V, I_{OUT} = 1.3 A		0.4	0.65	Ω
		V_S = 10 V, I_{OUT} = 1.3 A, T_j = 125 °C(1)		0.53	0.87	
		V_S = 3 V, I_{OUT} = 0.4 A		0.53	0.8	
I_{DSS}	Leakage current	OUTx = V_S			1	µA
		OUTx = GND	- 1			
V_{DF}	Freewheeling diode forward voltage	I_D = 1.3 A		0.9		V
t_{rise}	Rise time	V_S = 10 V; unloaded outputs		10		ns
t_{fall}	Fall time	V_S = 10 V; unloaded outputs		10		ns
t_{DT}	Dead time			50		ns
PWM current controller						
$V_{SNS,OFFSET}$	Sensing offset	V_{REF} = 0.5 V; internal reference 20% V_{REF}	-15		+15	mV
t_{OFF}	Total OFF time	R_{OFF} = 10 kΩ		9		µs
		R_{OFF} = 160 kΩ		125		µs
Δf_{OSC}	Internal oscillator precision ($f_{OSC}/f_{OSC,ID}$)	R_{OFF} = 20 kΩ	-20%		+20%	
$t_{OFF,jitter}$	Total OFF time jittering	R_{OFF} = 10 kΩ			2%	

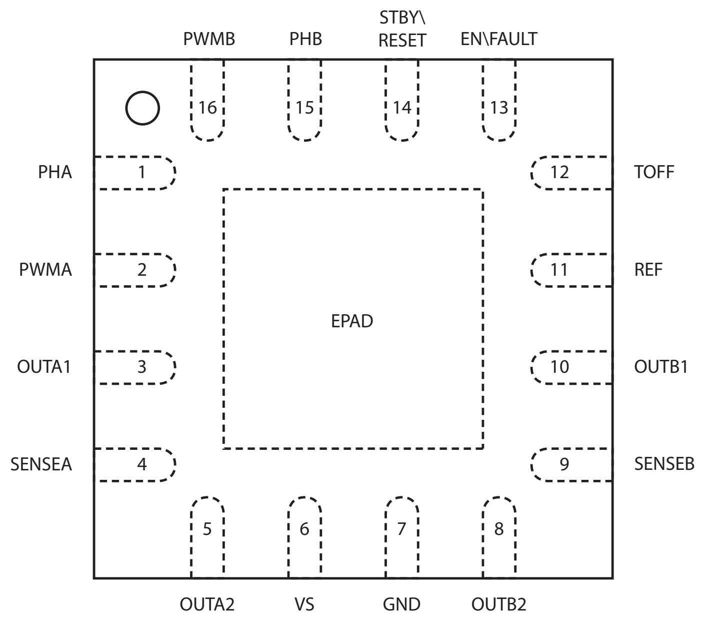
Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Logic IOs						
V_{IH}	High logic level input voltage		1.6			V
V_{IL}	Low logic level input voltage				0.6	V
$V_{RELEASE}$	FAULT open drain release voltage				0.4	V
V_{OL}	Low logic level output voltage	I_{OL} = 4 mA			0.4	V
R_{STBY}	STBY pull-down resistance			36		kΩ
I_{PDEN}	EN pull-down current			10.5		µA
t_{ENd}	EN input propagation delay	From EN falling edge to OUT high impedance		55		ns
$t_{PWM,d(ON)}$	PWMX turn-on propagation delay	See *Figure 4 on page 13*		125		ns
$t_{PWM,d(OFF)}$	PWMX turn-off propagation delay	See *Figure 4*		140		ns
$t_{PH,d}$	PHX propagation delay	See *Figure 4*		125		ns
Protections						
T_{jSD}	Thermal shutdown threshold			160		°C
$T_{jSD,Hyst}$	Thermal shutdown hysteresis			40		°C
I_{OC}	Overcurrent threshold	See *Figure 14 on page 21*		2		A

1. Based on characterization data on a limited number of samples, not tested during production.

4 Pin description

Figure 2. Pin connection (top view)



1. The exposed pad must be connected to ground.

Table 6. Pin description

No.	Name	Type	Function
1	PHA	Logic input	Phase input for bridge A
2	PWMA	Logic input	PWM input for bridge A
3	OUTA1	Power output	Power bridge output side A1
4	SENSEA	Power output	Sense output of the bridge A
5	OUTA2	Power output	Power bridge output side A2
6	VS	Supply	Device supply voltage
7, EPAD	GND	Ground	Device ground
8	OUTB2	Power output	Power bridge output side B2
9	SENSEB	Power output	Sense output of the bridge B
10	OUTB1	Power output	Power bridge output side B1
11	REF	Analog input	Reference voltage for the current limiter circuitry
12	TOFF	Analog input	Internal oscillator frequency adjustment
13	EN\FAULT	Logic input\ open drain output	Logic input 5 V compliant with open drain output. This is the power stage enable (when low, the power stage is turned off) and is forced low through the integrated open drain MOSFET when a failure occurs.

Table 6. Pin description (continued)

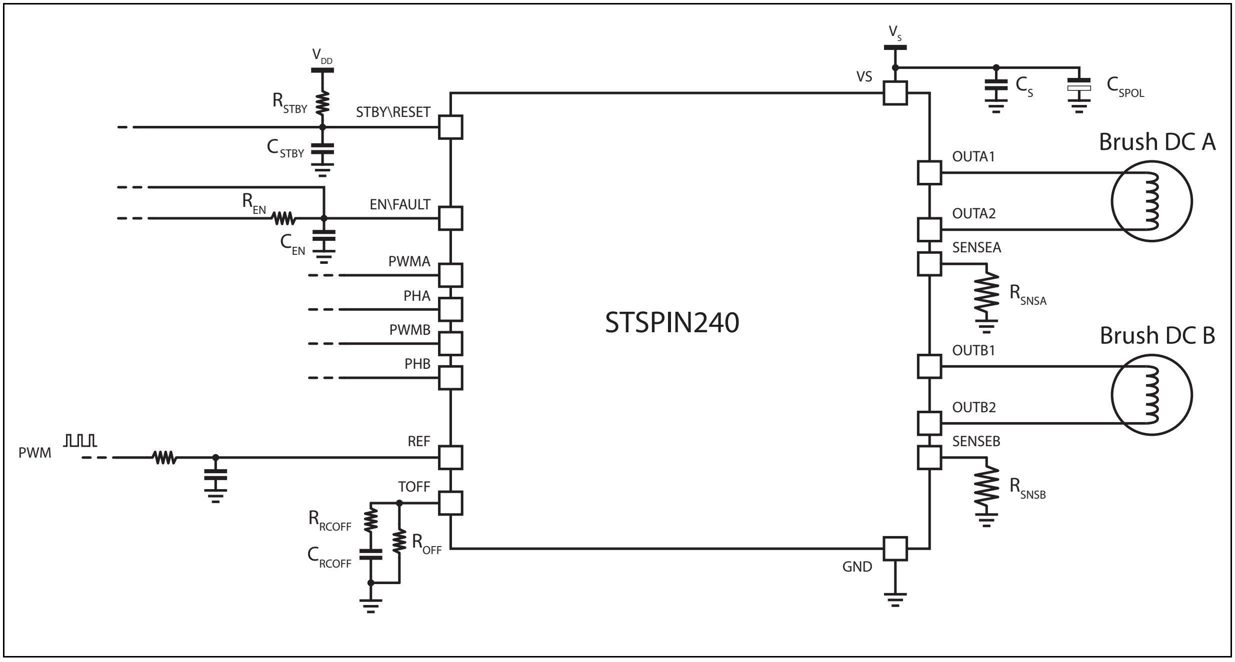
No.	Name	Type	Function
14	STBY\RESET	Logic input	Logic input 5 V compliant. When forced low, the device is forced into low consumption mode.
15	PHB	Logic input	Phase input for bridge B
16	PWMB	Logic input	PWM input for bridge B

5 Typical applications

Table 7. Typical application values

Name	Value
C_S	2.2 µF / 16 V
C_{SPOL}	22 µF / 16 V
R_{SNSA}, R_{SNSB}	330 mΩ / 1 W
C_{EN}	10 nF / 6.3 V
R_{EN}	18 kΩ
C_{STBY}	1 nF / 6.3 V
R_{STBY}	18 kΩ
C_{RCOFF}	22 nF
R_{RCOFF}	1 kΩ
R_{OFF}	47 kΩ ($t_{OFF} \cong$ 37 µs)

Figure 3. Typical application schematic



6 Functional description

The STSPIN240 is a dual brush DC motor driver integrating two PWM current controllers and a power stage composed by two fully-protected full-bridges.

6.1 Standby and power-up

The device provides a low settable consumption mode forcing the STBY\RESET input below the V_{STBYL} threshold.

When the device is in standby status, the power stage is disabled (outputs are in high impedance) and the supply to the integrated control circuitry is cut off.

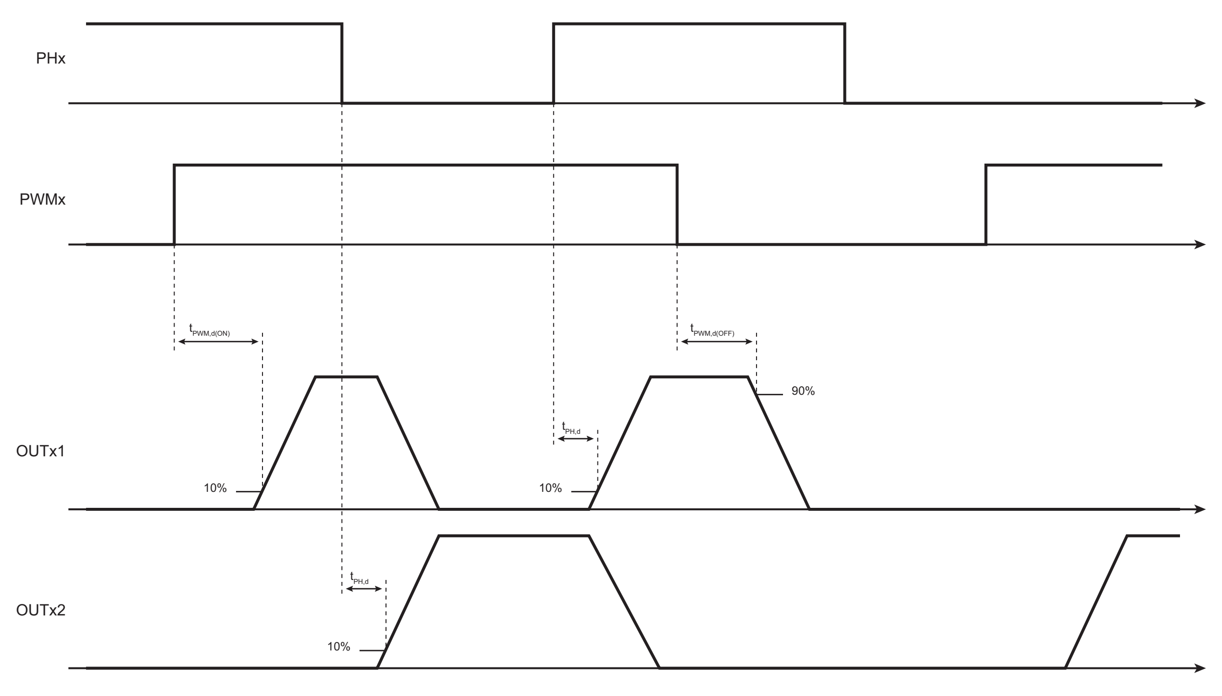
6.2 Motor driving

The outputs of each bridge are controlled by the respective PWMx and PHx inputs as listed in *Table 8*.

Table 8. Truth table

EN\FAULT	PHx	PWMx	OUTx1	OUTx2	Full-bridge condition
0	X	X	HiZ	HiZ	Disabled
1	0	0	GND	GND	Both LS on
1	0	1	GND	VS	HS2 and LS1 on (current X1 ← X2)
1	1	0	GND	GND	Both LS on
1	1	1	VS	GND	HS1 and LS2 on (current X1 → X2)

Figure 4. Timing diagram



6.3 PWM current control

The device implements two independent current controllers, one for each full-bridge.

The voltage on the sense pins (V_{SENSEA} and V_{SENSEB}) is compared to the reference voltage applied on the REF pin (V_{REF}).

When $V_{SENSEX} > V_{REF}$, the current limiter is triggered, the OFF time counter is started and the decay sequence is performed.

The decay sequence starts turning on both low sides of the full-bridge.

Table 9. ON and slow decay states

PHx	PWMx	ON	Decay
0	0	HSx1 = OFF **LSx1 = ON** HSx2 = OFF **LSx2 = ON**	N.A.[1]
0	1	HSx1 = OFF **LSx1 = ON** **HSx2 = ON** LSx2 = OFF	HSx1 = OFF **LSx1 = ON** HSx2 = OFF **LSx2 = ON**
1	0	HSx1 = OFF **LSx1 = ON** HSx2 = OFF **LSx2 = ON**	N.A.[1]
1	1	**HSx1 = ON** LSx1 = OFF HSx2 = OFF **LSx2 = ON**	HSx1 = OFF **LSx1 = ON** HSx2 = OFF **LSx2 = ON**

1. During decays the inputs values are ignored until the system returns to ON condition (decay time expired).

The reference voltage value, V_{REF}, has to be selected according to the load current target value (peak value) and sense resistors value.

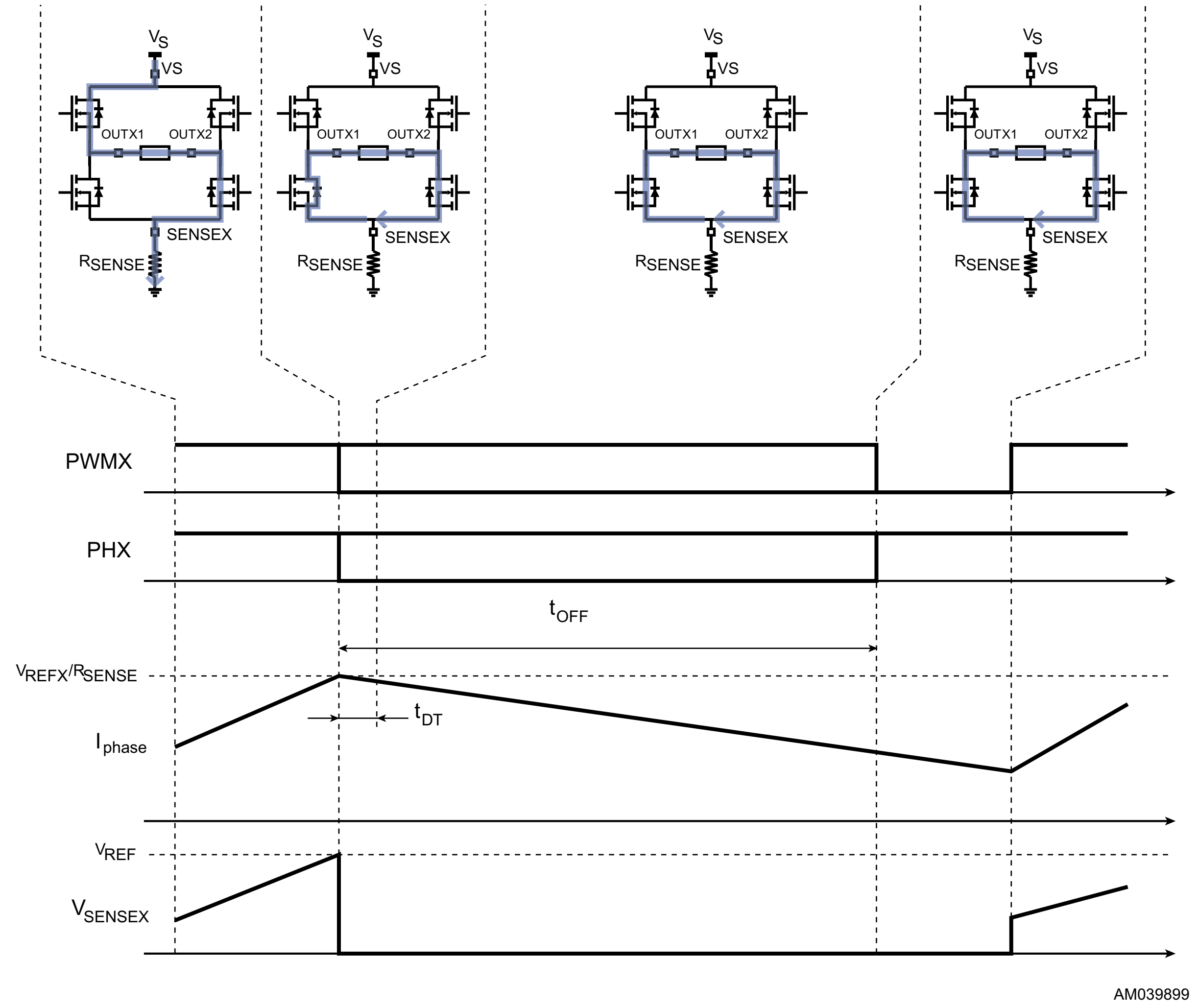
Equation 1

$$V_{REF} = R_{SNSx} \bullet I_{LOAD,peak}$$

In choosing the sense resistor value, two main issues must be taken into account:

- The sensing resistor dissipates energy and provides dangerous negative voltages on the SENSE pins during the current recirculation. For this reason the resistance of this component should be kept low (using multiple resistors in parallel will help to obtain the required power rating with standard resistors).
- The lower is the R_{SNSx} value, the higher is the peak current error due to noise on the V_{REF} pin and to the input offset of the current sense comparator: too low values of R_{SNSx} must be avoided.

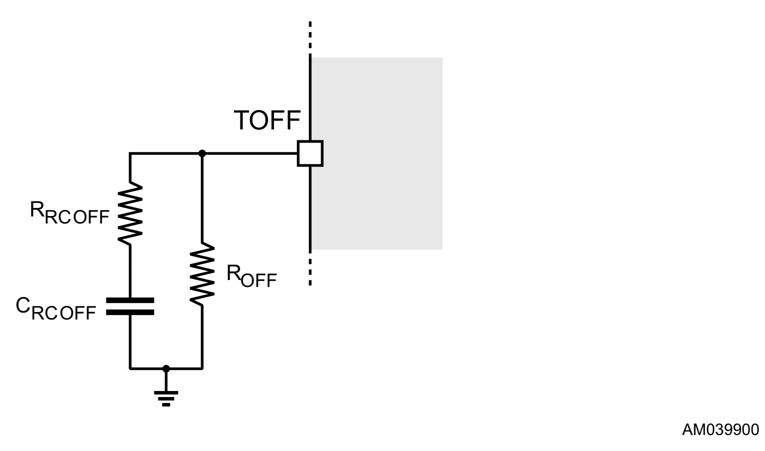
Figure 5. PWM current control



TOFF adjustment

The decay time is adjusted through an external resistor connected between the TOFF pin and ground as shown in *Figure 6*. A small RC series must be inserted in parallel with the regulator resistor in order to increase the stability of the regulation circuit according to indications listed in *Table 10*.

Figure 6. OFF time regulation circuit

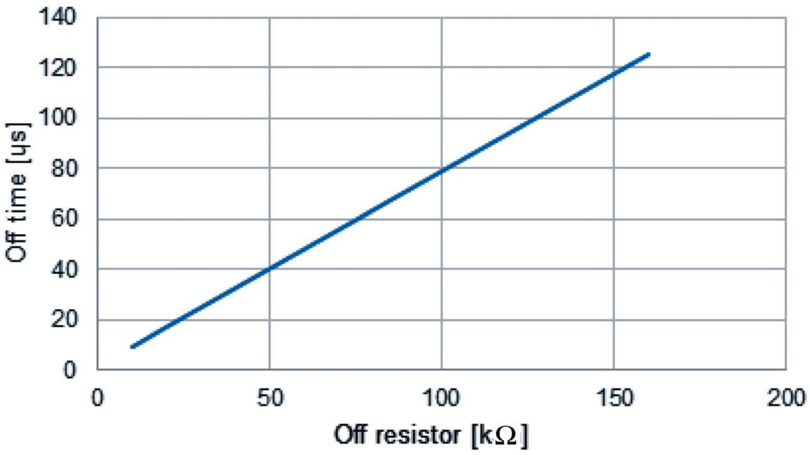


The relation between the OFF time and the external resistor value is shown in the graph of *Figure 7*. The value typically ranges from 10 µs to 150 µs.

Table 10. Recommended R_{RCOFF} and C_{RCOFF} values according to R_{OFF}

R_{OFF}	R_{RCOFF}	C_{RCOFF}
10 kΩ ≤ R_{OFF} < 82 kΩ	1 kΩ	22 nF
82 kΩ ≤ R_{OFF} ≤ 160 kΩ	2.2 kΩ	22 nF

Figure 7. OFF time vs. R_{OFF} value



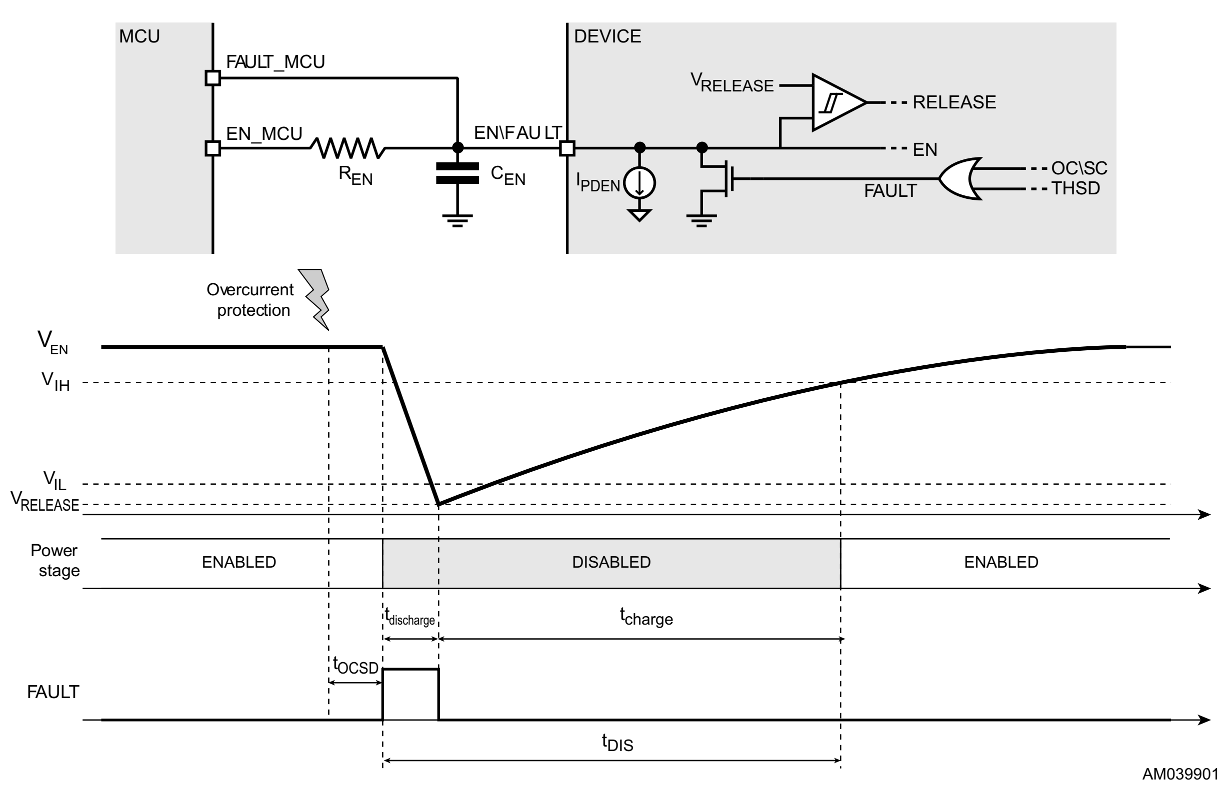
6.4 Overcurrent and short-circuit protections

The device embeds circuitry protecting each power output against the overload and short-circuit conditions (short to ground, short to VS and short between outputs).

When the overcurrent or the short-circuit protection is triggered, the power stage is disabled and the EN\FAULT input is forced low through the integrated open drain MOSFET discharging the external C_{EN} capacitor.

The power stage is kept disabled and the open drain MOSFET is kept ON until the EN\FAULT input falls below the $V_{RELEASE}$ threshold, then the C_{EN} capacitor is charged through the R_{EN} resistor.

Figure 8. Overcurrent and short-circuit protections management



The total disable time after an overcurrent event can be set by properly sizing the external network connected to the EN\FAULT pin (refer to *Figure 9* and *Figure 10*):

Equation 2

$$t_{DIS} = t_{discharge} + t_{charge}$$

But t_{charge} is normally much higher than $t_{discharge}$, thus we can consider only the second one contribution:

Equation 3

$$t_{DIS} \cong R_{EN} \cdot C_{EN} \cdot ln \frac{(V_{DD} - R_{EN} \cdot I_{PDEN}) - V_{RELEASE}}{(V_{DD} - R_{EN} \cdot I_{PDEN}) - V_{IH}}$$

Where V_{DD} is the pull-up voltage of the R_{EN} resistor.

Figure 9. Disable time versus R_{EN} and C_{EN} values (V_{DD} = 3.3 V)

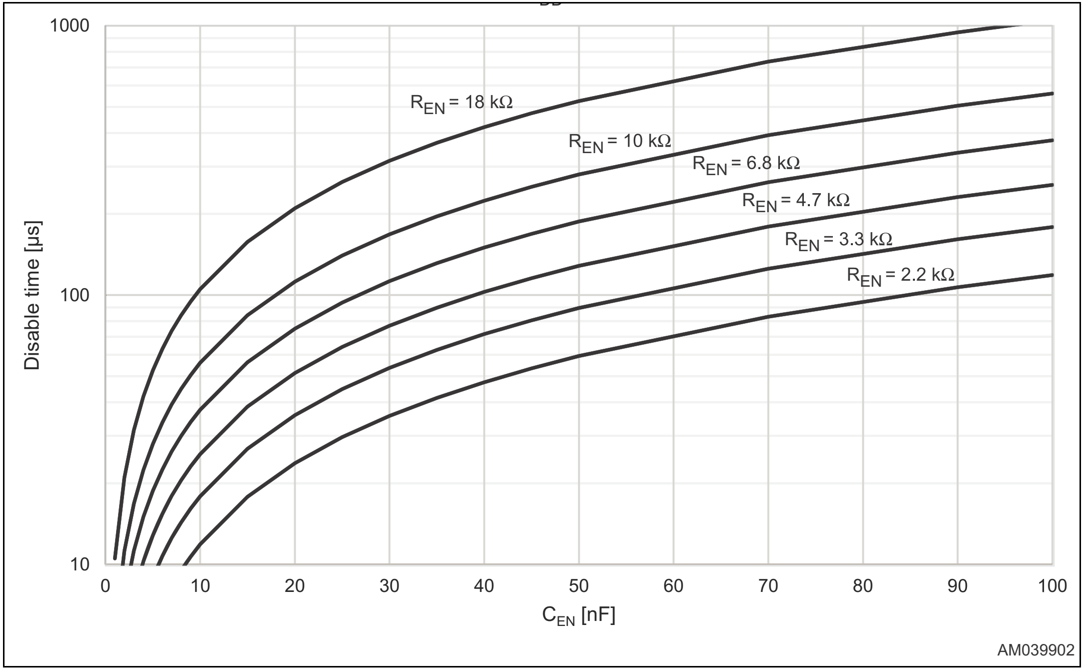
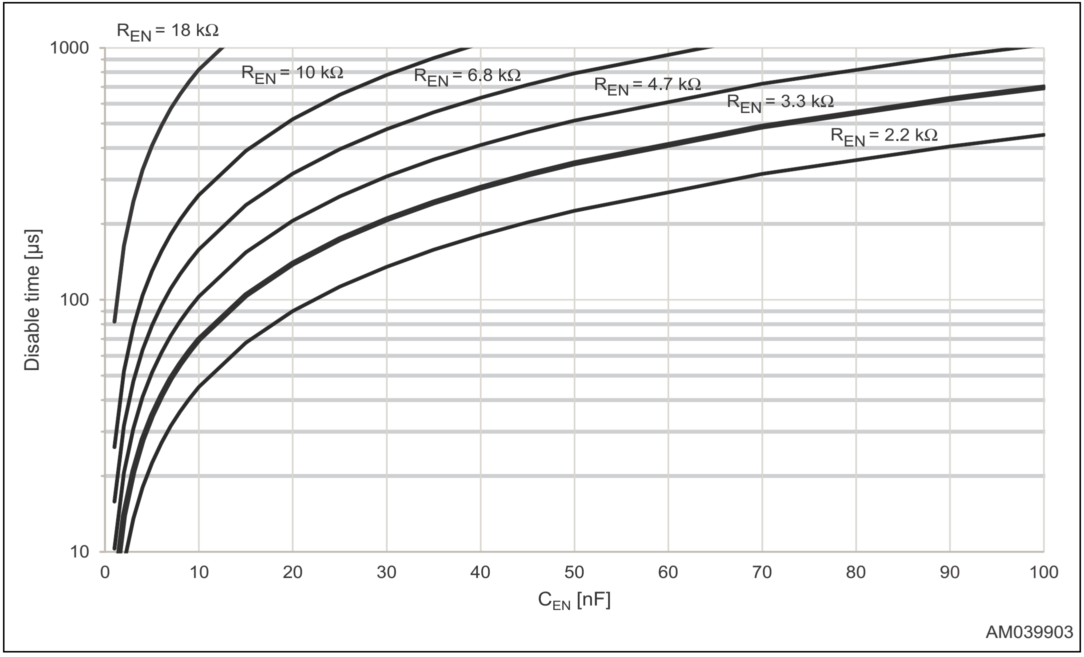


Figure 10. Disable time versus R_{EN} and C_{EN} values (V_{DD} = 1.8 V)



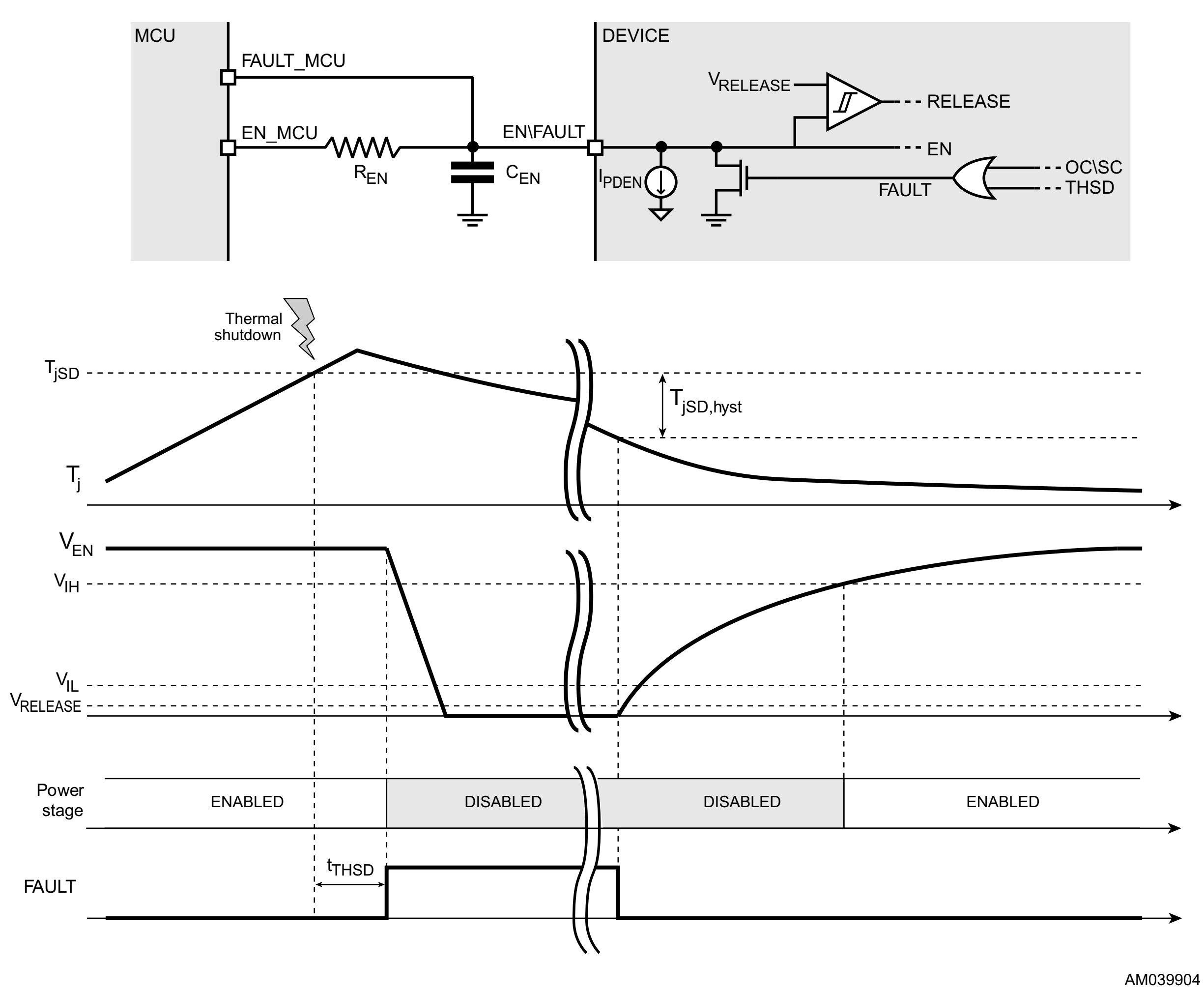
6.5 Thermal shutdown

The device embeds circuitry protecting it from overtemperature conditions.

When the thermal shutdown temperature is reached, the power stage is disabled and the EN\FAULT input is forced low through the integrated open drain MOSFET.

The protection and the EN\FAULT output are released when the IC temperature returns below a safe operating value (T_{jSD} - $T_{jSD,Hyst}$).

Figure 11. Thermal shutdown management



7 Graphs

Figure 12. Power stage resistance versus supply voltage (normalized at V_S = 5 V)

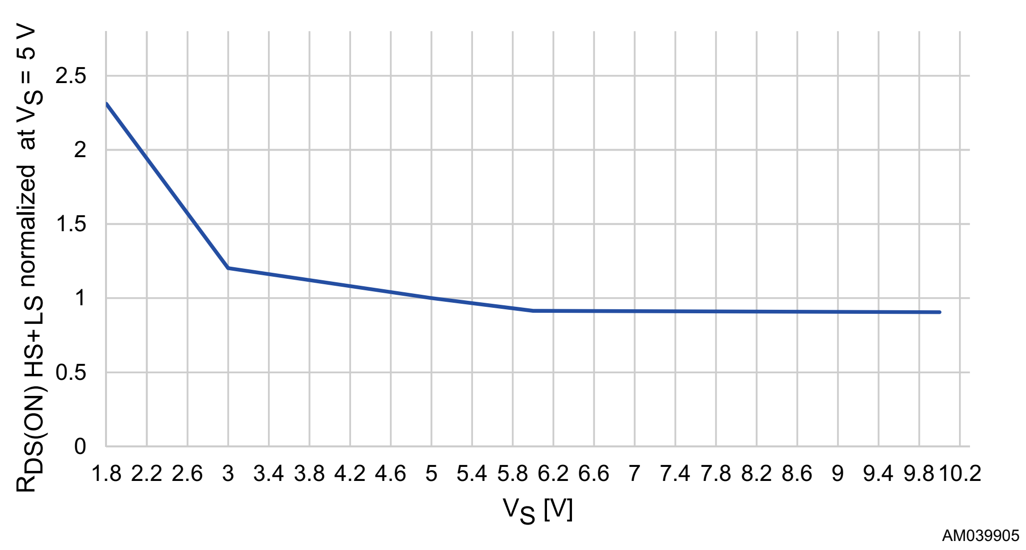


Figure 13. Power stage resistance versus temperature (normalized at T = 25 °C)

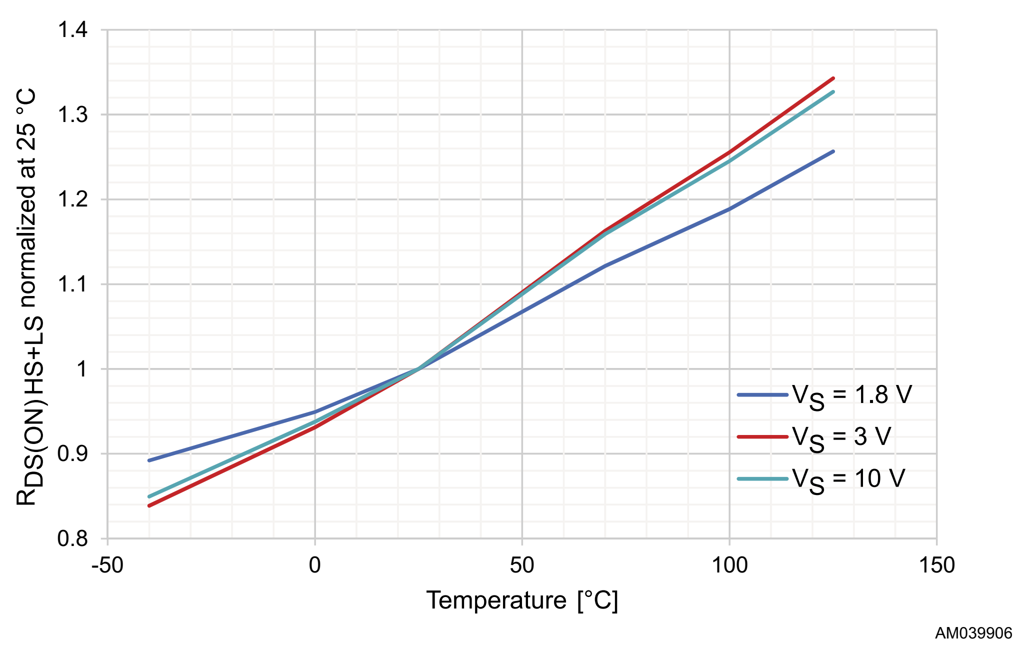
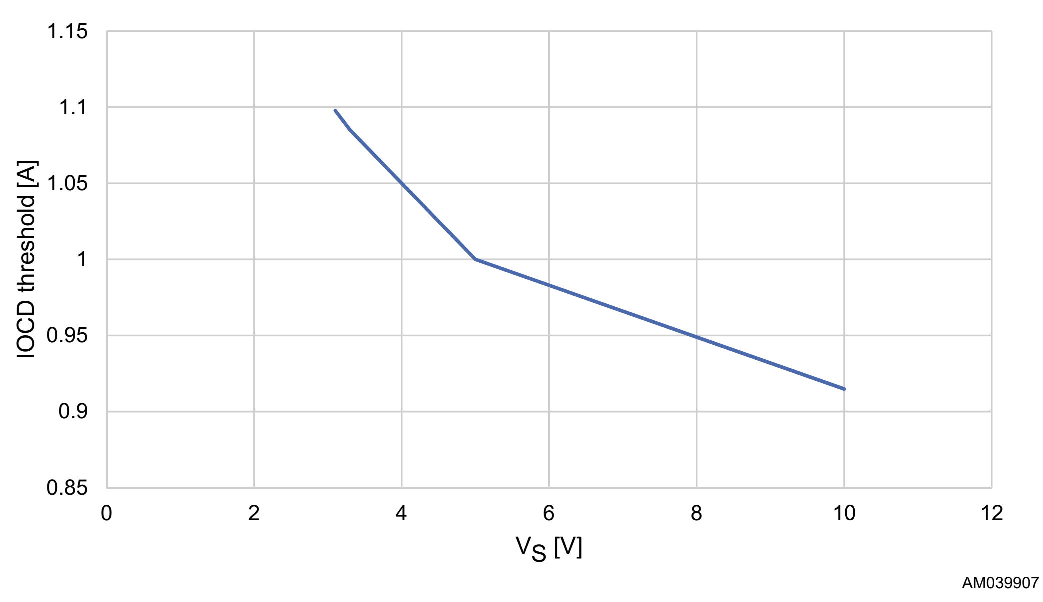


Figure 14. Overcurrent threshold versus supply voltage (normalized at V_S = 5 V)



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

8.1 VFQFPN 3x3x1.0 16L package information

Figure 15. VFQFPN 3x3x1.0 16L package outline

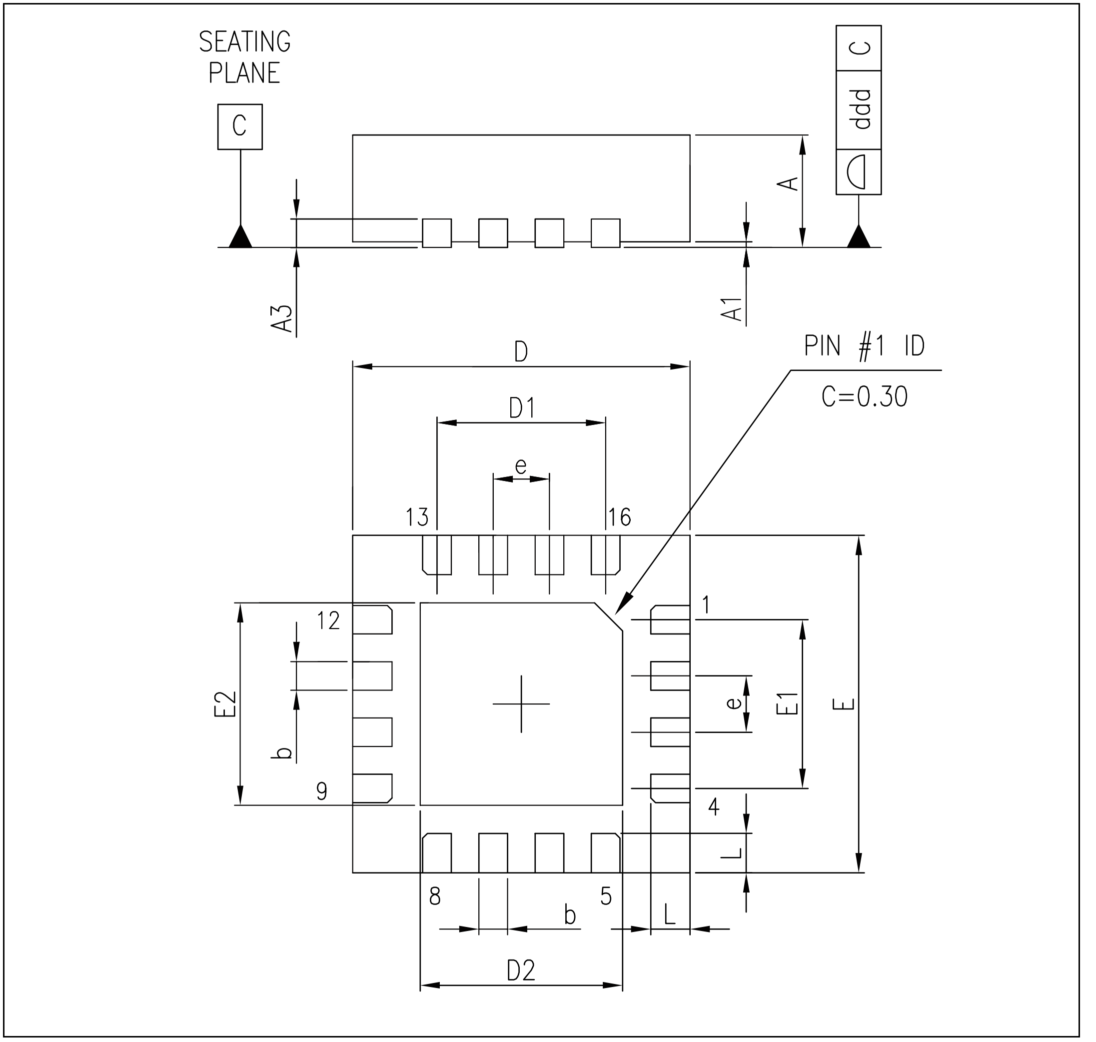
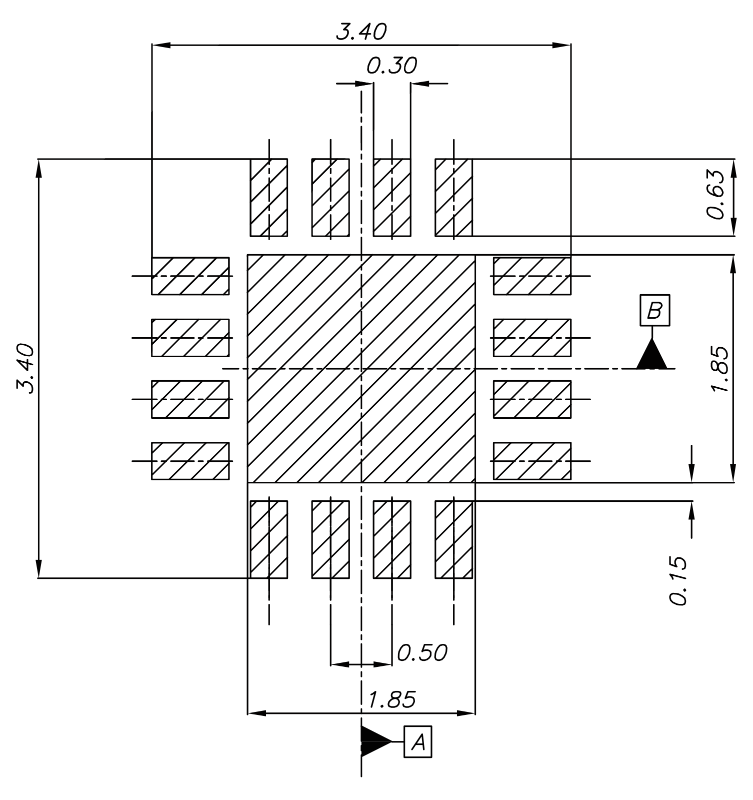


Table 11. VFQFPN 3x3x1.0 16L package mechanical data

Symbol	Dimensions (mm)			NOTES
	Min.	Typ.	Max.	
A	0.80	0.90	1.00	(1)
A1		0.02		
A3		0.20		
b	0.18	0.25	0.30	
D	2.85	3.00	3.15	
D2	1.70	1.80	1.90	
E	2.85	3.00	3.15	
E2	1.70	1.80	1.90	
e		0.50		
L	0.45	0.50	0.55	

1. VFQFPN stands for “Thermally Enhanced Very thin Fine pitch Quad Packages No lead”.
Very thin: 0.80 < A ≤ 1.00 mm / fine pitch: e < 1.00 mm.
The pin #1 identifier must be present on the top surface of the package by using an indentation mark or an other feature of the package body.

Figure 16. VFQFPN 3x3x1.0 16L recommended footprint



9 Ordering information

Table 12. Device summary

Order code	Package	Packaging
STSPIN240	VFQFPN 3x3x1.0 16L	Tape and reel

10 Revision history

Table 13. Document revision history

Date	Revision	Changes
06-May-2016	1	Initial release.
30-Jun-2016	2	Updated document status to *Datasheet - production data* on page 1. Updated *Table 1 on page 6* (changed Max. value of V_S from 12 to 11). Updated *Table 7 on page 11* (changed value of t_{OFF} from 47 µs to 37 µs).