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August 2014

FCP20N60 / FCPF20N60

N-Channel SuperFET® MOSFET

600 V, 20 A, 190 mΩ

Features

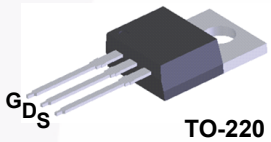
- 650V @ T_J = 150°C
- Typ. $R_{DS(on)}$ = 150 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 75 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 165 pF)
- 100% Avalanche Tested

Applications

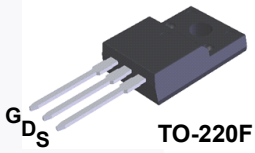
- Solar Inverter
- AC-DC Power Supply

Description

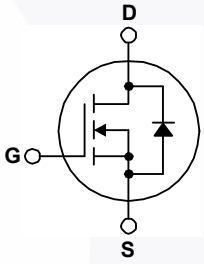
SuperFET® MOSFET is Fairchild Semiconductor's first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.



TO-220



TO-220F



Absolute Maximum Ratings

Symbol	Parameter		FCP20N60	FCPF20N60	Unit
V_{DSS}	Drain-Source Voltage		600		V
I_D	Drain Current	- Continuous (T_C = 25°C) - Continuous (T_C = 100°C)	20 12.5	20* 12.5*	A A
I_{DM}	Drain Current	- Pulsed (Note 1)	60	60*	A
V_{GSS}	Gate-Source Voltage		± 30		V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	690		mJ
I_{AR}	Avalanche Current	(Note 1)	20		A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	20.8		mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5		V/ns
P_D	Power Dissipation - Derate Above 25°C	(T_C = 25°C)	208 1.67	39 0.3	W W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150		°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300		°C

*Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	FCP20N60	FCPF20N60	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.6	3.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	°C/W

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCP20N60	FCP20N60	TO-220	Tube	N/A	N/A	50 units
FCPF20N60	FCPF20N60	TO-220F	Tube	N/A	N/A	50 units

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V, T_J = 25°C	600	-	-	V
		I_D = 250 μA, V_{GS} = 0 V, T_J = 150°C	-	650	-	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	-	0.6	-	V/°C
BV_{DS}	Drain-Source Avalanche Breakdown Voltage	V_{GS} = 0 V, I_D = 20 A	-	700	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 600 V, V_{GS} = 0 V	-	-	1	μA
		V_{DS} = 480 V, T_C = 125°C	-	-	10	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 10 A	-	0.15	0.19	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 10 A	-	17	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	-	2370	3080	pF
C_{oss}	Output Capacitance		-	1280	1665	pF
C_{rss}	Reverse Transfer Capacitance		-	95	-	pF
C_{oss}	Output Capacitance	V_{DS} = 480 V, V_{GS} = 0 V, f = 1 MHz	-	65	85	pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	-	165	-	pF
Q_g	Total Gate Charge at 10V	V_{DS} = 480 V, I_D = 20 A, V_{GS} = 10 V (Note 4)	-	75	98	nC
Q_{gs}	Gate to Source Gate Charge		-	13.5	18	nC
Q_{gd}	Gate to Drain “Miller” Charge		-	36	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 300 V, I_D = 20 A, V_{GS} = 10 V, R_G = 25 Ω (Note 4)	-	62	135	ns
t_r	Turn-On Rise Time		-	140	290	ns
$t_{d(off)}$	Turn-Off Delay Time		-	230	470	ns
t_f	Turn-Off Fall Time		-	65	140	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	20	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	60	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 20 A	-	-	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 20 A, dI_F/dt = 100 A/μs	-	530	-	ns
Q_{rr}	Reverse Recovery Charge		-	10.5	-	μC

Notes:

1: Repetitive rating: pulse-width limited by maximum junction temperature.

2: I_{AS} = 10 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.

3: I_{SD} ≤ 20 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.

4: Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

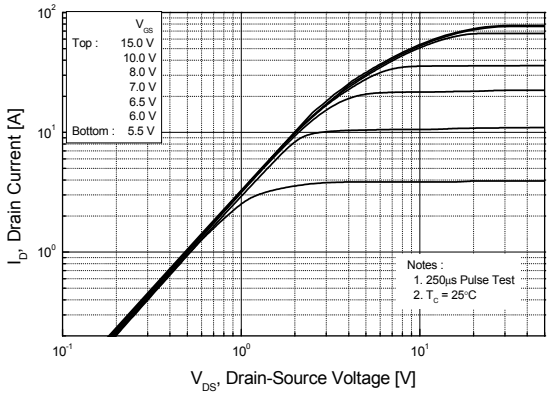


Figure 2. Transfer Characteristics

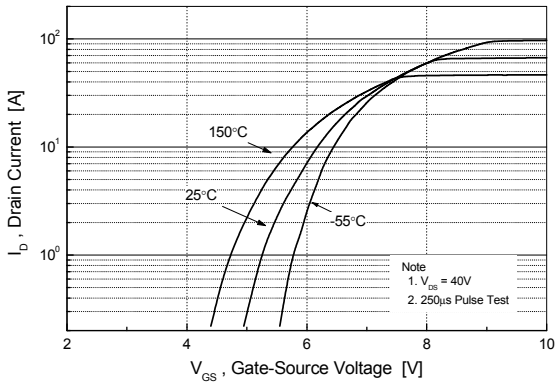


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

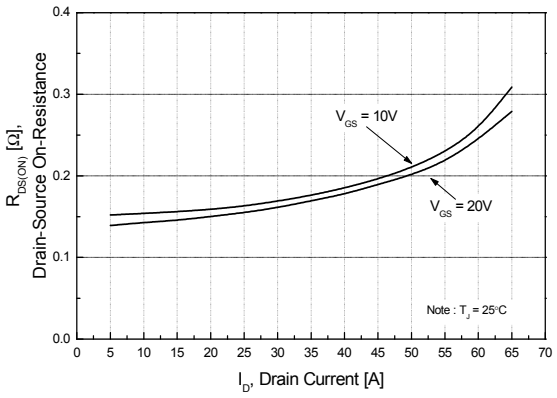


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue

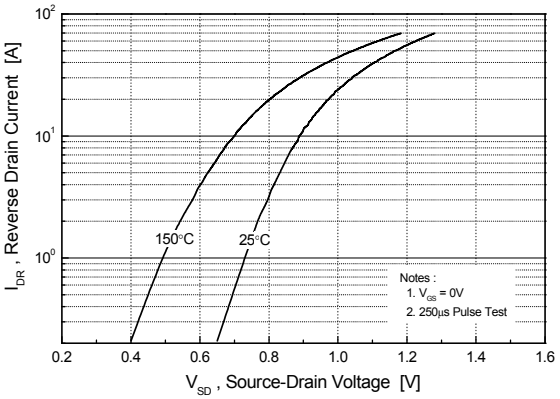


Figure 5. Capacitance Characteristics

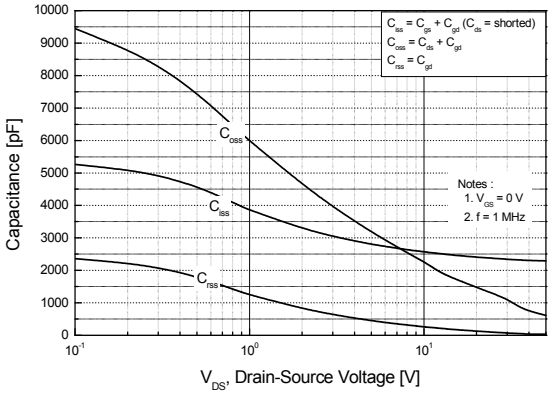
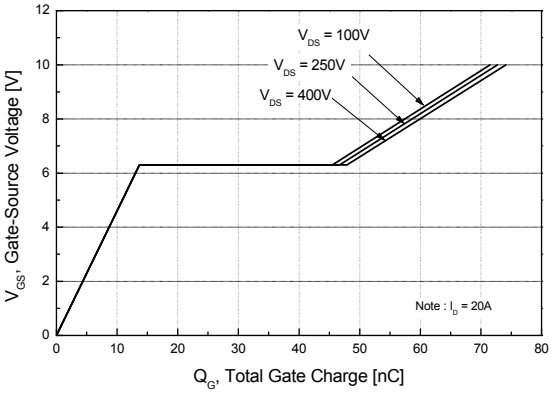


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

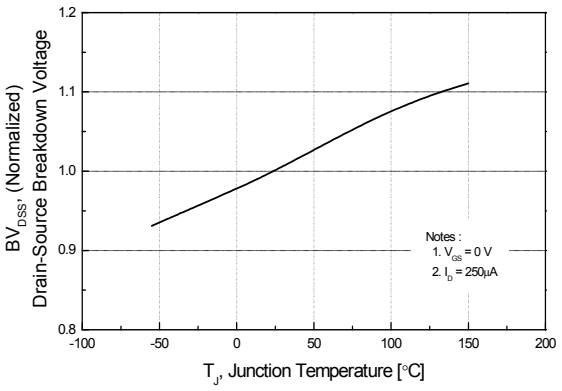


Figure 8. On-Resistance Variation vs. Temperature

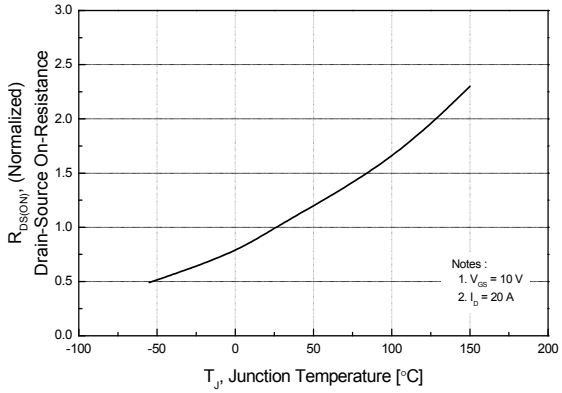


Figure 9-1. Maximum Safe Operating Area for FCP20N60

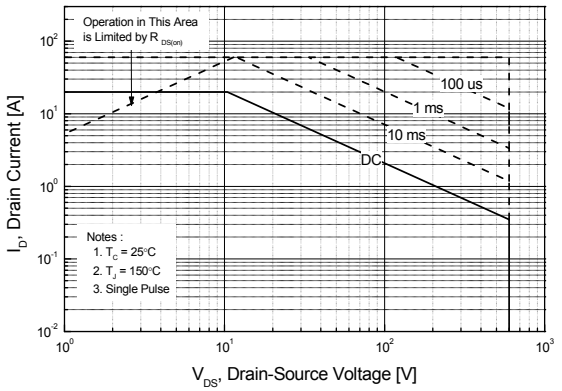


Figure 9-2. Maximum Safe Operating Area for FCPF20N60

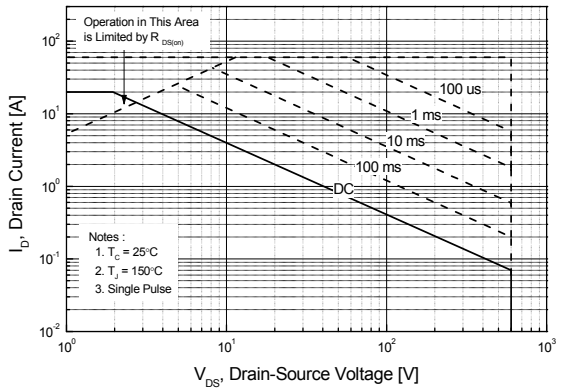
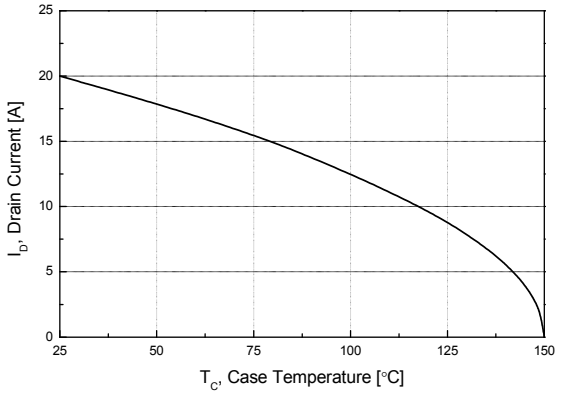


Figure 10. Maximum Drain Current vs. Case Temperature



Typical Performance Characteristics (Continued)

Figure 11-1. Transient Thermal Response Curve for FCP20N60

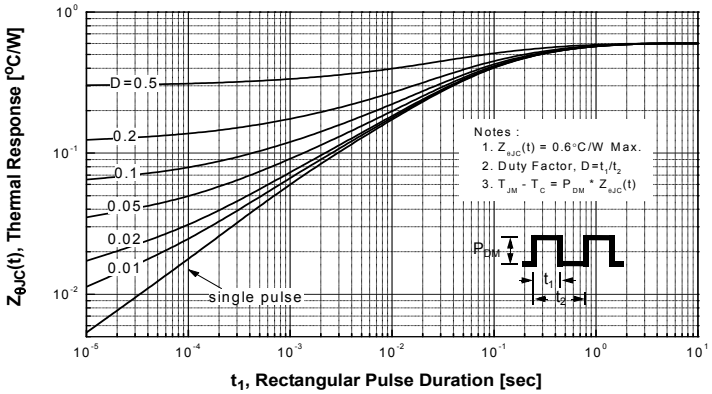
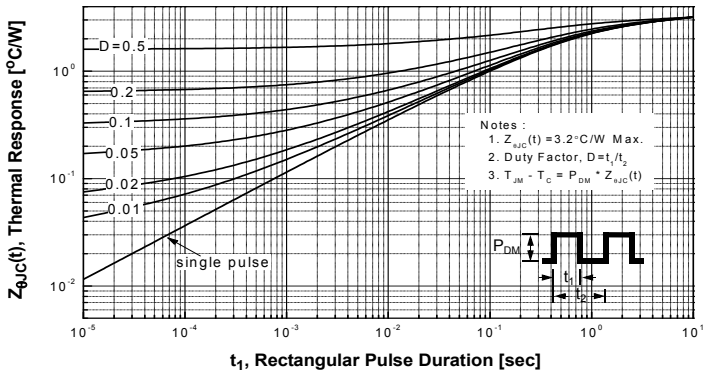


Figure 11-2. Transient Thermal Response Curve for FCPF20N60



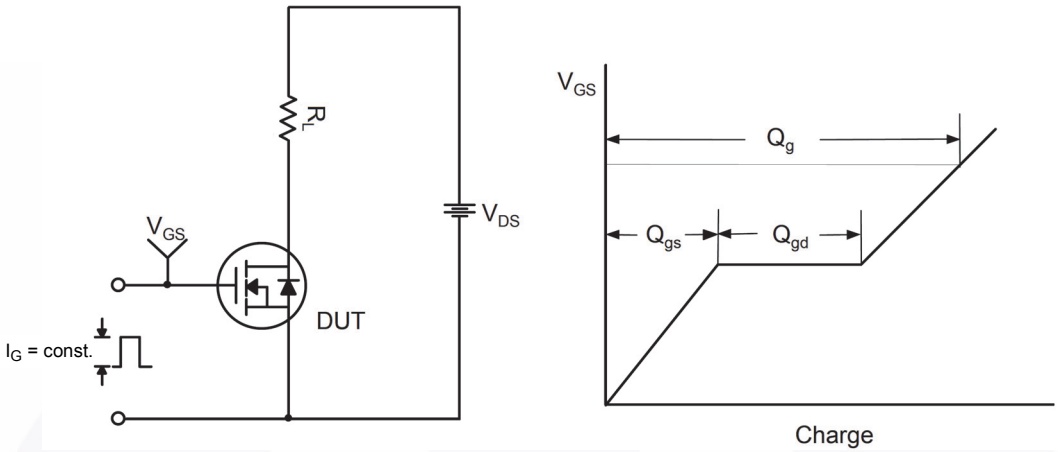


Figure 12. Gate Charge Test Circuit & Waveform

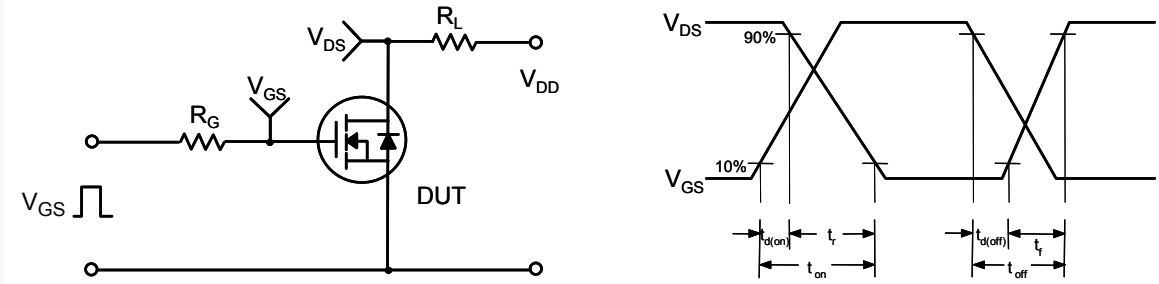


Figure 13. Resistive Switching Test Circuit & Waveforms

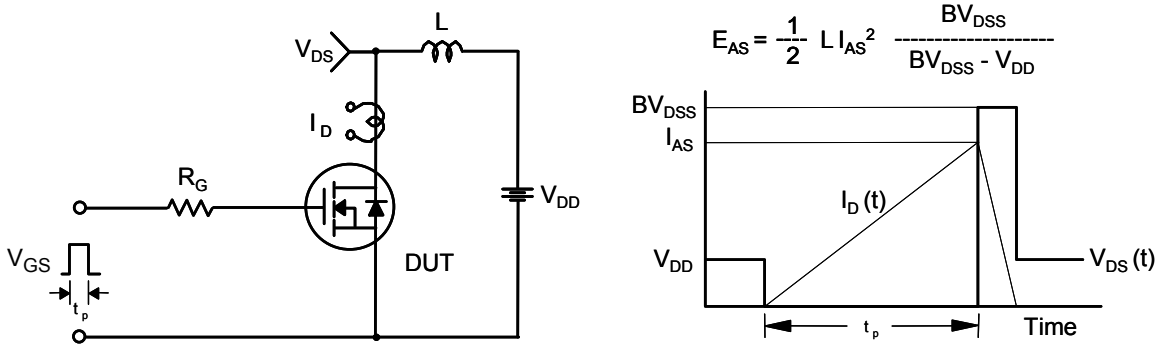


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

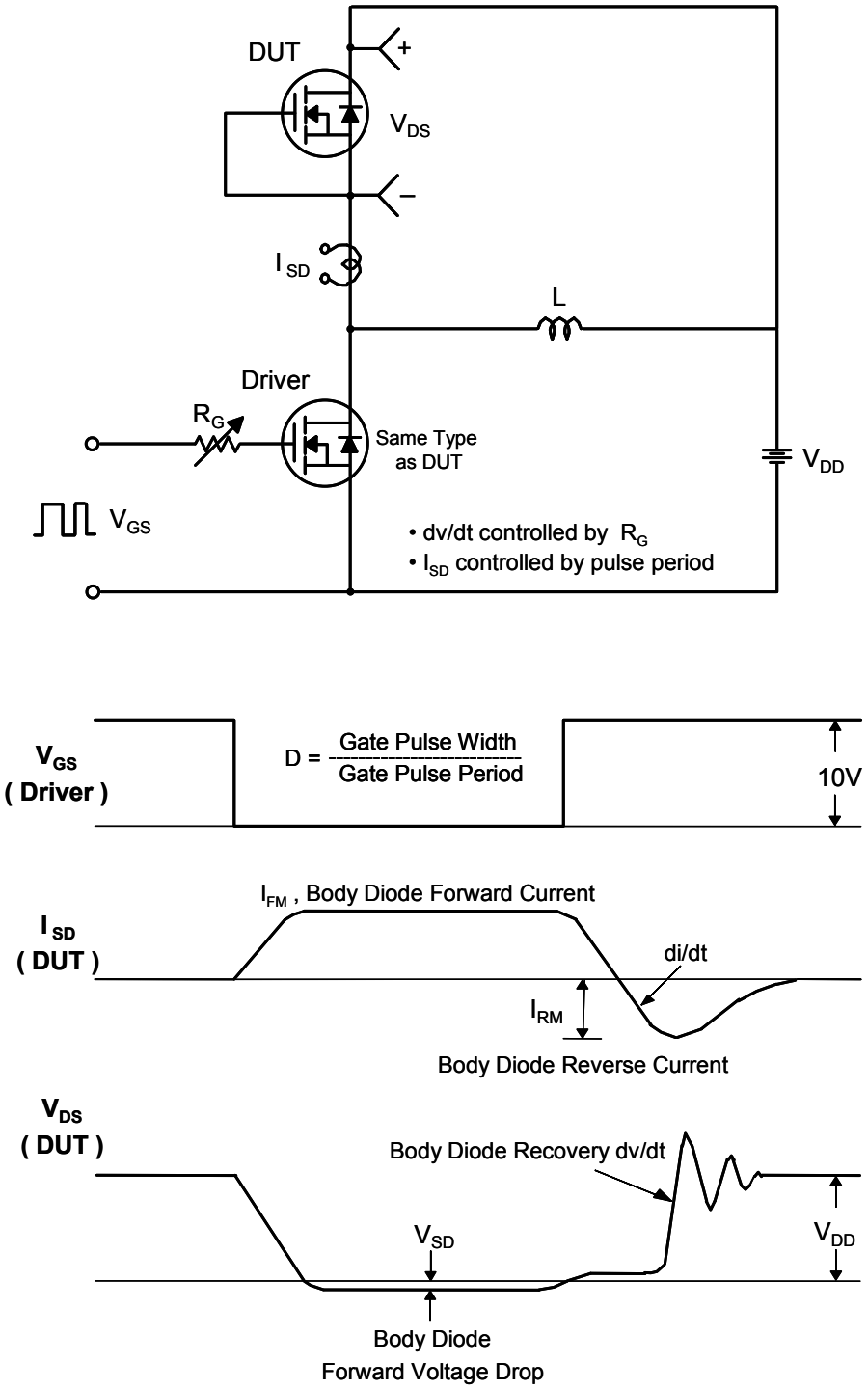
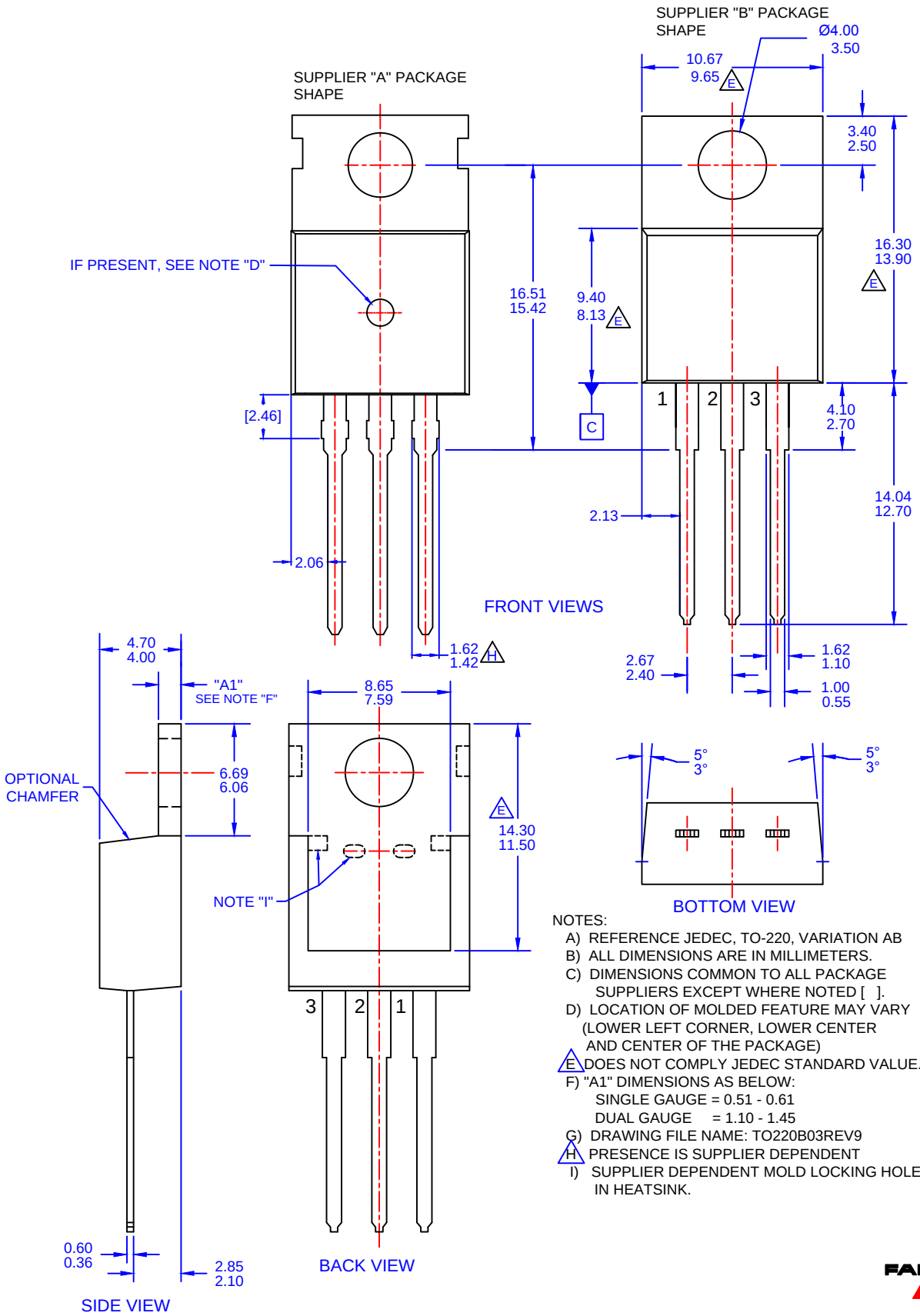


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



NOTES:

A) REFERENCE JEDEC, TO-220, VARIATION AB
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
E DOES NOT COMPLY JEDEC STANDARD VALUE.
F) "A1" DIMENSIONS AS BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1.10 - 1.45
G) DRAWING FILE NAME: TO220B03REV9
H PRESENCE IS SUPPLIER DEPENDENT
I) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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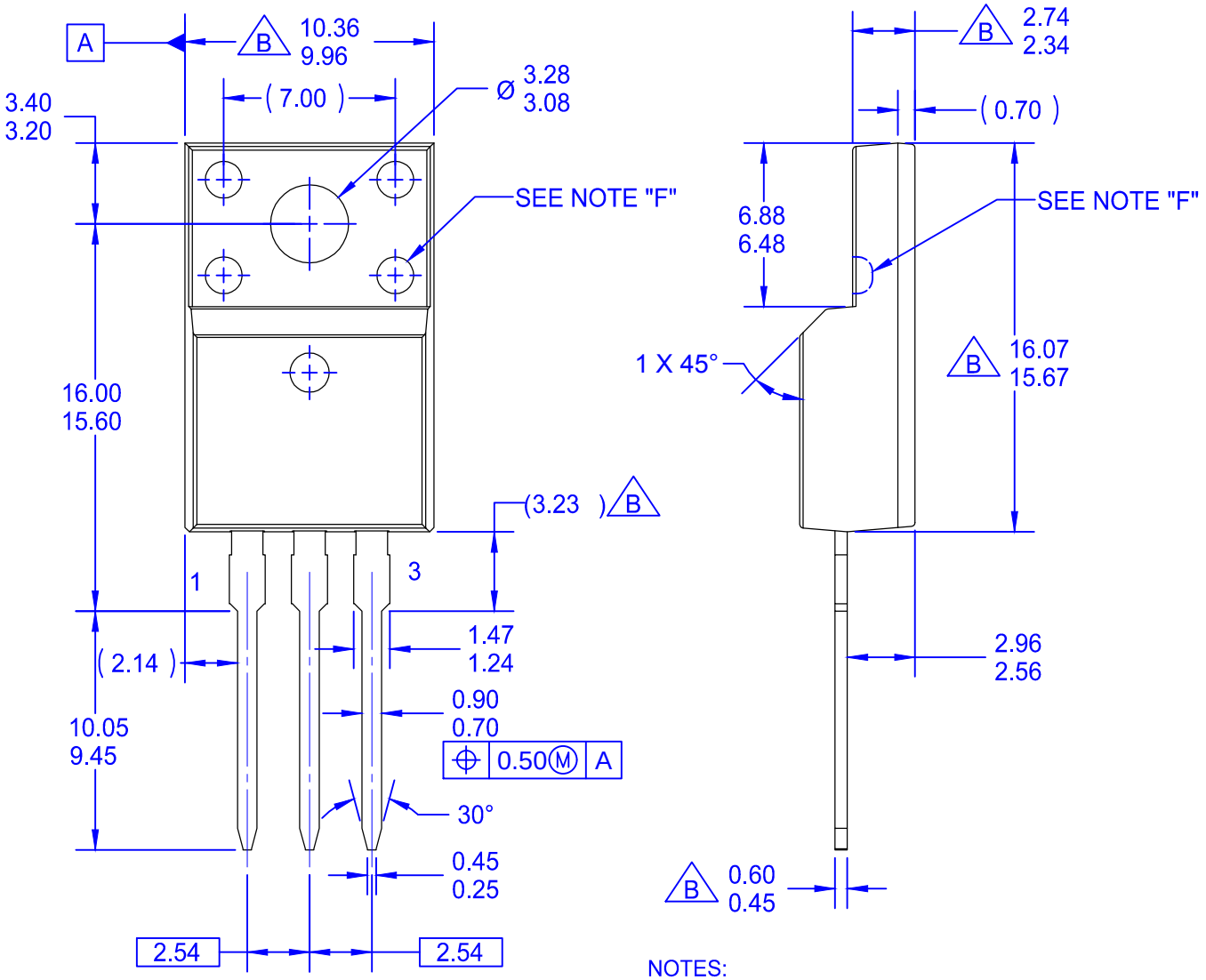

NOTES:

A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
B DOES NOT COMPLY EIAJ STD. VALUE.
C. ALL DIMENSIONS ARE IN MILLIMETERS.
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
F. OPTION 1 - WITH SUPPORT PIN HOLE.
OPTION 2 - NO SUPPORT PIN HOLE.
G. DRAWING FILE NAME: TO220M03REV4

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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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