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March 2015



FDD6612A/FDU6612A

# FDD6612A/FDU6612A

## 30V N-Channel PowerTrench<sup>®</sup> MOSFET

### General Description

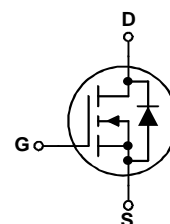
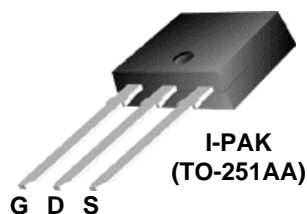
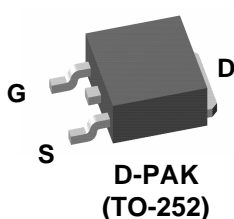
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $R_{DS(ON)}$ , fast switching speed and extremely low  $R_{DS(ON)}$  in a small package.

### Applications

- DC/DC converter
- Motor Drives

### Features

- 30 A, 30 V  $R_{DS(ON)} = 20 \text{ m}\Omega @ V_{GS} = 10 \text{ V}$   
 $R_{DS(ON)} = 28 \text{ m}\Omega @ V_{GS} = 4.5 \text{ V}$
- Low gate charge
- Fast Switching
- High performance trench technology for extremely low  $R_{DS(ON)}$



### Absolute Maximum Ratings

 $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current @ $T_C = 25^\circ\text{C}$ (Note 3)	30	A
	@ $T_A = 25^\circ\text{C}$ (Note 1a)	9.5	
	Pulsed (Note 1a)	60	
$P_D$	Power Dissipation @ $T_C = 25^\circ\text{C}$ (Note 1)	36	W
	@ $T_A = 25^\circ\text{C}$ (Note 1a)	2.8	
	@ $T_A = 25^\circ\text{C}$ (Note 1b)	1.3	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	$-55$ to $+175$	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	3.9	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	45	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1b)	96	$^\circ\text{C/W}$

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape width	Quantity
FDD6612A	FDD6612A	D-PAK (TO-252)	13"	16mm	2500 units
FDU6612A	FDU6612A	I-PAK (TO-251)	Tube	N/A	75

**Electrical Characteristics** $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Drain-Source Avalanche Ratings</b> (Note 2)						
$W_{DSS}$	Drain-Source Avalanche Energy	Single Pulse, $V_{DD} = 27\text{ V}$ , $I_D = 10\text{ A}$			51	mJ
$I_{AR}$	Drain-Source Avalanche Current				10	A
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$		25		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate-Body Leakage	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 100$	nA
<b>On Characteristics</b> (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	1	2.0	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$		-5.1		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 9.5\text{ A}$ $V_{GS} = 4.5\text{ V}$ , $I_D = 8\text{ A}$ $V_{GS} = 10\text{ V}$ , $I_D = 9.5\text{ A}$ , $T_J = 125^\circ\text{C}$		15 20 23	20 28 33	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}$ , $I_D = 9.5\text{ A}$		28		S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		660		pF
$C_{oss}$	Output Capacitance			170		pF
$C_{rss}$	Reverse Transfer Capacitance			90		pF
$R_G$	Gate Resistance	$V_{GS} = 15\text{ Mv}$ , $f = 1.0\text{ MHz}$		2.3		$\Omega$
<b>Switching Characteristics</b> (Note 2)						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}$ , $I_D = 1\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		9	18	ns
$t_r$	Turn-On Rise Time			5	10	ns
$t_{d(off)}$	Turn-Off Delay Time			24	38	ns
$t_f$	Turn-Off Fall Time			4	8	ns
$Q_g$	Total Gate Charge	$V_{DS} = 15\text{ V}$ , $I_D = 9.5\text{ A}$ , $V_{GS} = 5\text{ V}$		6.7	9.4	nC
$Q_{gs}$	Gate-Source Charge			2.1		nC
$Q_{gd}$	Gate-Drain Charge			2.7		nC

# Electrical Characteristics

T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Drain–Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain–Source Diode Forward Current				2.3	A
V <sub>SD</sub>	Drain–Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 2.3 A (Note 2)		0.8	1.2	V
t <sub>rr</sub>	Diode Reverse Recovery Time	IF = 9.5 A, diF/dt = 100 A/μs		20		nS
Q <sub>rr</sub>	Diode Reverse Recovery Charge			10		nC

- Notes:**
- R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design.



a) R<sub>θJA</sub> = 45°C/W when mounted on a 1in<sup>2</sup> pad of 2 oz copper



b) R<sub>θJA</sub> = 96°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

- Maximum current is calculated as: 
$$\sqrt{\frac{P_D}{R_{DS(ON)}}}$$

where P<sub>D</sub> is maximum power dissipation at T<sub>C</sub> = 25°C and R<sub>DS(on)</sub> is at T<sub>J(max)</sub> and V<sub>GS</sub> = 10V. Package current limitation is 21A

## Typical Characteristics

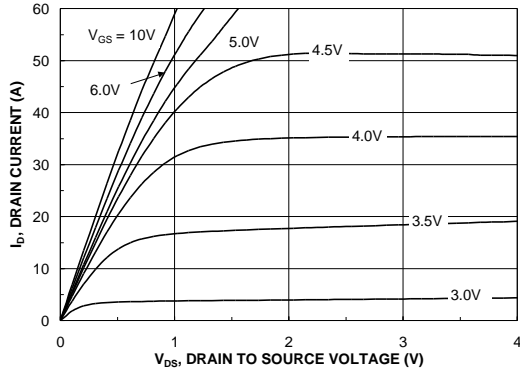


Figure 1. On-Region Characteristics

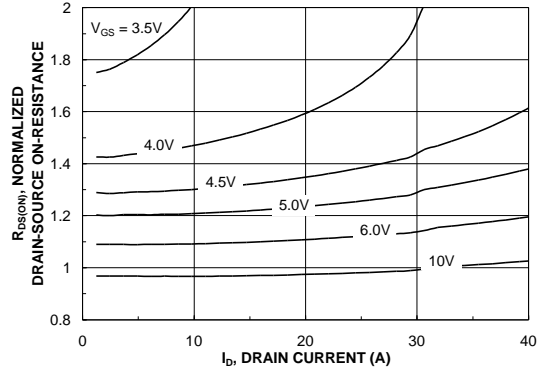


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

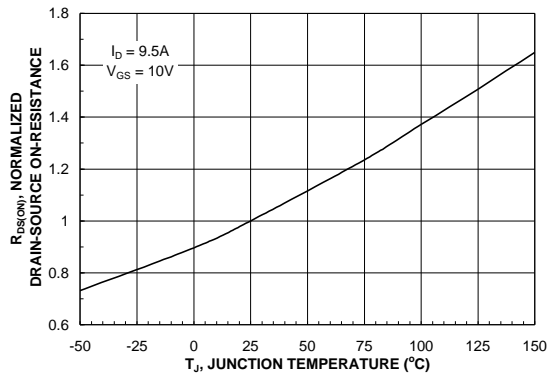


Figure 3. On-Resistance Variation with Temperature

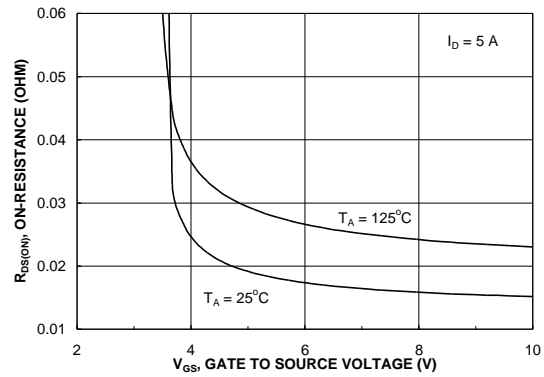


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

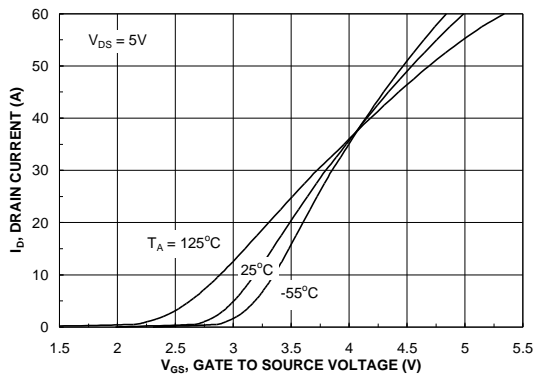


Figure 5. Transfer Characteristics

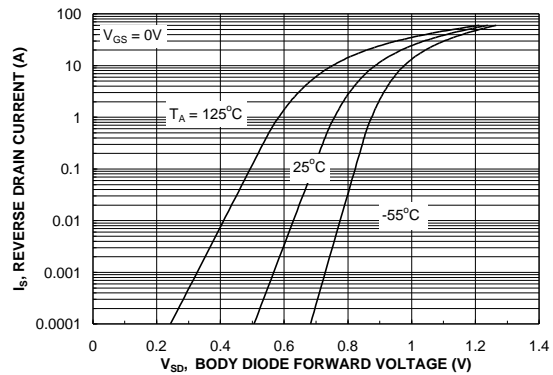


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

## Typical Characteristics

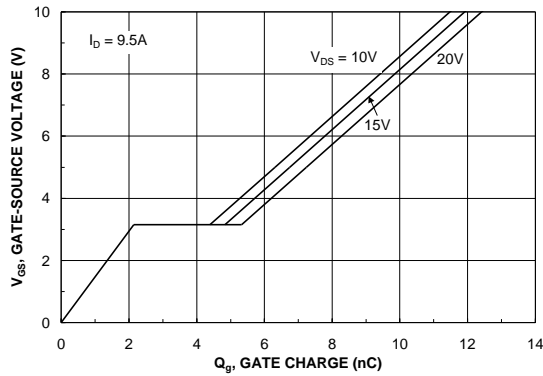


Figure 7. Gate Charge Characteristics

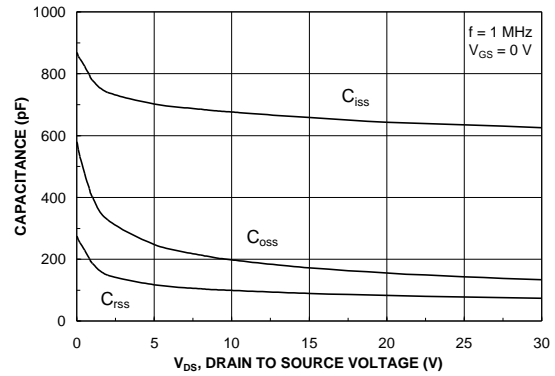


Figure 8. Capacitance Characteristics

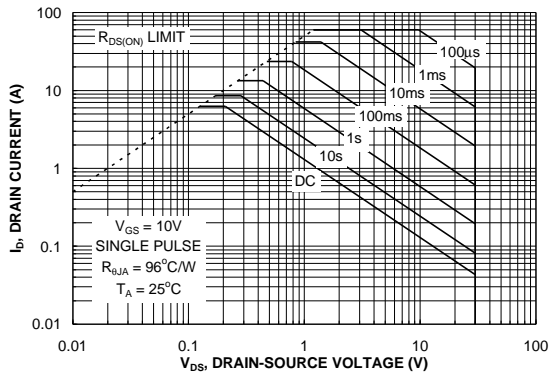


Figure 9. Maximum Safe Operating Area

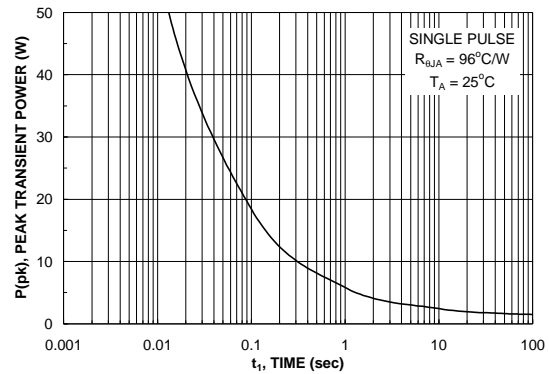


Figure 10. Single Pulse Maximum Power Dissipation

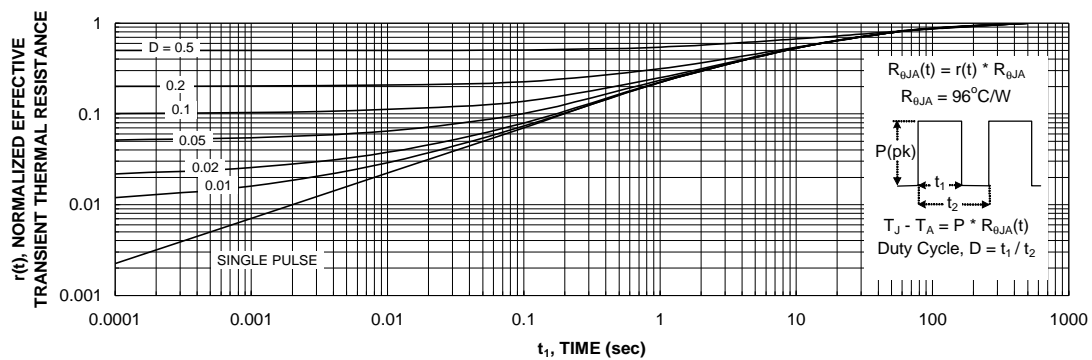
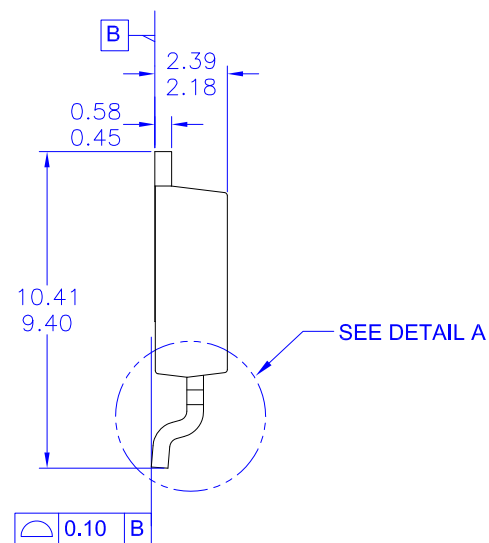
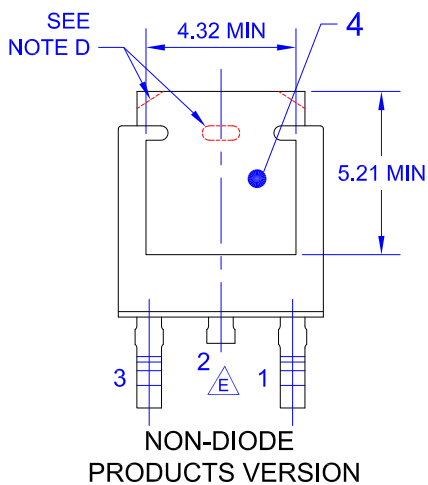
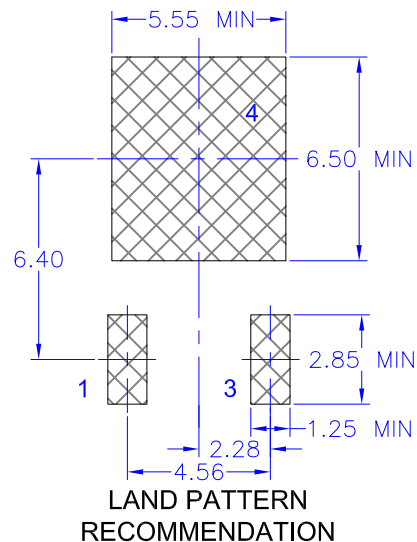
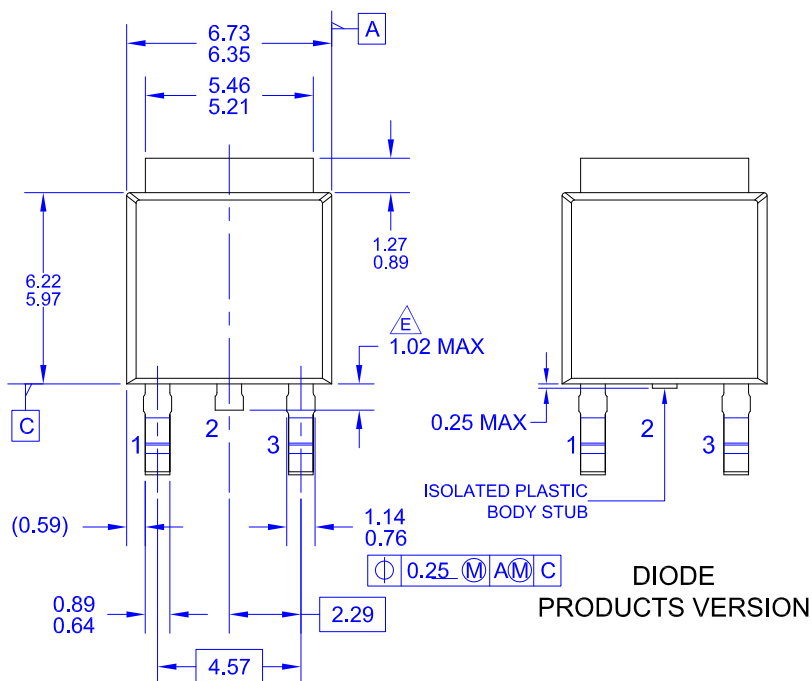


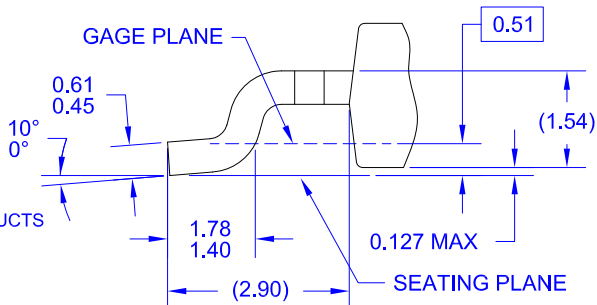
Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1b.  
Transient thermal response will change depending on the circuit board design.



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
- F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
- H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11



DETAIL A  
(ROTATED -90°)  
SCALE: 12X





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