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April 2014

# FQD17P06 / FQU17P06

## P-Channel QFET<sup>®</sup> MOSFET

-60 V, -12 A, 135 mΩ

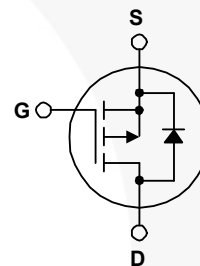
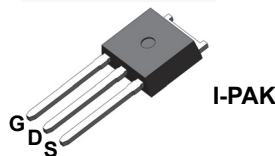
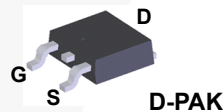


### Description

This P-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

### Features

- -12 A, -60 V,  $R_{DS(on)} = 135 \text{ m}\Omega$  (Max.) @  $V_{GS} = -10 \text{ V}$ ,  $I_D = -6 \text{ A}$
- Low Gate Charge (Typ. 21 nC)
- Low Crss (Typ. 80 pF)
- 100% Avalanche Tested



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQD17P06 / FQU17P06	Unit
$V_{DSS}$	Drain-Source Voltage	-60	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	-12
		- Continuous ( $T_C = 100^\circ\text{C}$ )	-7.6
$I_{DM}$	Drain Current	- Pulsed (Note 1)	-48
$V_{GSS}$	Gate-Source Voltage	$\pm 25$	V
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	300
$I_{AR}$	Avalanche Current	(Note 1)	-12
$E_{AR}$	Repetitive Avalanche Energy	(Note 1)	4.4
$dv/dt$	Peak Diode Recovery $dv/dt$	(Note 3)	-7.0
$P_D$	Power Dissipation ( $T_A = 25^\circ\text{C}$ ) *		2.5
	Power Dissipation ( $T_C = 25^\circ\text{C}$ )		44
	- Derate above $25^\circ\text{C}$		0.35
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds.	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FQD17P06 / FQU17P06	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	2.85	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	110	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (*1 in <sup>2</sup> Pad of 2-oz Copper), Max.	50	

\* When mounted on the minimum pad size recommended (PCB Mount)

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQD17P06TM	FQD17P06	DPAK	Tape and Reel	330 mm	16 mm	2500 units
FQU17P06TU	FQU17P06	IPAK	Tube	N/A	N/A	70 units

## Electrical Characteristics T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA	-60	--	--	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = -250 μA, Referenced to 25°C	--	-0.06	--	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0 V	--	--	-1	μA
		V <sub>DS</sub> = -48 V, T <sub>C</sub> = 125°C	--	--	-10	μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = -25 V, V <sub>DS</sub> = 0 V	--	--	-100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = 25 V, V <sub>DS</sub> = 0 V	--	--	100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	-2.0	--	-4.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -6.0 A	--	0.11	0.135	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = -30 V, I <sub>D</sub> = -6.0 A	--	8.7	--	S
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = -25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	--	690	900	pF
C <sub>oss</sub>	Output Capacitance		--	325	420	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	80	105	pF
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = -30 V, I <sub>D</sub> = -8.5 A, R <sub>G</sub> = 25 Ω  (Note 4)	--	13	35	ns
t <sub>r</sub>	Turn-On Rise Time		--	100	210	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	22	55	ns
t <sub>f</sub>	Turn-Off Fall Time		--	60	130	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = -48 V, I <sub>D</sub> = -17 A, V <sub>GS</sub> = -10 V  (Note 4)	--	21	27	nC
Q <sub>gs</sub>	Gate-Source Charge		--	4.2	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	10	--	nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	-12	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	-48	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -12 A	--	--	-4.0	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -17 A,	--	92	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge	di <sub>F</sub> / dt = 100 A/μs	--	0.32	--	μC

### NOTES:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. L = 2.4 mH, I<sub>AS</sub> = -12 A, V<sub>DD</sub> = -25 V, R<sub>G</sub> = 25 Ω, starting T<sub>J</sub> = 25°C.
3. I<sub>SD</sub> ≤ -17 A, di/dt ≤ 300 A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, starting T<sub>J</sub> = 25°C.
4. Essentially independent of operating temperature typical characteristics.

## Typical Performance Characteristics

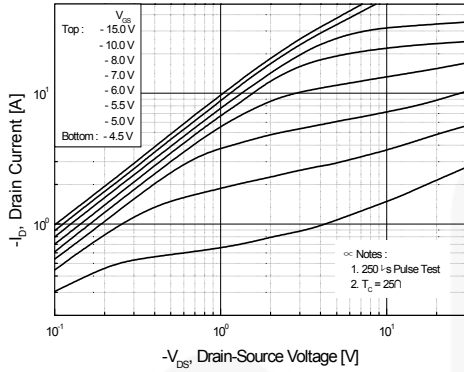


Figure 1. On-Region Characteristics

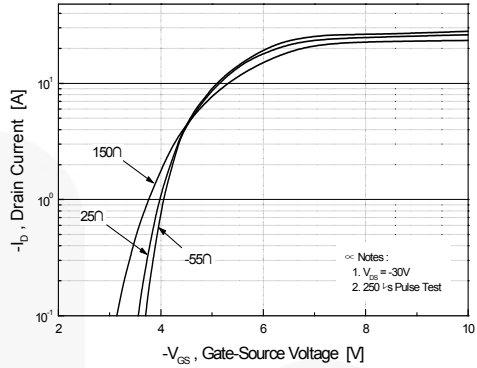


Figure 2. Transfer Characteristics

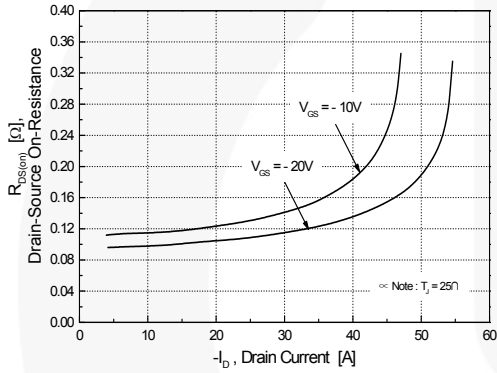


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

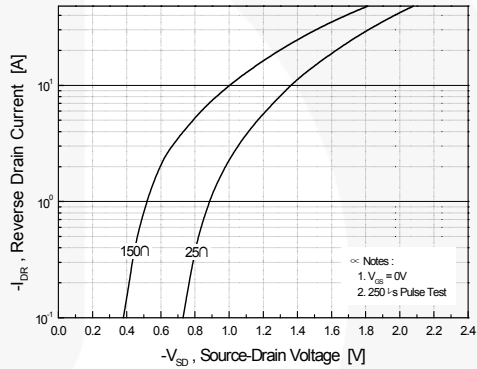


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

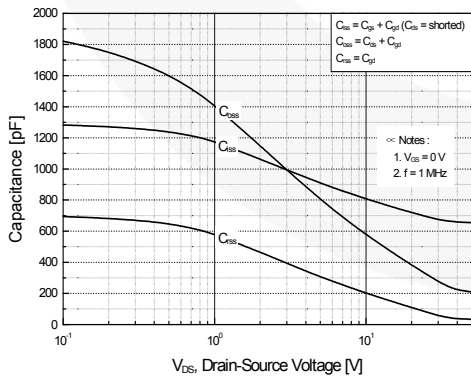


Figure 5. Capacitance Characteristics

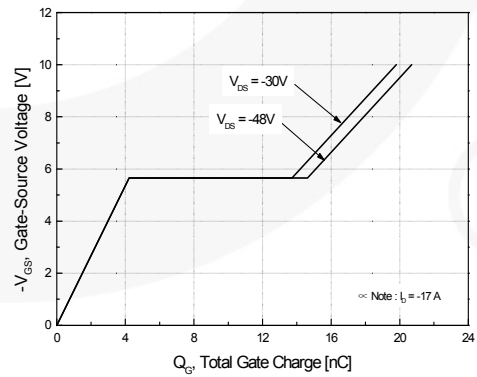
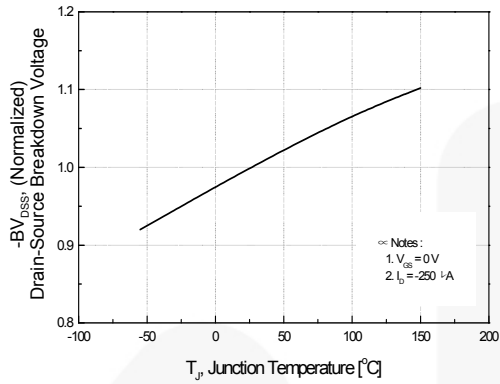
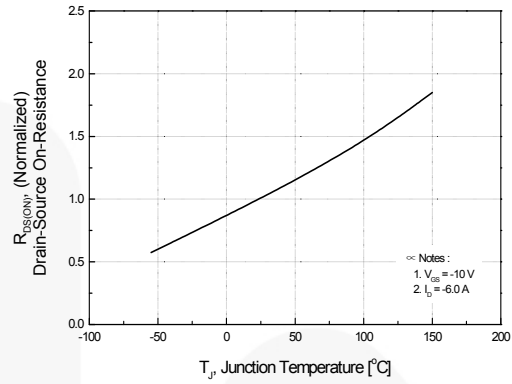


Figure 6. Gate Charge Characteristics

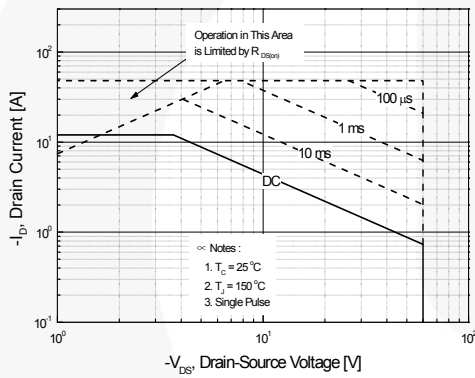
**Typical Performance Characteristics** (Continued)



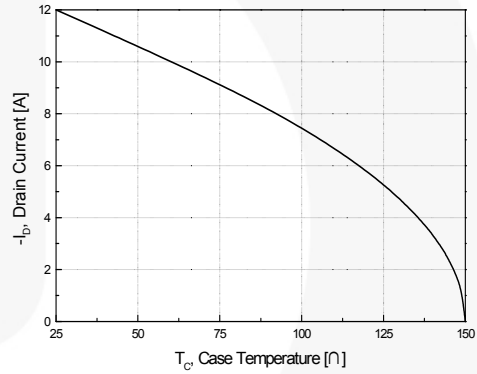
**Figure 7. Breakdown Voltage Variation vs. Temperature**



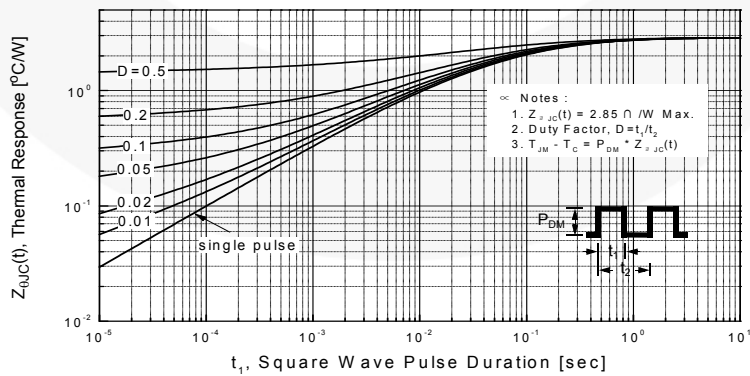
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response Curve**

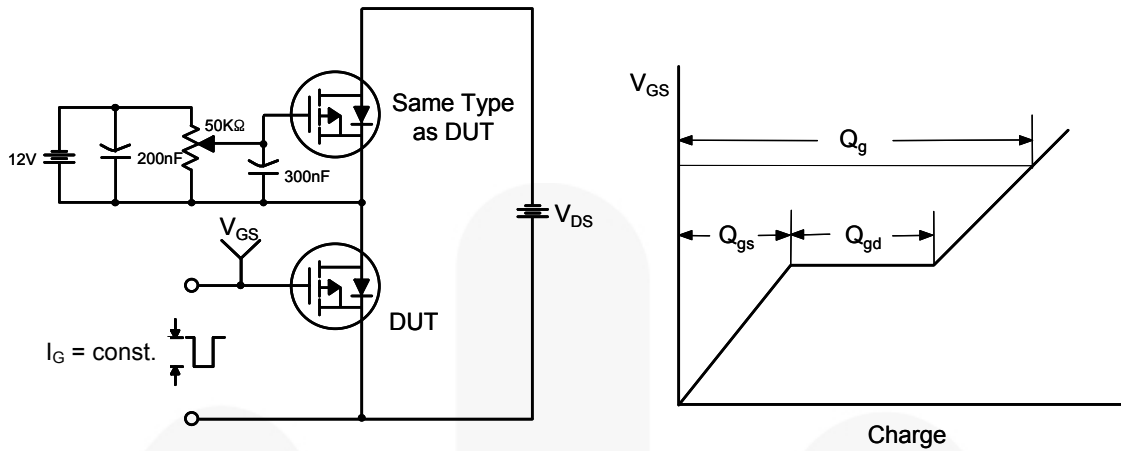


Figure 12. Gate Charge Test Circuit & Waveform

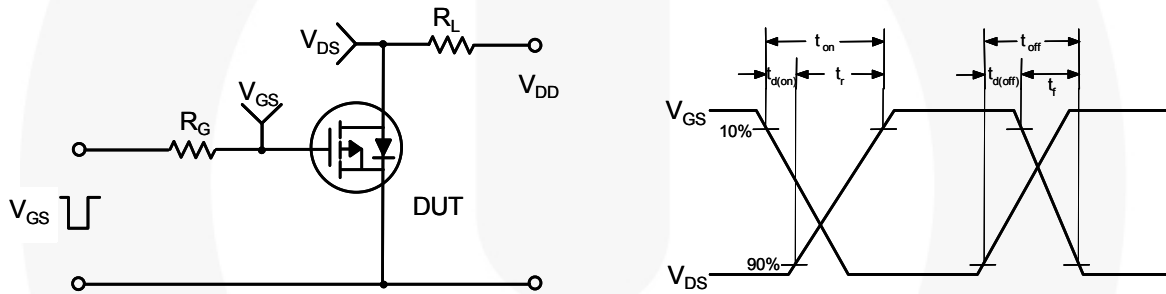


Figure 13. Resistive Switching Test Circuit & Waveforms

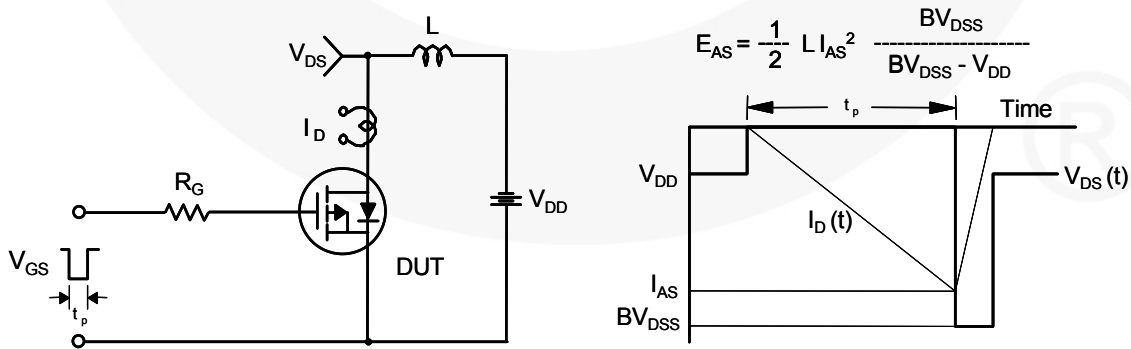


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

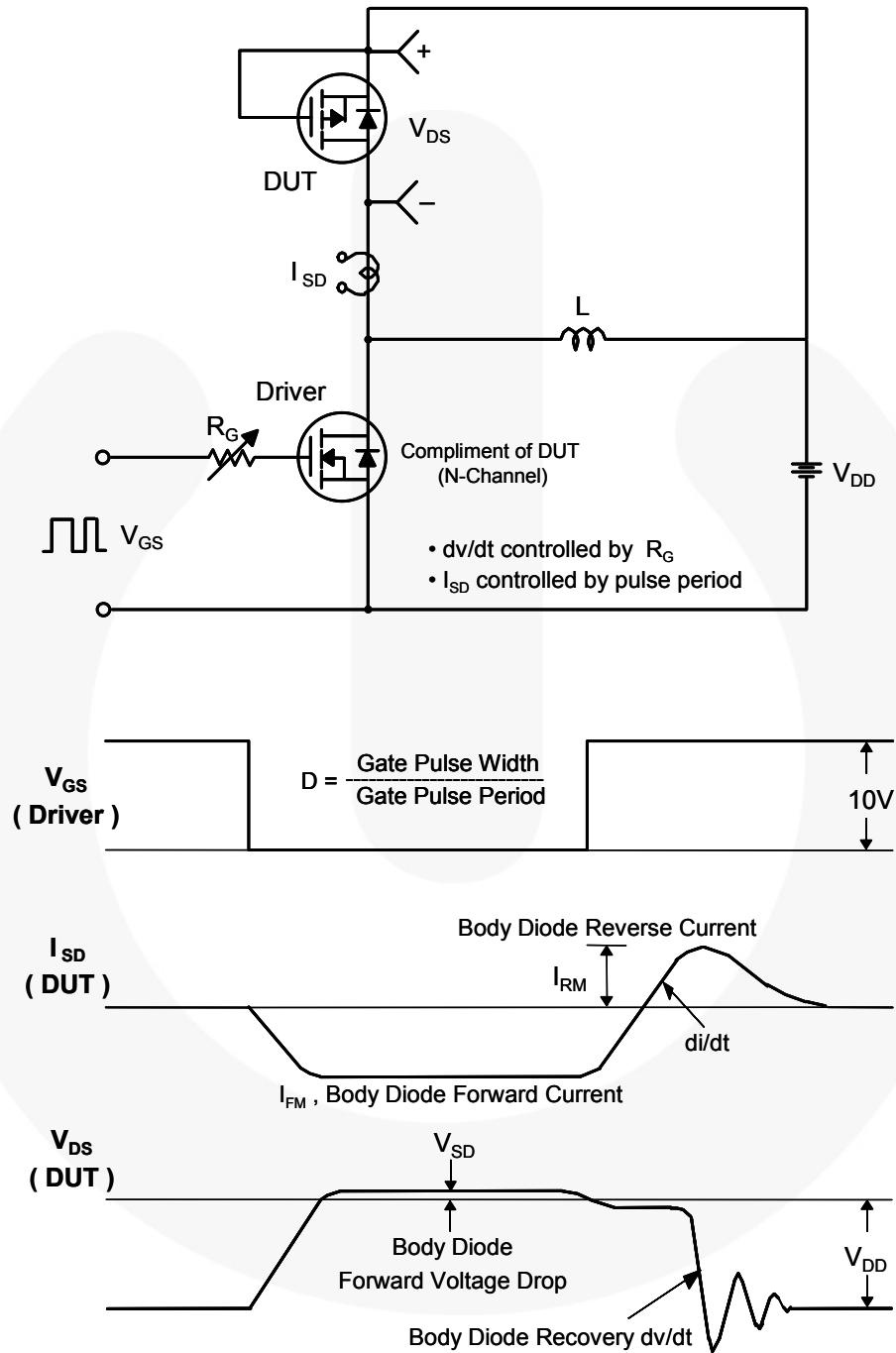
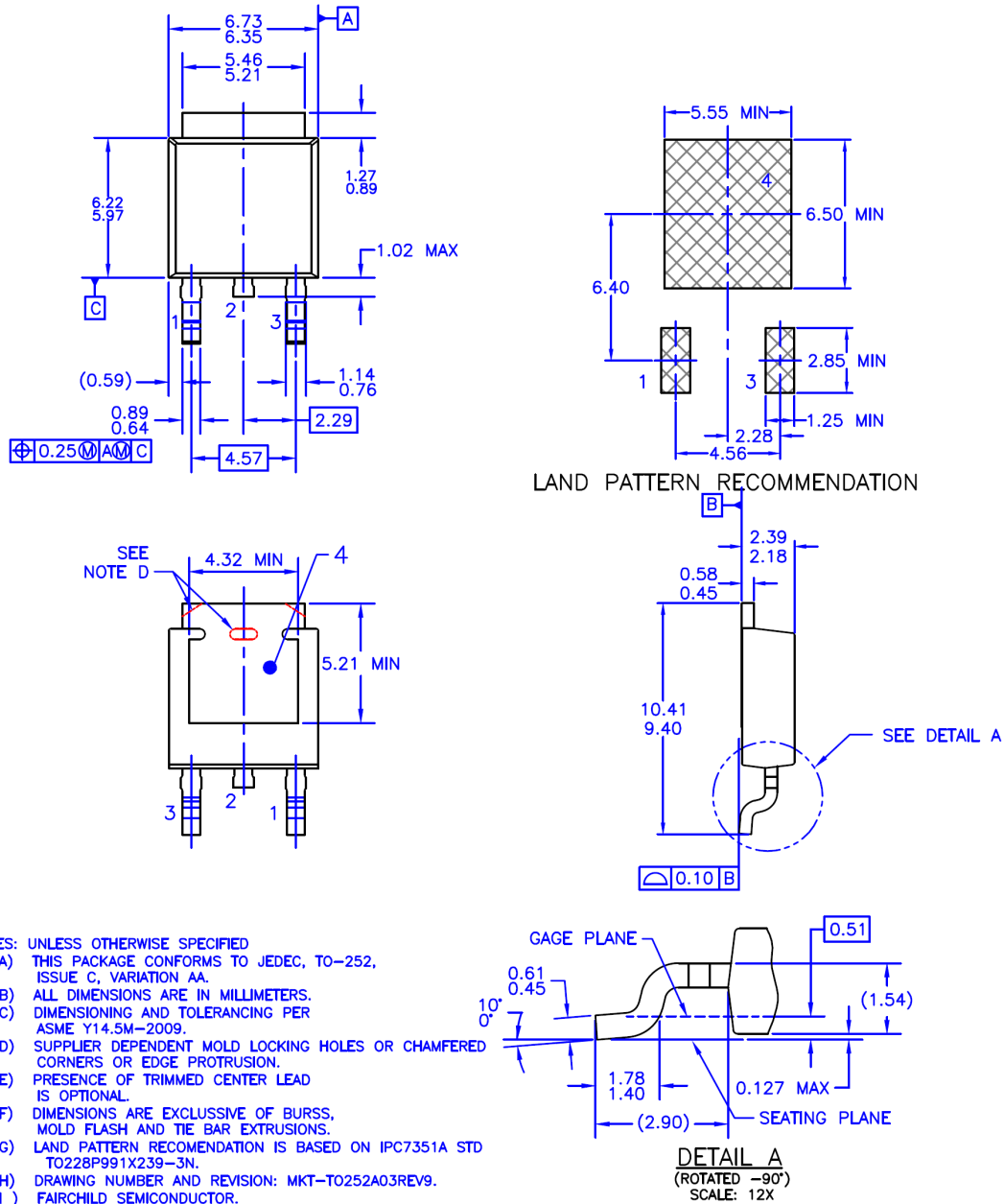


Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

## Mechanical Dimensions



**Figure 16. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB**

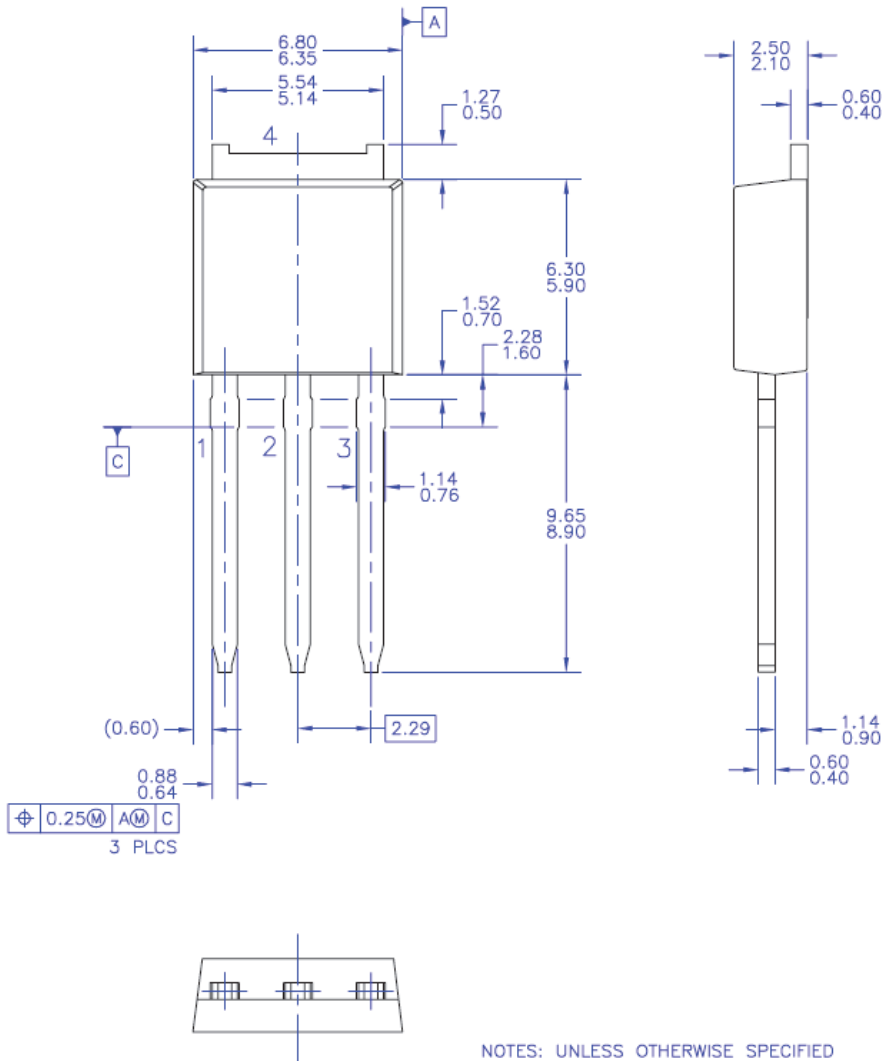
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## Mechanical Dimensions



**Figure 17. TO251 (I-PAK), Molded, 3-Lead**

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