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April 2014

# FQA19N60

## N-Channel QFET<sup>®</sup> MOSFET

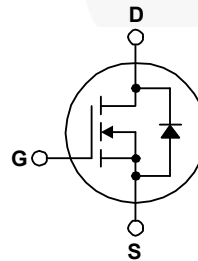
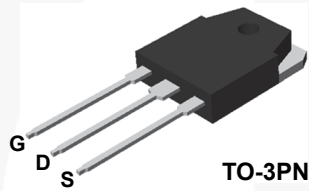
600 V, 18.5 A, 380 mΩ

### Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

### Features

- 18.5 A, 600 V,  $R_{DS(on)} = 380\text{ m}\Omega$  (Max.) @  $V_{GS} = 10\text{ V}$ ,  $I_D = 9.3\text{ A}$
- Low Gate Charge (Typ. 70 nC)
- Low Crss (Typ. 35 pF)
- 100% Avalanche Tested



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQA19N60	Unit
$V_{DSS}$	Drain-Source Voltage	600	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ )	18.5	A
	- Continuous ( $T_C = 100^\circ\text{C}$ )	11.7	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	74	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	1150	mJ
$I_{AR}$	Avalanche Current (Note 1)	18.5	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	30	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	300	W
	- Derate above $25^\circ\text{C}$	2.38	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FQA19N60	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.42	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink, Typ.	0.24	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	40	$^\circ\text{C}/\text{W}$

FQA19N60 — N-Channel QFET<sup>®</sup> MOSFET

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQA19N60	FQA19N60	TO-3PN	Tube	N/A	N/A	30 units

## Electrical Characteristics $T_c = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	600	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.65	--	V/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	--	--	10	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, T_C = 125^\circ\text{C}$	--	--	100	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 9.3\text{ A}$	--	0.3	0.38	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 50\text{ V}, I_D = 9.3\text{ A}$	--	16	--	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	2800	3600	pF
$C_{oss}$	Output Capacitance		--	350	450	pF
$C_{rss}$	Reverse Transfer Capacitance		--	35	45	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 300\text{ V}, I_D = 18.5\text{ A},$ $R_G = 25\ \Omega$	--	65	140	ns
$t_r$	Turn-On Rise Time		--	210	430	ns
$t_{d(off)}$	Turn-Off Delay Time		--	150	310	ns
$t_f$	Turn-Off Fall Time		(Note 4)	--	135	280
$Q_g$	Total Gate Charge	$V_{DS} = 480\text{ V}, I_D = 18.5\text{ A},$ $V_{GS} = 10\text{ V}$	--	70	90	nC
$Q_{gs}$	Gate-Source Charge		--	17	--	nC
$Q_{gd}$	Gate-Drain Charge		(Note 4)	--	33	--

### Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	18.5	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	74	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 18.5\text{ A}$	--	--	1.4	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 18.5\text{ A},$	--	420	--	ns
$Q_{rr}$	Reverse Recovery Charge	$di_F / dt = 100\text{ A}/\mu\text{s}$	--	4.7	--	$\mu\text{C}$

#### Notes:

1. Repetitive rating : pulse-width limited by maximum junction temperature.
2.  $L = 6.2\text{ mH}, I_{AS} = 18.5\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 18.5\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature.

Typical Characteristics

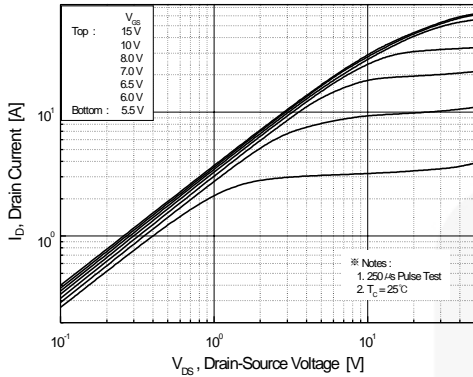


Figure 1. On-Region Characteristics

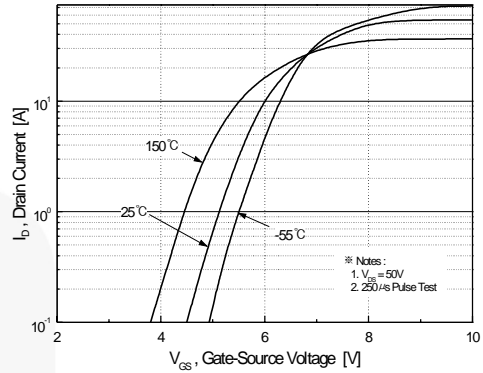


Figure 2. Transfer Characteristics

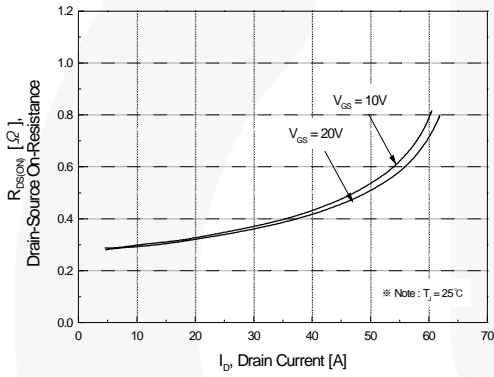


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

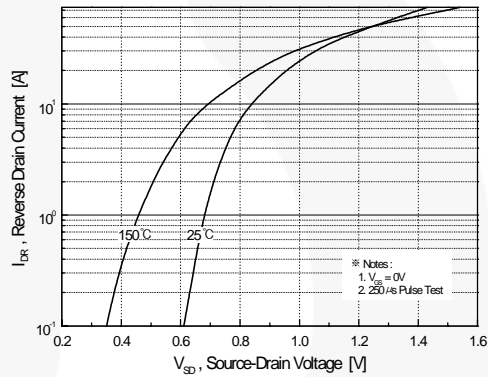


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

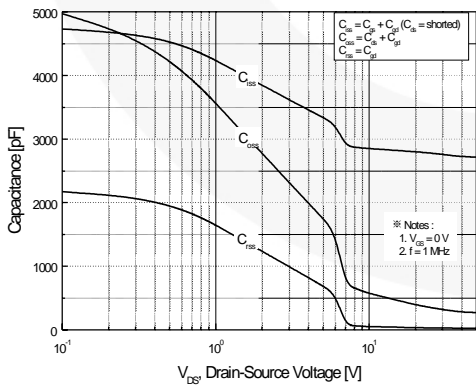


Figure 5. Capacitance Characteristics

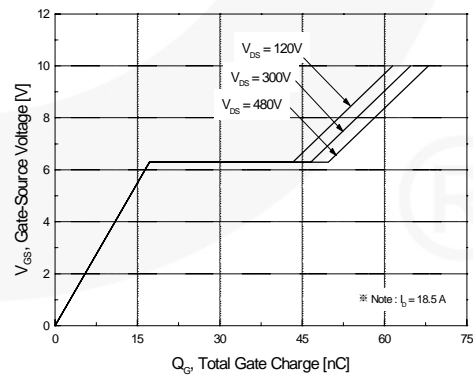


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

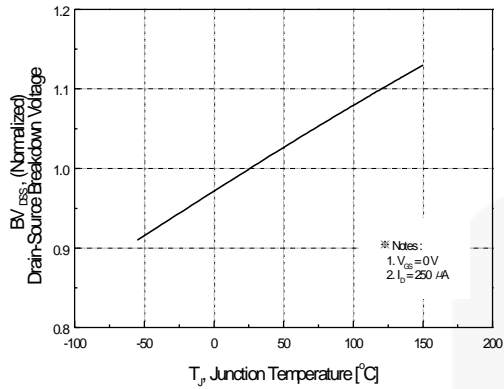


Figure 7. Breakdown Voltage Variation vs. Temperature

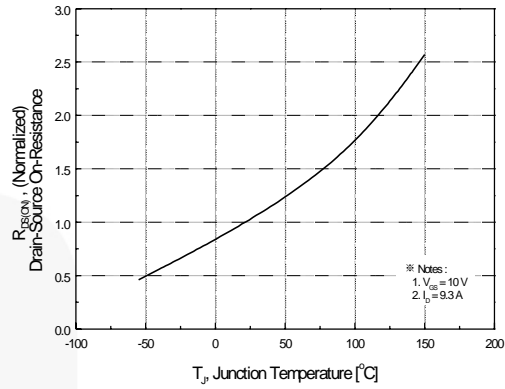


Figure 8. On-Resistance Variation vs. Temperature

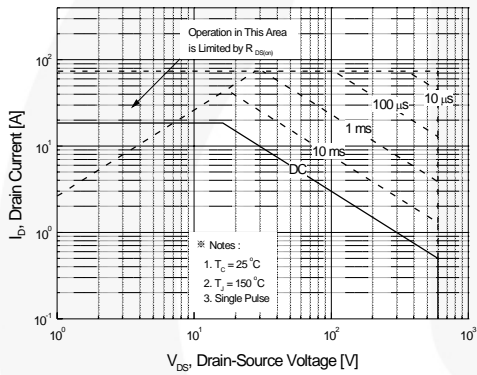


Figure 9. Maximum Safe Operating Area

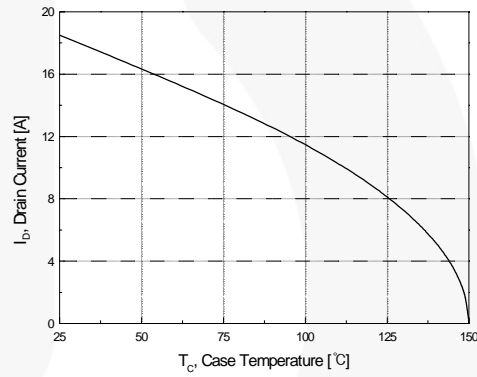


Figure 10. Maximum Drain Current vs. Case Temperature

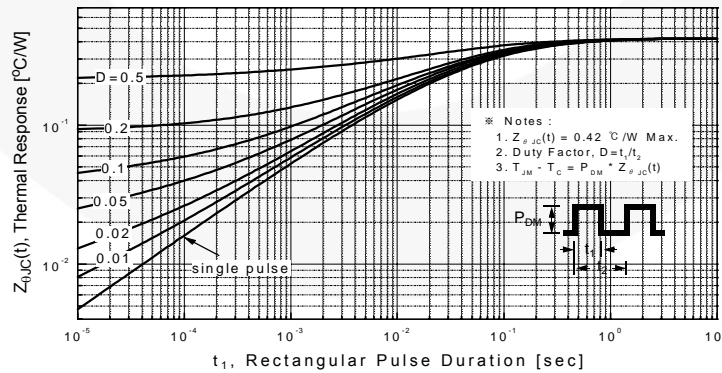


Figure 11. Transient Thermal Response Curve

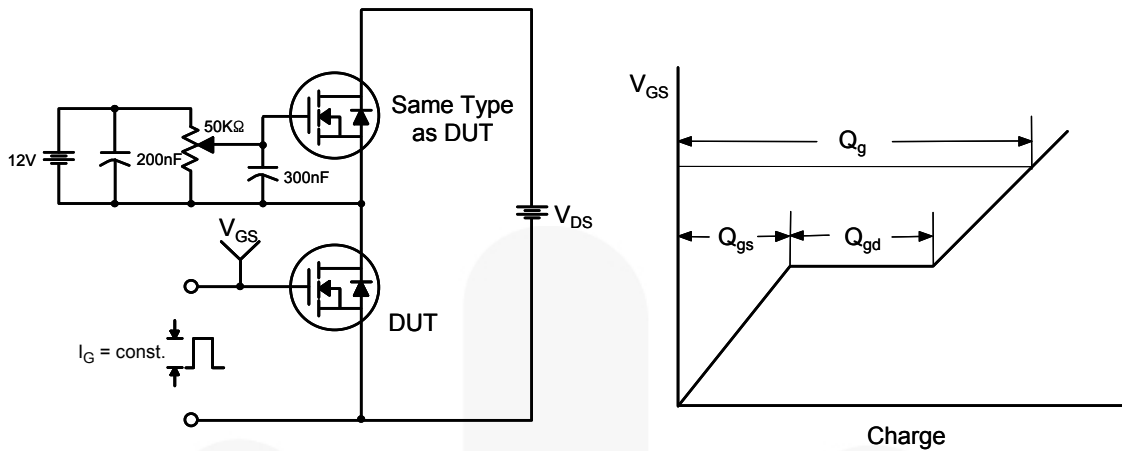


Figure 12. Gate Charge Test Circuit & Waveform

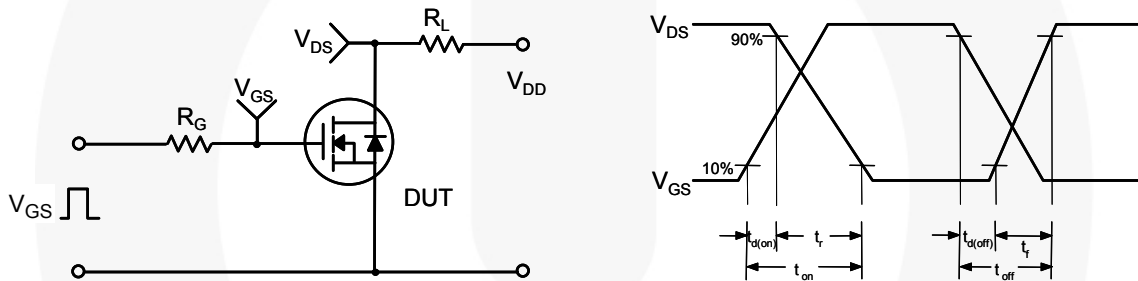


Figure 13. Resistive Switching Test Circuit & Waveforms

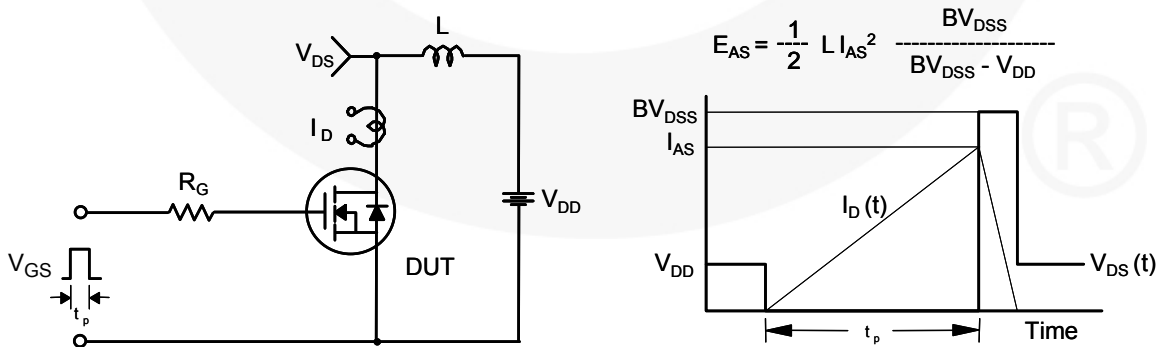


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

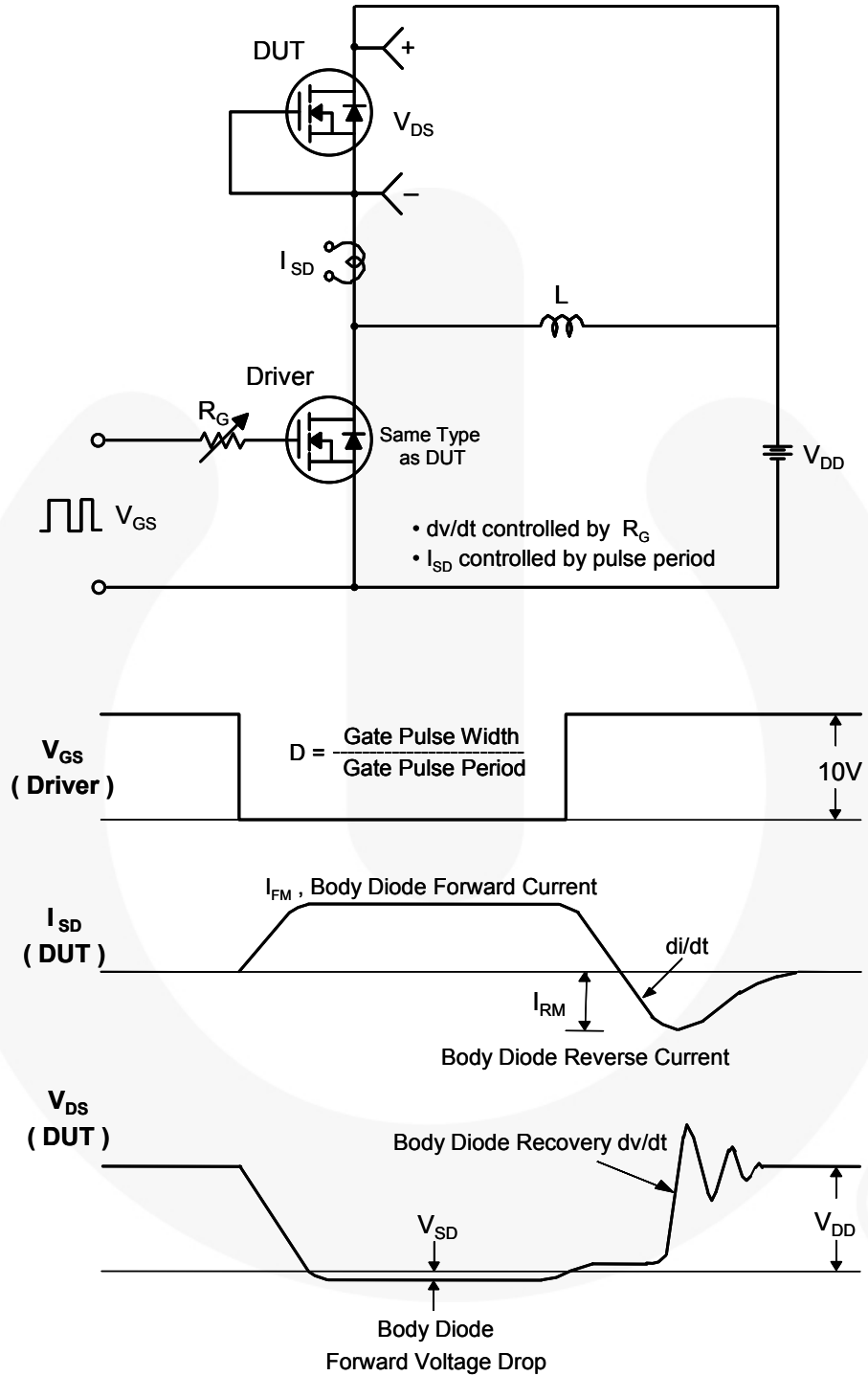
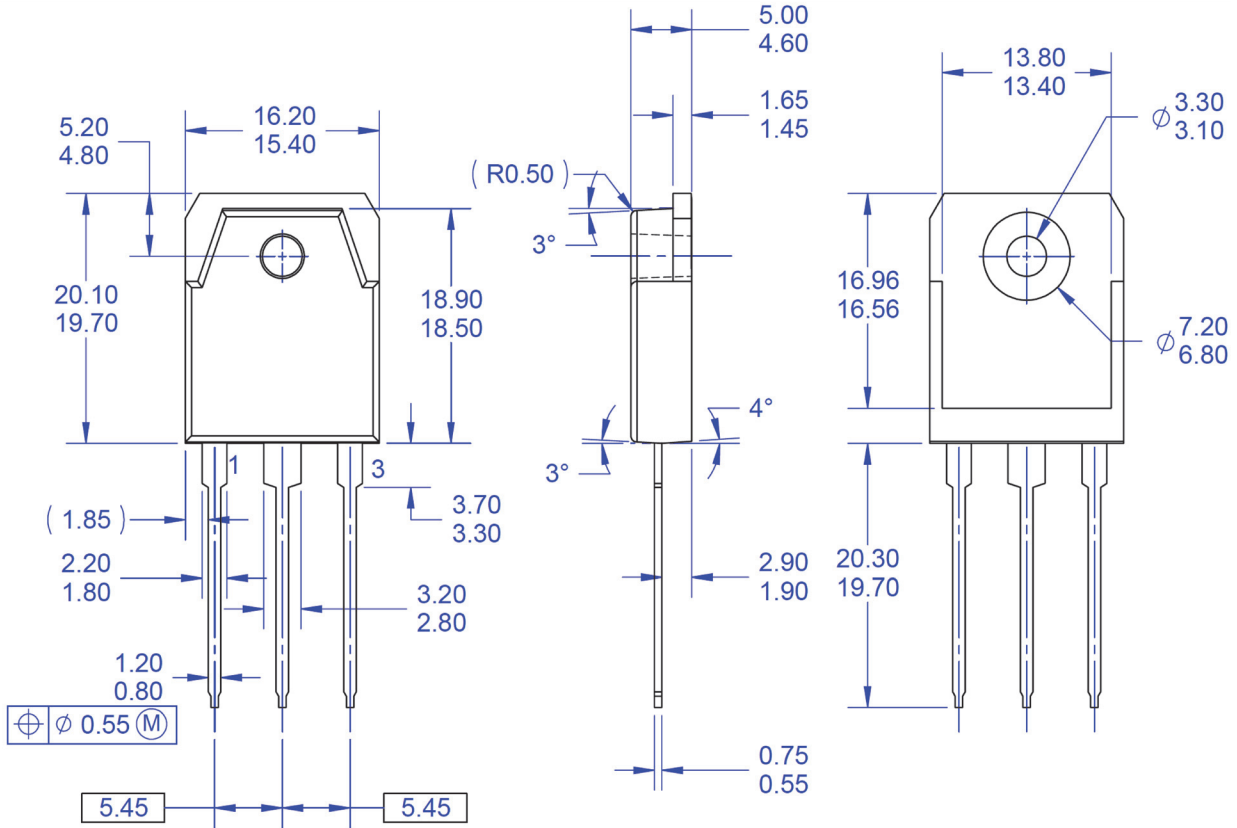


Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

### Mechanical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO EIAJ SC-65 PACKAGING STANDARD.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSION AND TOLERANCING PER ASME14.5-2009.
- D) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- E) DRAWING FILE NAME: TO3PN03AREV1.
- F) FAIRCHILD SEMICONDUCTOR.

**Figure 16. TO3PN, 3-Lead, Plastic, EIAJ SC-65**

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| BitSiC™                  | Global Power Resource <sup>SM</sup>             | PowerXS™                              | TinyBuck®        |
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