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October 2013

FDP3652 / FDB3652

N-Channel PowerTrench® MOSFET

100 V, 61 A, 16 mΩ

Features

- $r_{DS(on)}$ = 14 mΩ (Typ.), V_{GS} = 10 V, I_D = 61 A
- $Q_{g(tot)}$ = 41 nC (Typ.), V_{GS} = 10 V
- Low Miller Charge
- Low Q_{RR} Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)

Formerly developmental type 82769

Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor drives and Uninterruptible Power Supplies
- Micro Solar Inverter

TO-220

D^2-PAK
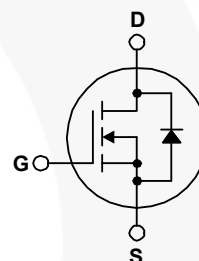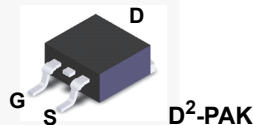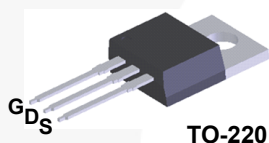
MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	FDP3652 / FDB3652	Unit
V_{DSS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current		
	Continuous (T_C = 25°C, V_{GS} = 10V)	61	A
	Continuous (T_C = 100°C, V_{GS} = 10V)	43	A
	Continuous (T_{amb} = 25°C, V_{GS} = 10V) with $R_{\theta JA}$ = 43°C/W	9	A
	Pulsed	Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)	182	mJ
P_D	Power dissipation	150	W
	Derate above 25°C	1.0	W/°C
T_J, T_{STG}	Operating and Storage Temperature	-55 to 175	°C

Thermal Characteristics

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance Junction to Case TO-220, D^2-PAK	1.0	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-220, D^2-PAK (Note 2)	62	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient D^2-PAK, 1in^2 copper pad area	43	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB3652	FDB3652	D²-PAK	330 mm	24 mm	800 units
FDP3652	FDP3652	TO-220	Tube	N/A	50 units

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
Off Characteristics							
B_{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu A$, $V_{GS} = 0V$		100	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80V$		-	-	1	μA
		$V_{GS} = 0V$	$T_C = 150°C$	-	-	250	
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm20V$		-	-	±100	nA
On Characteristics							
$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		2	-	4	V
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = 61A$, $V_{GS} = 10V$		-	0.014	0.016	Ω
		$I_D = 30A$, $V_{GS} = 6V$		-	0.018	0.026	
		$I_D = 61A$, $V_{GS} = 10V$, $T_J = 175°C$		-	0.035	0.043	
Dynamic Characteristics							
C_{ISS}	Input Capacitance	$V_{DS} = 25V$, $V_{GS} = 0V$, f = 1MHz		-	2880	-	pF
C_{OSS}	Output Capacitance			-	390	-	pF
C_{RSS}	Reverse Transfer Capacitance			-	100	-	pF
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0V$ to 10V	$V_{DD} = 50V$ $I_D = 61A$ $I_g = 1.0mA$		41	53	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0V$ to 2V		-	5	6.5	nC
Q_{gs}	Gate to Source Gate Charge			-	15	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau			-	10	-	nC
Q_{gd}	Gate to Drain "Miller" Charge			-	10	-	nC

Switching Characteristics (V_{GS} = 10V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{ON}	Turn-On Time		-	-	146	ns
$t_{d(ON)}$	Turn-On Delay Time		-	12	-	ns
t_r	Rise Time	$V_{DD} = 50V$, $I_D = 61A$	-	85	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time	$V_{GS} = 10V$, $R_{GS} = 6.8\Omega$	-	26	-	ns
t_f	Fall Time		-	45	-	ns
t_{OFF}	Turn-Off Time		-	-	107	ns

Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 61A$	-	-	1.25	V
		$I_{SD} = 30A$	-	-	1.0	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 61A$, $dI_{SD}/dt = 100A/\mu s$	-	-	62	ns
Q_{RR}	Reverse Recovered Charge	$I_{SD} = 61A$, $dI_{SD}/dt = 100A/\mu s$	-	-	45	nC

Notes:
1: Starting $T_J = 25°C$, L = 0.228mH, $I_{AS} = 40A$.
2: Pulse Width = 100s

Typical Characteristics T_C = 25°C unless otherwise noted
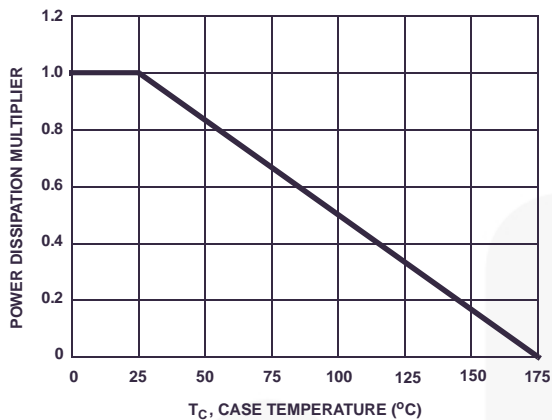
Figure 1. Normalized Power Dissipation vs Ambient Temperature
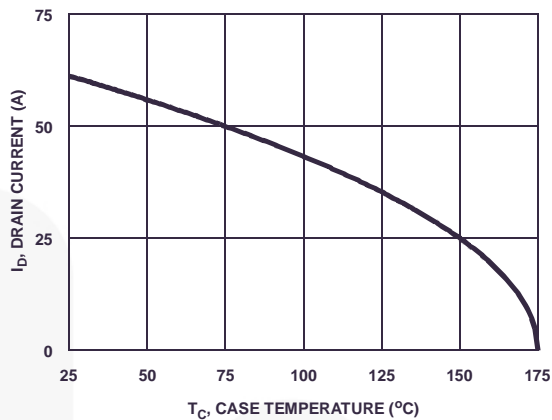
Figure 2. Maximum Continuous Drain Current vs Case Temperature

NOTES:
DUTY FACTOR: D = t_1/t_2
PEAK T_J = P_{DM} x $Z_{\theta JC}$ x $R_{\theta JC}$ + T_C
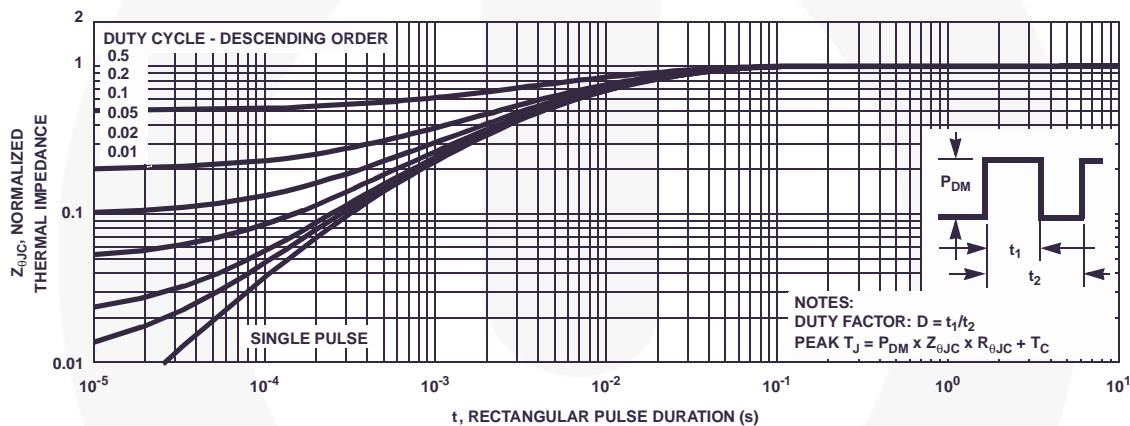
Figure 3. Normalized Maximum Transient Thermal Impedance

T_C = 25°C
FOR TEMPERATURES ABOVE 25°C DERATE PEAK CURRENT AS FOLLOWS:

$$I = I_{25} \sqrt{\frac{175 - T_C}{150}}$$

TRANSCONDUCTANCE MAY LIMIT CURRENT IN THIS REGION

V_{GS} = 10V
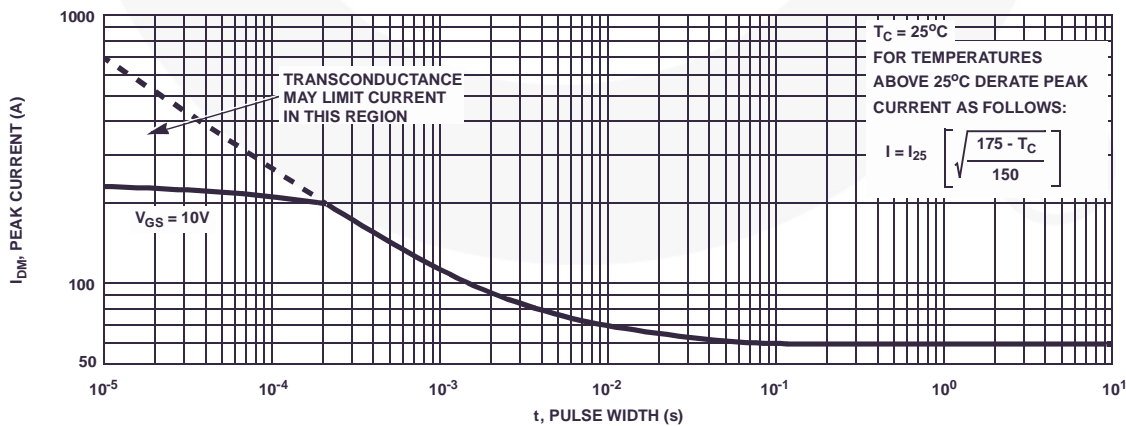
Figure 4. Peak Current Capability

Typical Characteristics T_C = 25°C unless otherwise noted
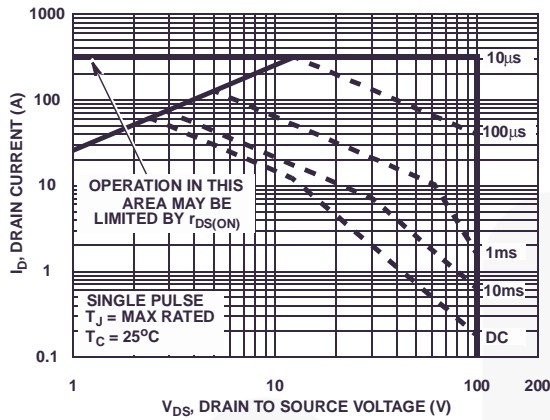
Figure 5. Forward Bias Safe Operating Area
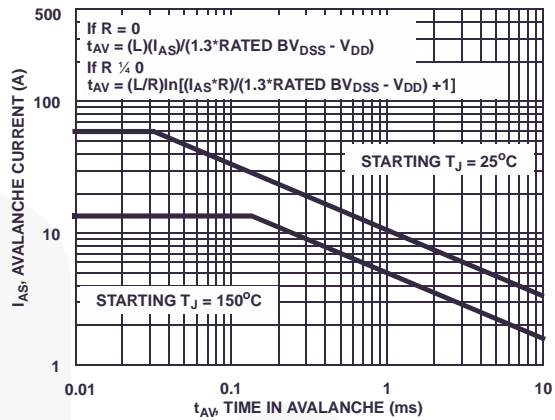
NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability
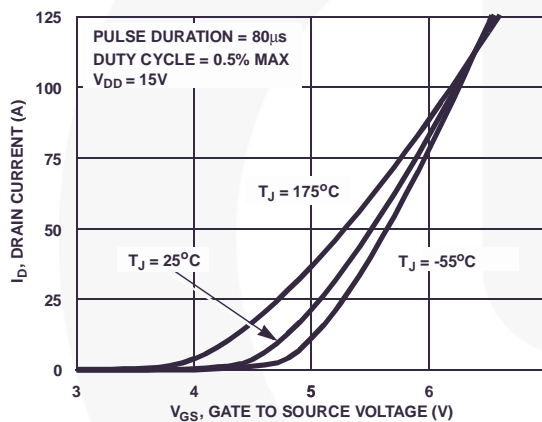
Figure 7. Transfer Characteristics
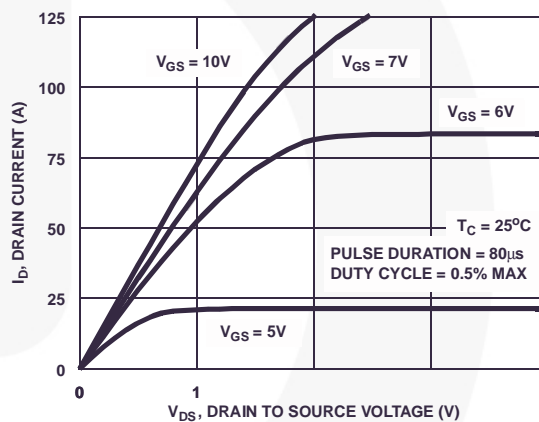
Figure 8. Saturation Characteristics
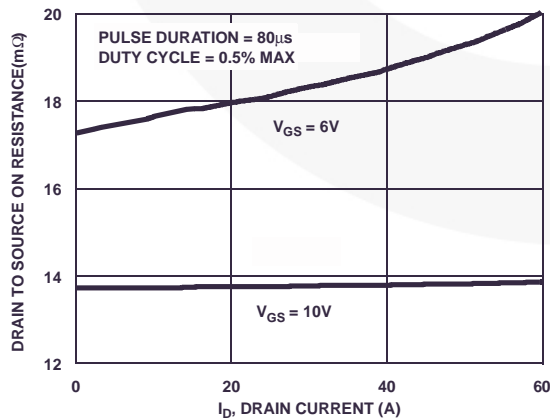
Figure 9. Drain to Source On Resistance vs Drain Current
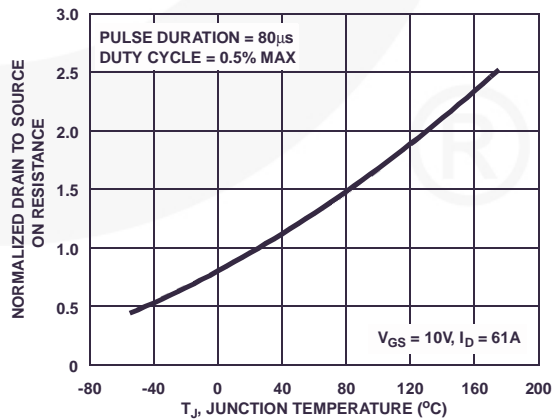
Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Typical Characteristics T_C = 25°C unless otherwise noted
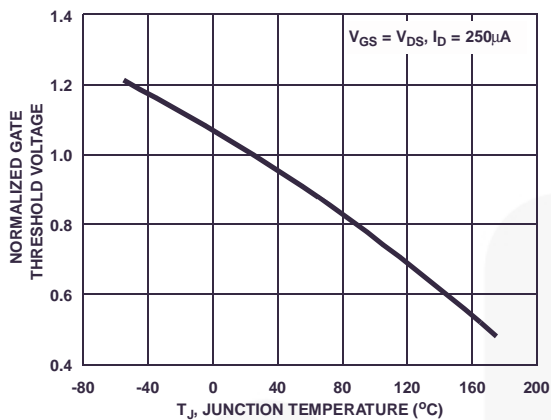
Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature
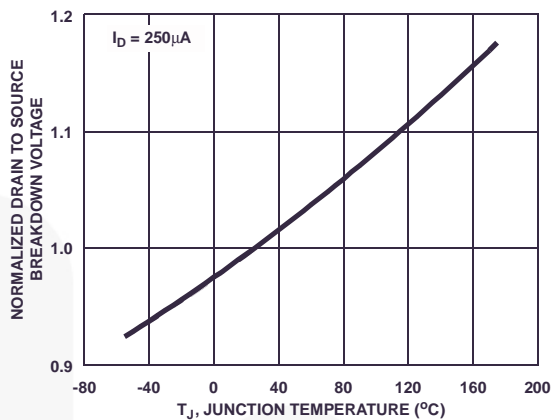
Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature
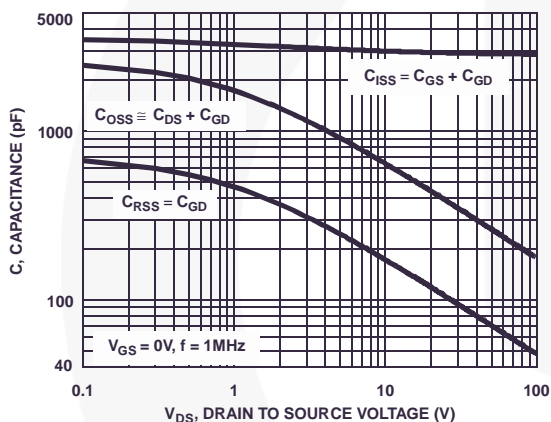
Figure 13. Capacitance vs Drain to Source Voltage
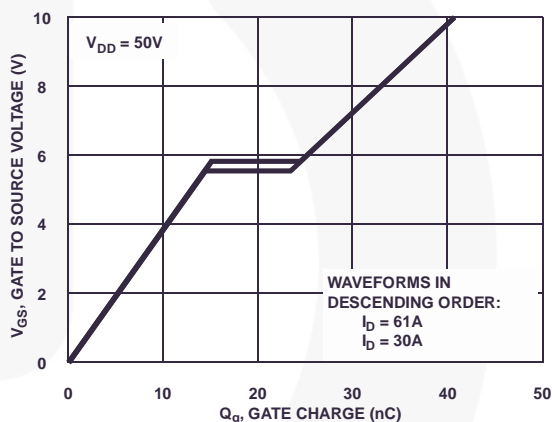
Figure 14. Gate Charge Waveforms for Constant Gate Currents

Test Circuits and Waveforms
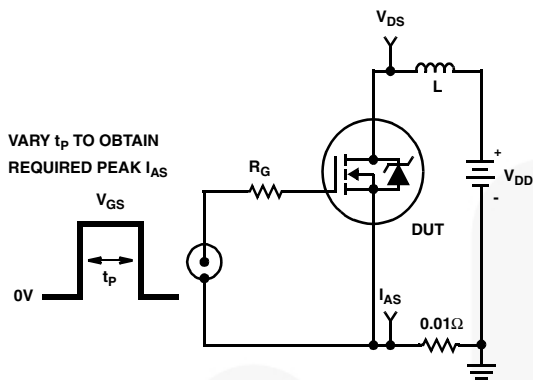
Figure 15. Unclamped Energy Test Circuit

VARY t_P TO OBTAIN REQUIRED PEAK I_AS
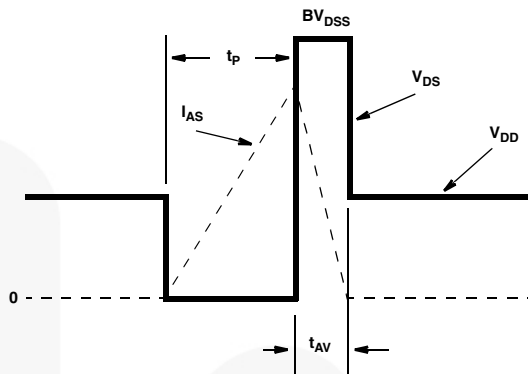
Figure 16. Unclamped Energy Waveforms
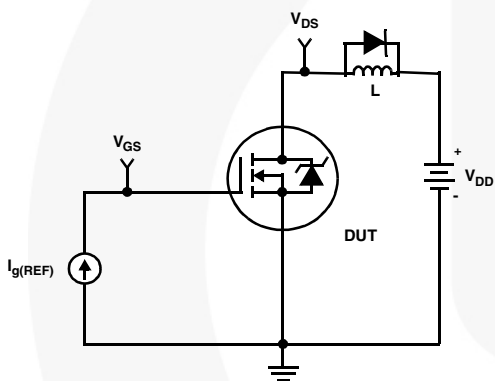
Figure 17. Gate Charge Test Circuit
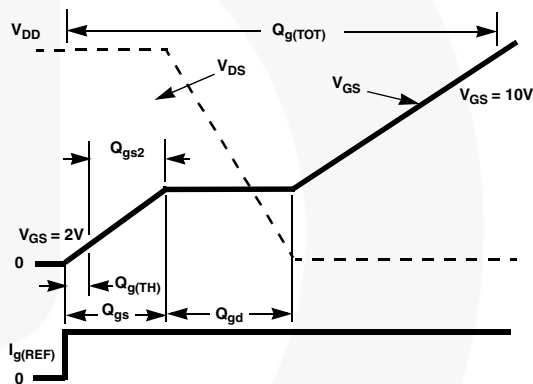
Figure 18. Gate Charge Waveforms
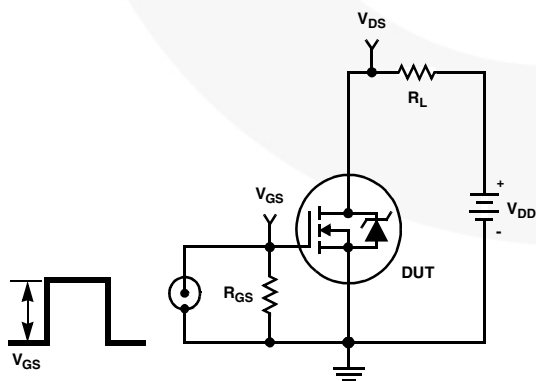
Figure 19. Switching Time Test Circuit
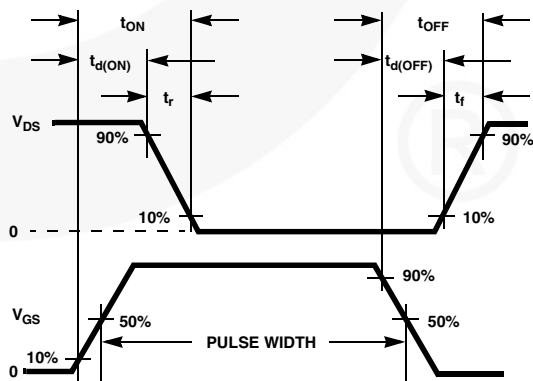
Figure 20. Switching Time Waveforms

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM}, and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM}, in an application. Therefore the application's ambient temperature, T_A (°C), and thermal resistance $R_{\theta JA}$ (°C/W) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \qquad \text{(EQ. 1)}$$

In using surface mount devices such as the TO-263 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.

2. The number of copper layers and the thickness of the board.

3. The use of external heat sinks.

4. The use of thermal vias.

5. Air flow and board orientation.

6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 21 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2 or 3. Equation 2 is used for copper area defined in inches square and equation 3 is for area in centimeter square. The area, in square inches or square centimeters is the top copper area including the gate and source pads.

$$R_{\theta JA} = 26.51 + \frac{19.84}{(0.262 + Area)} \qquad \text{(EQ. 2)}$$

Area in Iches Squared

$$R_{\theta JA} = 26.51 + \frac{128}{(1.69 + Area)} \qquad \text{(EQ. 3)}$$

Area in Centimeter Squared

$R_{\theta JA} = 26.51 + 19.84/(0.262 + Area)$ EQ.2
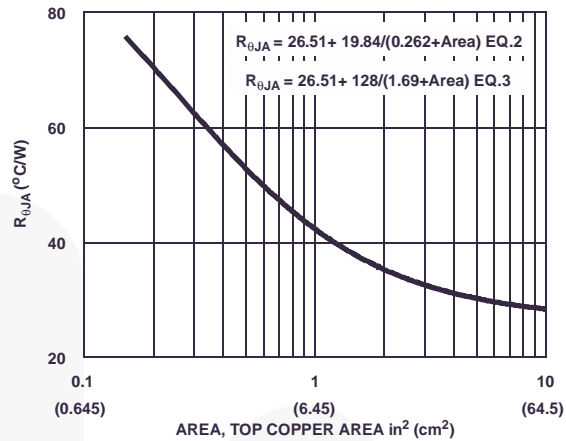$R_{\theta JA} = 26.51 + 128/(1.69 + Area)$ EQ.3

Figure 21. Thermal Resistance vs Mounting Pad Area

PSPICE Electrical Model

.SUBCKT FDP3652 2 1 3 rev March 2002
Ca 12 8 1.1e-9
Cb 15 14 1.1e-9
Cin 6 8 2.8e-9

Dbody 7 5 DbodyMOD
Dbreak 5 11 DbreakMOD
Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 108.2
Eds 14 8 5 8 1
Egs 13 8 6 8 1
Esg 6 10 6 8 1
Evthres 6 21 19 8 1
Evtemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 7.16e-9
Ldrain 2 5 1.0e-9
Lsource 3 7 2.29e-9

RLgate 1 9 71.6
RLdrain 2 5 10
RLsource 3 7 22.9

Mmed 16 6 8 8 MmedMOD
Mstro 16 6 8 8 MstroMOD
Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1
Rdrain 50 16 RdrainMOD 5.7e-3
Rgate 9 20 1.06
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
Rsource 8 7 RsourceMOD 6.5e-3
Rvthres 22 8 RvthresMOD 1
Rvtemp 18 19 RvtempMOD 1
S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*150),7))}

.MODEL DbodyMOD D (IS=1.5E-11 N=1.06 RS=2.5e-3 TRS1=2.4e-3 TRS2=1.1e-6
+ CJO=1.9e-9 M=5.8e-1 TT=2.5e-8 XTI=3.9)
.MODEL DbreakMOD D (RS=2.7e-1 TRS1=1e-3 TRS2=-8.9e-6)
.MODEL DplcapMOD D (CJO=7e-10 IS=1e-30 N=10 M=0.58)
.MODEL MmedMOD NMOS (VTO=3.6 KP=5.5 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=1.06)
.MODEL MstroMOD NMOS (VTO=4.3 KP=110 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL MweakMOD NMOS (VTO=3 KP=0.03 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=1.06e1 RS=.1)
.MODEL RbreakMOD RES (TC1=1.05e-3 TC2=1e-6)
.MODEL RdrainMOD RES (TC1=1.7e-2 TC2=3.2e-5)
.MODEL RSLCMOD RES (TC1=1e-3 TC2=1e-7)
.MODEL RsourceMOD RES (TC1=1e-3 TC2=1e-6)
.MODEL RvthresMOD RES (TC1=-5.3e-3 TC2=-1.2e-5)
.MODEL RvtempMOD RES (TC1=-3.3e-3 TC2=1.3e-6)

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-8 VOFF=-5)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-5 VOFF=-8)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1 VOFF=0.5)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=0.5 VOFF=-1)

.ENDS

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.
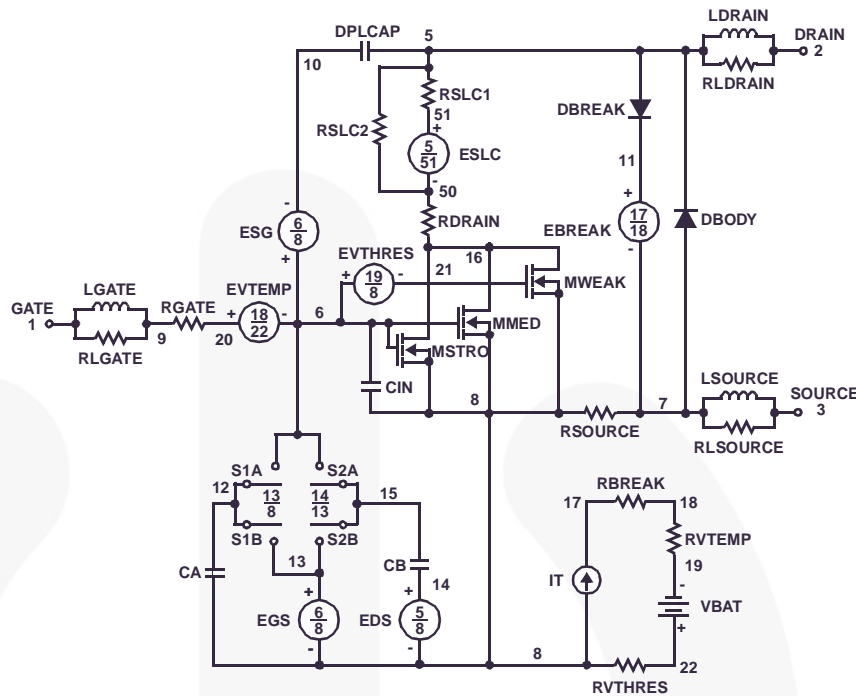
SABER Electrical Model

REV March 2002
template FDP3652 n2,n1,n3
electrical n2,n1,n3
{
var i iscl
dp..model dbodymod = (isl=1.5e-11,nl=1.06,rs=2.5e-3,trs1=2.4e-3,trs2=1.1e-6,cjo=1.9e-9,m=5.8e-1,tt=2.5e-8,xti=3.9)
dp..model dbreakmod = (rs=2.7e-1,trs1=1e-3,trs2=-8.9e-6)
dp..model dplcapmod = (cjo=7e-10,isl=10e-30,nl=10,m=0.58)
m..model mmedmod = (type=_n,vto=3.6,kp=5.5,is=1e-30, tox=1)
m..model mstrongmod = (type=_n,vto=4.3,kp=110,is=1e-30, tox=1)
m..model mweakmod = (type=_n,vto=3,kp=0.03,is=1e-30, tox=1,rs=.1)
sw_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-8,voff=-5)
sw_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-5,voff=-8)
sw_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-1,voff=0.5)
sw_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=0.5,voff=-1)
c.ca n12 n8 = 1.1e-9
c.cb n15 n14 = 1.1e-9
c.cin n6 n8 = 2.8e-9

dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod

spe.ebreak n11 n7 n17 n18 = 108.2
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evthres n6 n21 n19 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1

i.it n8 n17 = 1

l.lgate n1 n9 = 7.16e-9
l.ldrain n2 n5 = 1.0e-9
l.lsource n3 n7 = 2.29e-9

res.rlgate n1 n9 = 71.6
res.rldrain n2 n5 = 10
res.rlsource n3 n7 = 22.9

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18 = 1, tc1=1.05e-3,tc2=1e-6
res.rdrain n50 n16 = 5.7e-3, tc1=1.7e-2,tc2=3.2e-5
res.rgate n9 n20 = 1.06
res.rslc1 n5 n51 = 1e-6, tc1=1e-3,tc2=1e-7
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 6.5e-3, tc1=1e-3,tc2=1e-6
res.rvthres n22 n8 = 1, tc1=-5.3e-3,tc2=-1.2e-5
res.rvtemp n18 n19 = 1, tc1=-3.3e-3,tc2=1.3e-6
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1
equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/150))** 7))
}
}
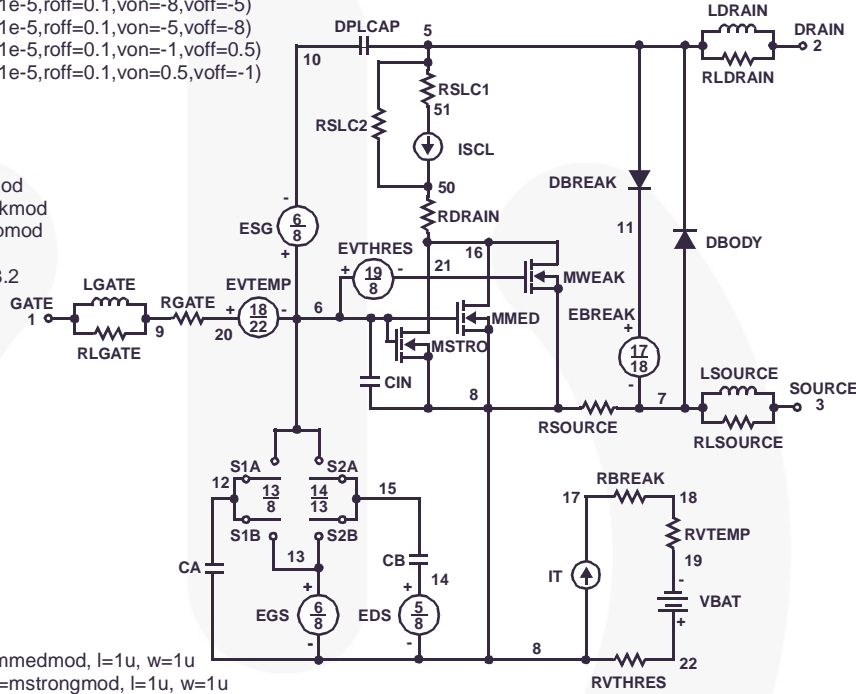
SPICE Thermal Model

REV 23 March 2002

FDP3652

CTHERM1 TH 6 1e-2
CTHERM2 6 5 1.5e-2
CTHERM3 5 4 2e-2
CTHERM4 4 3 2.1e-2
CTHERM5 3 2 2.2e-2
CTHERM6 2 TL 9e-2

RTHERM1 TH 6 2.7e-2
RTHERM2 6 5 2.8e-2
RTHERM3 5 4 7.8e-2
RTHERM4 4 3 9e-2
RTHERM5 3 2 2.7e-1
RTHERM6 2 TL 2.87e-1

SABER Thermal Model

SABER thermal model FDP3652
template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 6 =1e-2
ctherm.ctherm2 6 5 =1.5e-2
ctherm.ctherm3 5 4 =2e-2
ctherm.ctherm4 4 3 =2.1e-2
ctherm.ctherm5 3 2 =2.2e-2
ctherm.ctherm6 2 tl =9e-2

rtherm.rtherm1 th 6 =2.7e-2
rtherm.rtherm2 6 5 =2.8e-2
rtherm.rtherm3 5 4 =7.8e-2
rtherm.rtherm4 4 3 =9e-2
rtherm.rtherm5 3 2 =2.7e-1
rtherm.rtherm6 2 tl =2.87e-1
}

Mechanical Dimensions

TO-220 3L

Figure 22. TO-220, Molded, 3Lead, Jedec Variation AB

NOTES: UNLESS OTHERWISE SPECIFIED
A) REFERENCE JEDEC, TO-220, ISSUE K, VARIATION AB, DATED APRIL, 2002.
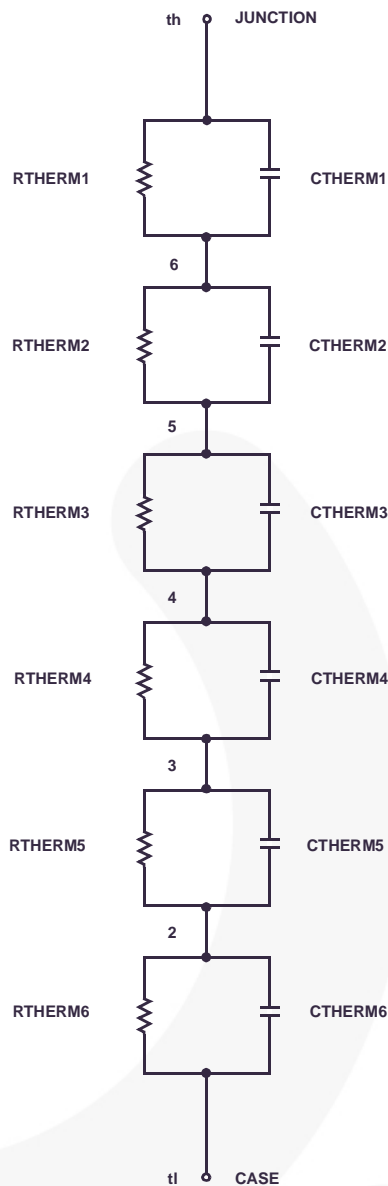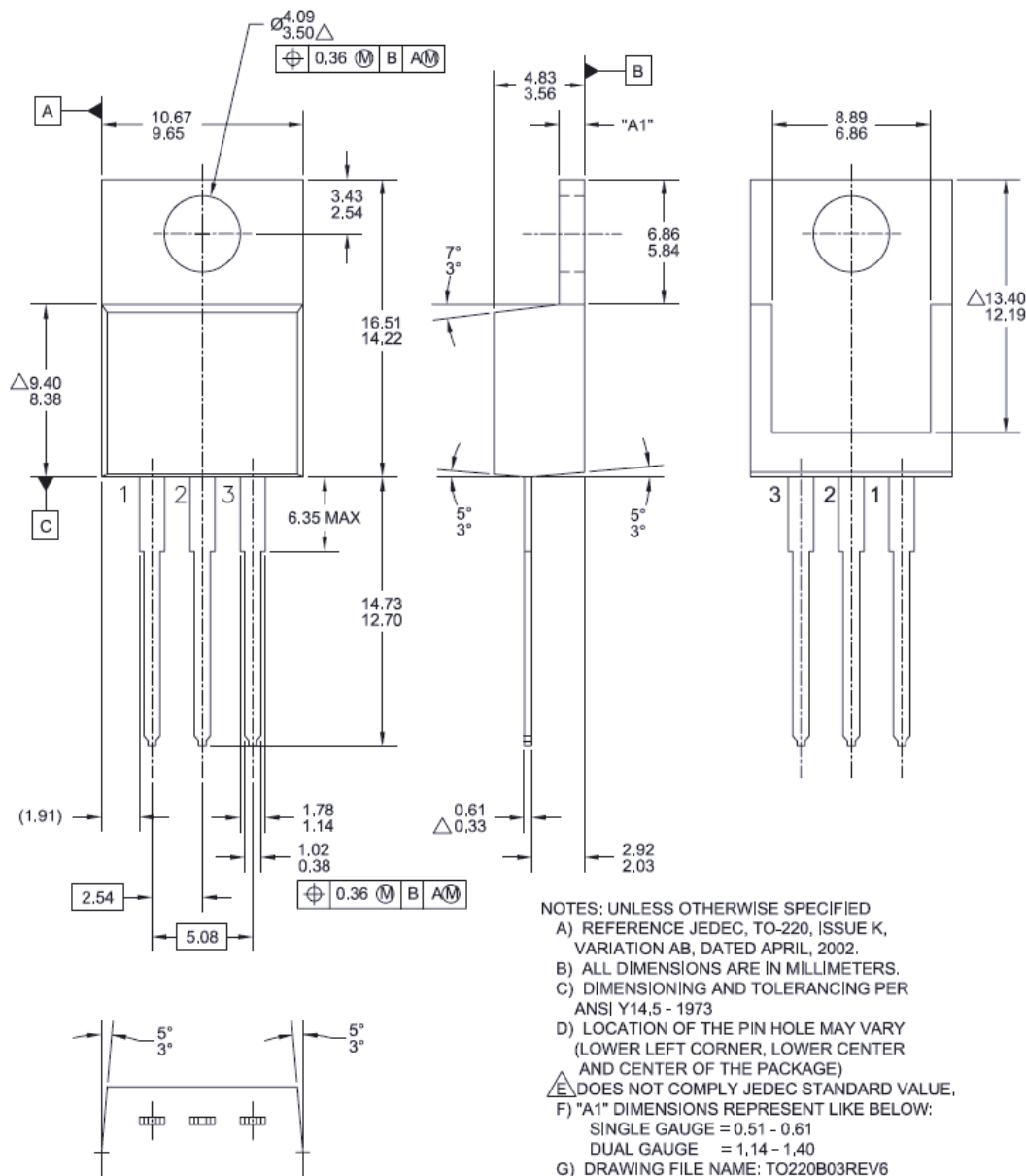B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ANSI Y14,5 - 1973
D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
E) DOES NOT COMPLY JEDEC STANDARD VALUE,
F) "A1" DIMENSIONS REPRESENT LIKE BELOW:
   SINGLE GAUGE = 0.51 - 0.61
   DUAL GAUGE   = 1,14 - 1,40
G) DRAWING FILE NAME: TO220B03REV6

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Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

http://www.fairchildsemi.com/package/packageDetails.html?id=PN_TT220-003

Dimension in Millimeters

Mechanical Dimensions

TO-263 2L (D²PAK)

Figure 23. 2LD, TO263, Surface Mount

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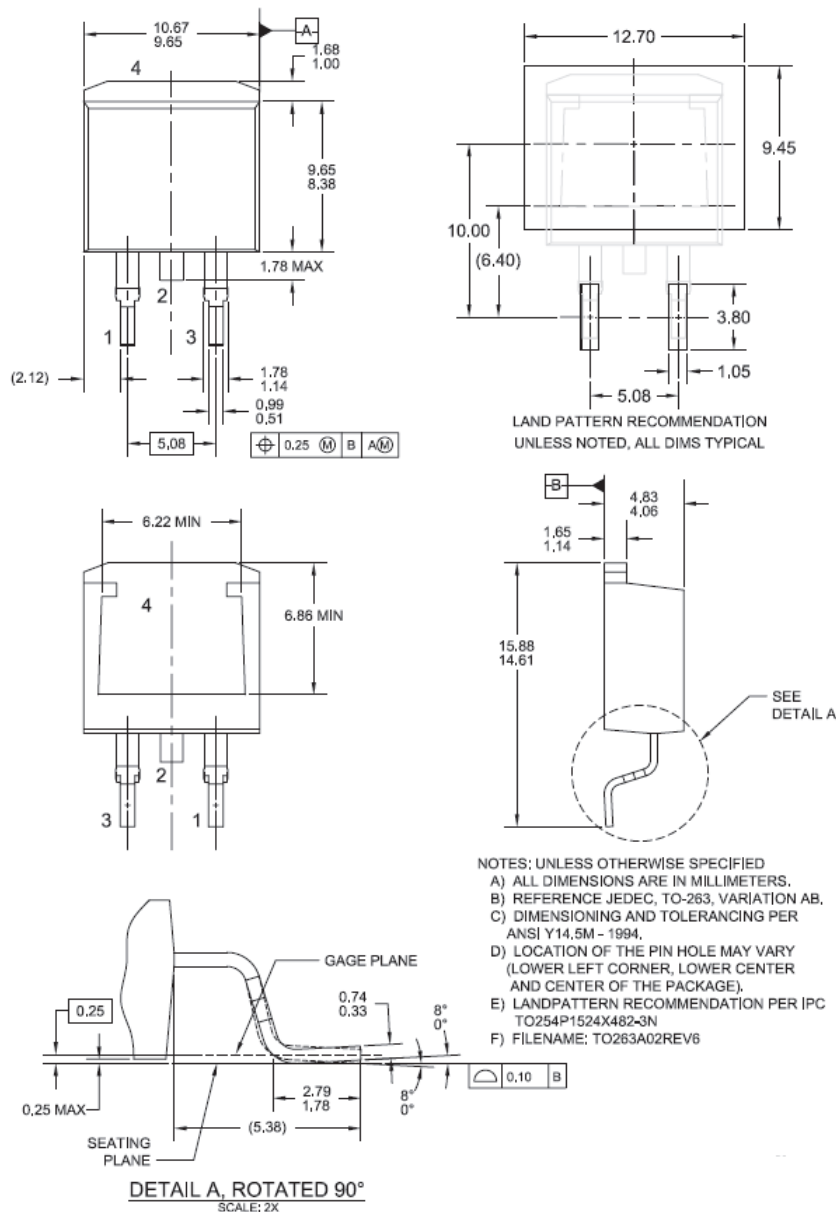
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Dimension in Millimeters

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