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FAIRCHILD SEMICONDUCTOR®

March 2009

# FDG6332C_F085

## 20V N & P-Channel PowerTrench® MOSFETs

### Features

- **Q1** 0.7 A, 20V. $R_{DS(ON)}$ = 300 mΩ @ $V_{GS}$ = 4.5 V
  $R_{DS(ON)}$ = 400 mΩ @ $V_{GS}$ = 2.5 V
- **Q2** –0.6 A, –20V. $R_{DS(ON)}$ = 420 mΩ @ $V_{GS}$ = –4.5 V
  $R_{DS(ON)}$ = 630 mΩ @ $V_{GS}$ = –2.5 V
- Low gate charge
- High performance trench technology for extremely low $R_{DS(ON)}$
- SC70-6 package: small footprint (51% smaller than SSOT-6); low profile (1mm thick)
- Qualified to AEC Q101
- RoHS Compliant

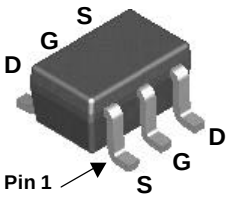
### General Description

The N & P-Channel MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

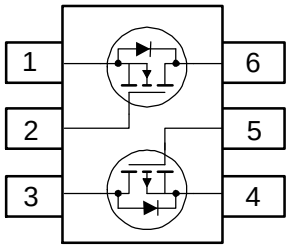
These devices have been designed to offer exceptional power dissipation in a very small footprint for applications where the bigger more expensive TSSOP-8 and SSOP-6 packages are impractical.

### Applications

- DC/DC converter
- Load switch
- LCD display inverter




SC70-6




Complementary

## Absolute Maximum Ratings

$T_A$=25°C unless otherwise noted

| Symbol | Parameter | | Q1 | Q2 | Units |
|---|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 20 | –20 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±12 | ±12 | V |
| $I_D$ | Drain Current – Continuous | (Note 1) | 0.7 | –0.6 | A |
| | – Pulsed | | 2.1 | –2 | |
| $P_D$ | Power Dissipation for Single Operation | (Note 1) | 0.3 | | W |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | –55 to +150 | | °C |

## Thermal Characteristics

| | | | | |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1) | 415 | °C/W |

## Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape width | Quantity |
|---|---|---|---|---|
| .32 | FDG6332C_F085 | 7'' | 8mm | 3000 units |

## Electrical Characteristics

$T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | | Test Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | | | |
| $BV_{DSS}$ | Drain–Source Breakdown Voltage | | $V_{GS}$ = 0 V, $I_D$ = 250 µA<br>$V_{GS}$ = 0 V, $I_D$ = –250 µA | **Q1**<br>**Q2** | 20<br>–20 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | | $I_D$ = 250 µA,Ref. to 25°C<br>$I_D$ = –250 µA,Ref. to 25°C | **Q1**<br>**Q2** | | 14<br>–14 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | | $V_{DS}$ = 16 V, $V_{GS}$ = 0 V<br>$V_{DS}$ = –16 V, $V_{GS}$ = 0 V | **Q1**<br>**Q2** | | | 1<br>–1 | µA |
| $I_{GSSF}$ /$I_{GSSR}$ | Gate–Body Leakage, Forward | | $V_{GS}$ = ± 12 V, $V_{DS}$ = 0 V | | | | ±100 | nA |
| $I_{GSSF}$ /$I_{GSSR}$ | Gate–Body Leakage, Reverse | | $V_{GS}$ = ± 12V , $V_{DS}$ = 0 V | | | | ±100 | nA |
| **On Characteristics** (Note 2) | | | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | **Q1** | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | | 0.6 | 1.1 | 1.5 | V |
| | | **Q2** | $V_{DS}$ = $V_{GS}$, $I_D$ = –250 µA | | -0.6 | –1.2 | –1.5 | |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | **Q1**<br>**Q2** | $I_D$ = 250 µA,Ref. To 25°C<br>$I_D$ = –250 µA,Ref. to 25°C | | | –2.8<br>3 | | mV/°C |
| $R_{DS(on)}$ | Static Drain–Source On–Resistance | **Q1** | $V_{GS}$ = 4.5 V, $I_D$ =0.7 A<br>$V_{GS}$ = 2.5 V, $I_D$ =0.6 A<br>$V_{GS}$ = 4.5 V, $I_D$ =0.7A,$T_J$=125°C | | | 180<br>293<br>247 | 300<br>400<br>442 | mΩ |
| | | **Q2** | $V_{GS}$ = –4.5 V, $I_D$ = –0.6 A<br>$V_{GS}$ = –2.5 V, $I_D$ = –0.5 A<br>$V_{GS}$=–4.5 V, $I_D$ =–0.6 A,$T_J$=125°C | | | 300<br>470<br>400 | 420<br>630<br>700 | |
| $g_{FS}$ | Forward Transconductance | **Q1** | $V_{DS}$ = 5 V $I_D$ = 0.7 A | | | 2.8 | | S |
| | | **Q2** | $V_{DS}$ = –5 V $I_D$ = –0.6A | | | 1.8 | | |
| $I_{D(on)}$ | On–State Drain Current | **Q1** | $V_{GS}$ = 4.5 V, $V_{DS}$ = 5 V | | 1 | | | A |
| | | **Q2** | $V_{GS}$ = –4.5 V, $V_{DS}$ = –5 V | | –2 | | | |
| **Dynamic Characteristics** | | | | | | | | |
| $C_{iss}$ | Input Capacitance | **Q1** | $V_{DS}$=10 V, $V_{GS}$= 0 V, f=1.0MHz | | | 113 | | pF |
| | | **Q2** | $V_{DS}$=–10 V, $V_{GS}$= 0 V, f=1.0MHz | | | 114 | | |
| $C_{oss}$ | Output Capacitance | **Q1** | $V_{DS}$=10 V, $V_{GS}$= 0 V, f=1.0MHz | | | 34 | | pF |
| | | **Q2** | $V_{DS}$=–10 V, $V_{GS}$= 0 V, f=1.0MHz | | | 24 | | |
| $C_{rss}$ | Reverse Transfer Capacitance | **Q1** | $V_{DS}$=10 V, $V_{GS}$= 0 V, f=1.0MHz | | | 16 | | pF |
| | | **Q2** | $V_{DS}$=–10 V, $V_{GS}$= 0 V, f=1.0MHz | | | 9 | | |
| **Switching Characteristics** (Note 2) | | | | | | | | |
| $t_{d(on)}$ | Turn–On Delay Time | **Q1** | For **Q1**:<br>$V_{DS}$ =10 V, $I_D$= 1 A<br>$V_{GS}$= 4.5 V, $R_{GEN}$ = 6 Ω<br>For **Q2**:<br>$V_{DS}$ =–10 V, $I_D$= –1 A<br>$V_{GS}$= –4.5 V, $R_{GEN}$ = 6 Ω | | | 5 | 10 | ns |
| | | **Q2** | | | | 5.5 | 11 | |
| $t_r$ | Turn–On Rise Time | **Q1** | | | | 7 | 15 | ns |
| | | **Q2** | | | | 14 | 25 | |
| $t_{d(off)}$ | Turn–Off Delay Time | **Q1** | | | | 9 | 18 | ns |
| | | **Q2** | | | | 6 | 12 | |
| $t_f$ | Turn–Off Fall Time | **Q1** | | | | 1.5 | 3 | ns |
| | | **Q2** | | | | 1.7 | 3.4 | |
| $Q_g$ | Total Gate Charge | **Q1** | For **Q1**:<br>$V_{DS}$ =10 V, $I_D$= 0.7 A<br>$V_{GS}$= 4.5 V, $R_{GEN}$ = 6 Ω<br>For **Q2**:<br>$V_{DS}$ =–10 V, $I_D$= –0.6 A<br>$V_{GS}$= –4.5 V, $R_{GEN}$ = 6 Ω | | | 1.1 | 1.5 | nC |
| | | **Q2** | | | | 1.4 | 2 | |
| $Q_{gs}$ | Gate–Source Charge | **Q1** | | | | 0.24 | | nC |
| | | **Q2** | | | | 0.3 | | |
| $Q_{gd}$ | Gate–Drain Charge | **Q1** | | | | 0.3 | | nC |
| | | **Q2** | | | | 0.4 | | |

## Electrical Characteristics

$T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | | Test Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| **Drain–Source Diode Characteristics and Maximum Ratings** | | | | | | | | |
| $I_S$ | Maximum Continuous Drain–Source Diode Forward Current | | | **Q1** | | | 0.25 | A |
| | | | | **Q2** | | | –0.25 | |
| $V_{SD}$ | Drain–Source Diode Forward Voltage | **Q1** | $V_{GS}$ = 0 V, $I_S$ = 0.25 A (Note 2) | | | 0.74 | 1.2 | V |
| | | **Q2** | $V_{GS}$ = 0 V, $I_S$ = –0.25 A (Note 2) | | | –0.77 | –1.2 | |

**Notes:**

**1.** $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design. $R_{\theta JA}$ = 415°C/W when mounted on a minimum pad of FR-4 PCB in a still air environment.

**2.** Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

## Typical Characteristics: N-Channel

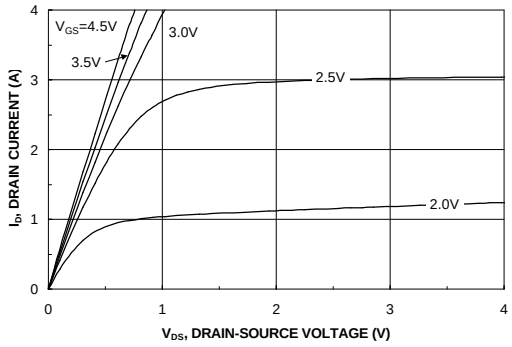



**Figure 1. On-Region Characteristics.**

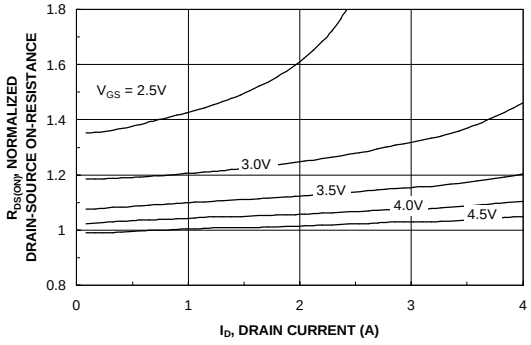



**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

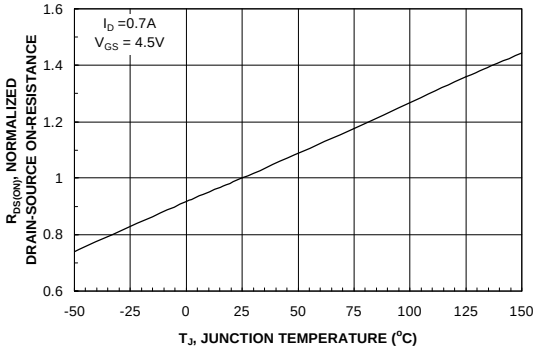



**Figure 3. On-Resistance Variation with Temperature.**

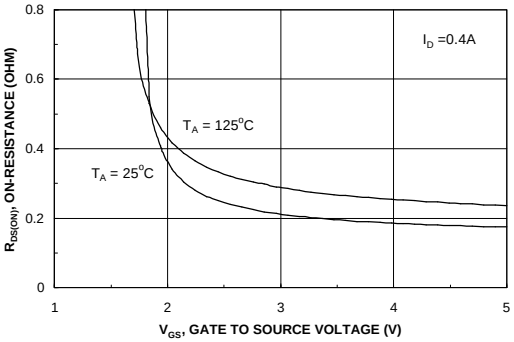



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

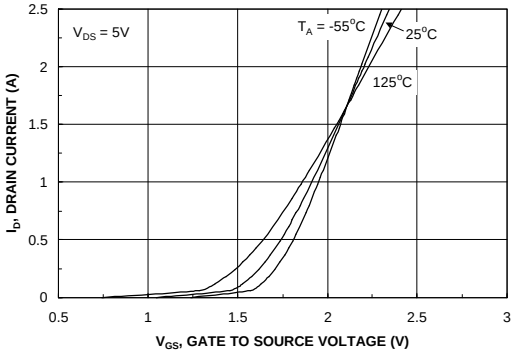



**Figure 5. Transfer Characteristics.**

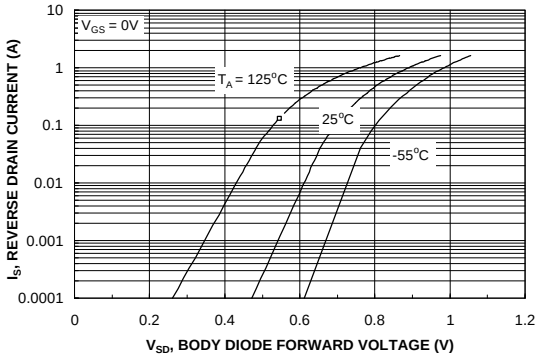



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Characteristics: N-Channel

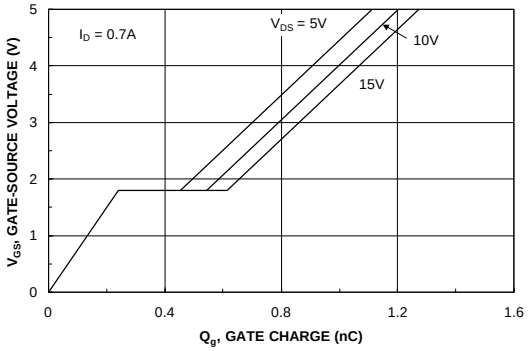



**Figure 7. Gate Charge Characteristics.**

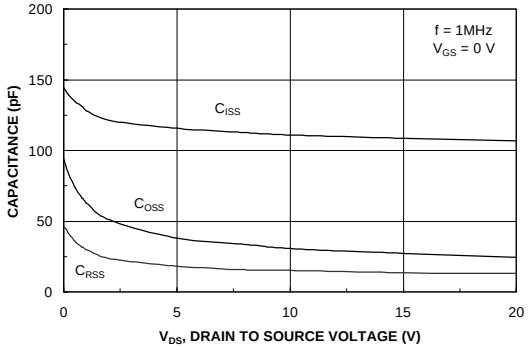



**Figure 8. Capacitance Characteristics.**

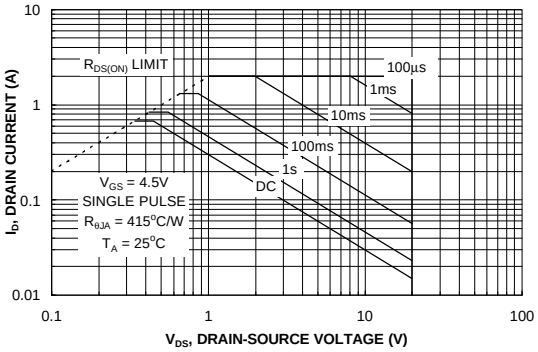



**Figure 9. Maximum Safe Operating Area.**

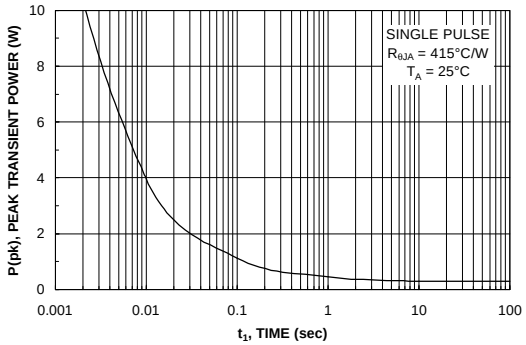



**Figure 10. Single Pulse Maximum Power Dissipation.**

## Typical Characteristics: P-Channel

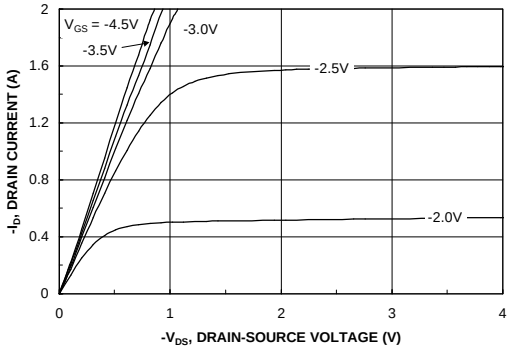



**Figure 11. On-Region Characteristics.**

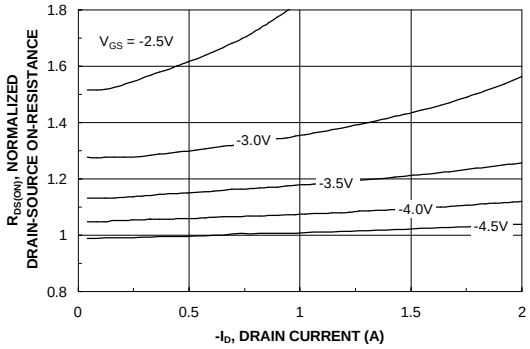



**Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.**

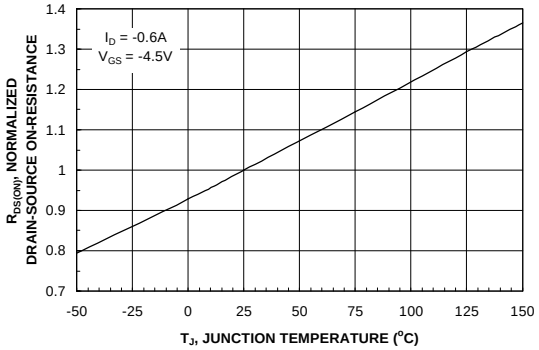



**Figure 13. On-Resistance Variation with Temperature.**

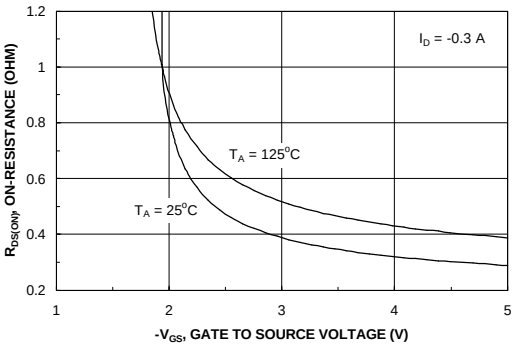



**Figure 14. On-Resistance Variation with Gate-to-Source Voltage.**

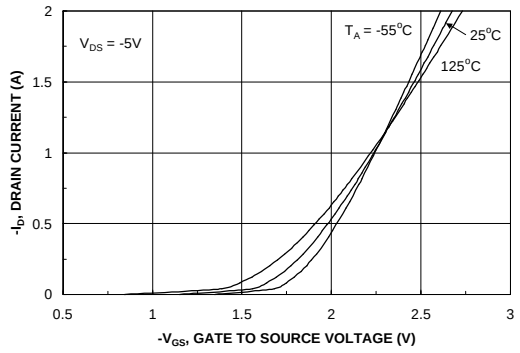



**Figure 15. Transfer Characteristics.**

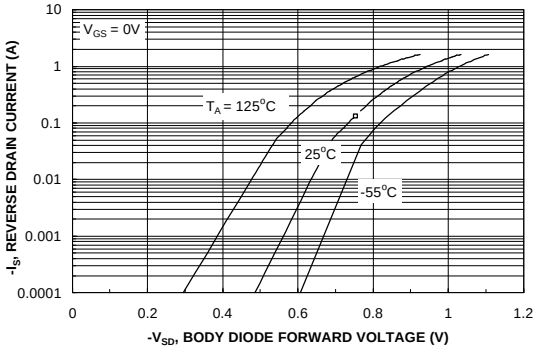



**Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Characteristics: P-Channel

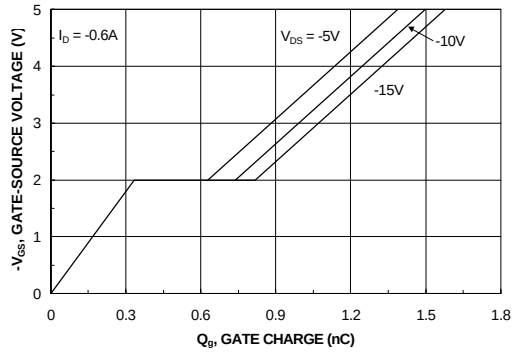



**Figure 17. Gate Charge Characteristics.**

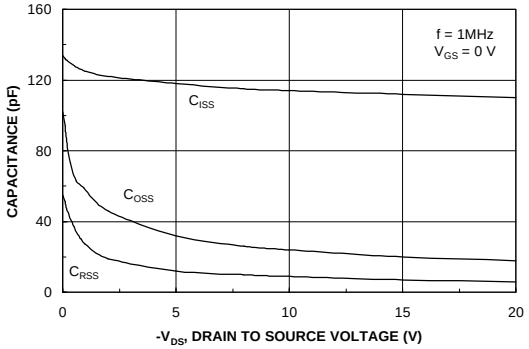



**Figure 18. Capacitance Characteristics.**

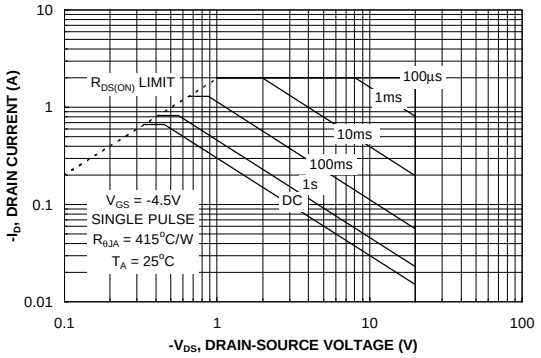



**Figure 19. Maximum Safe Operating Area.**

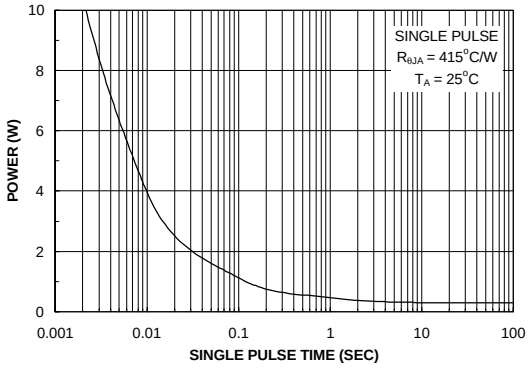



**Figure 20. Single Pulse Maximum Power Dissipation.**

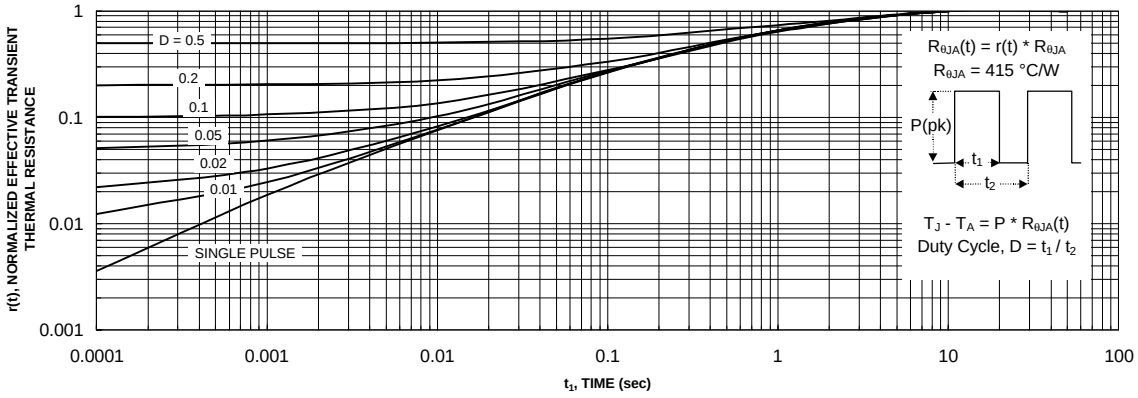
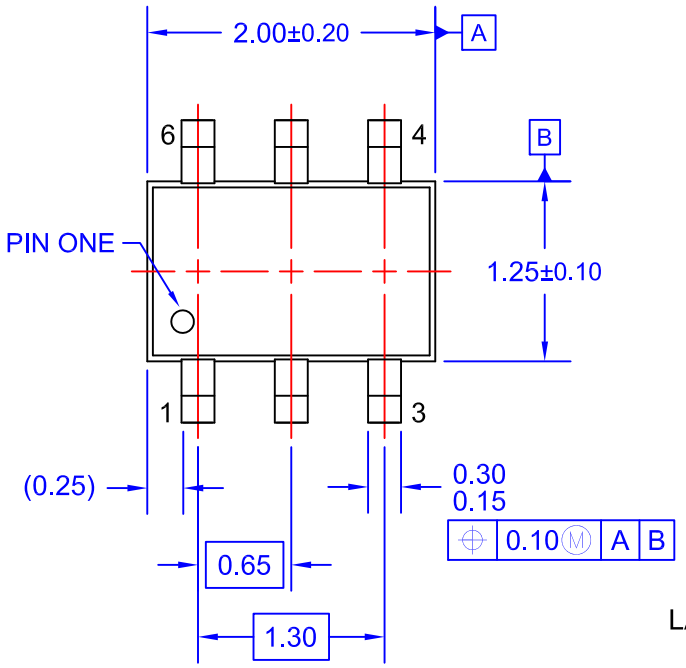
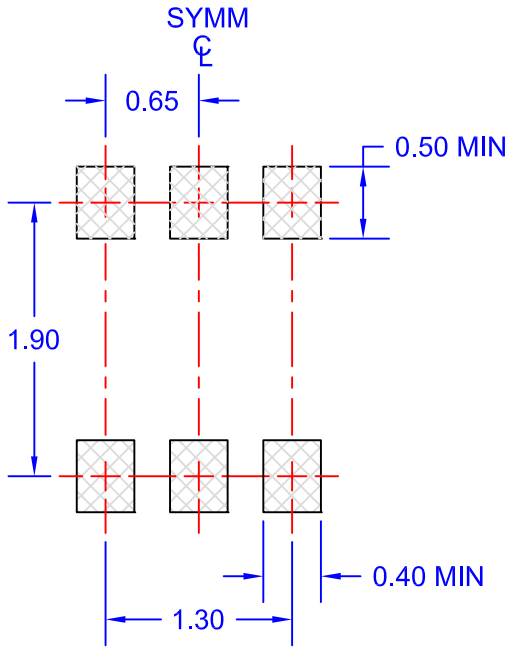


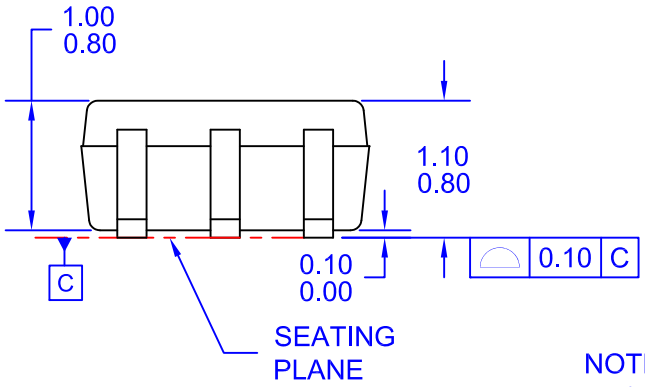

**Figure 21. Transient Thermal Response Curve.**

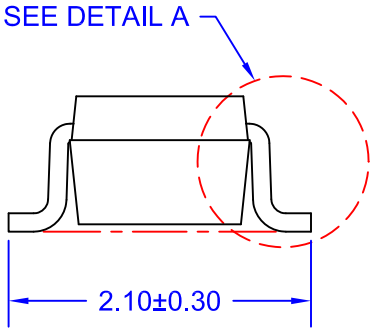
**Thermal characterization performed using the conditions described in Note 1.**
**Transient thermal response will change depending on the circuit board design.**




LAND PATTERN RECOMMENDATION




NOTES: UNLESS OTHERWISE SPECIFIED

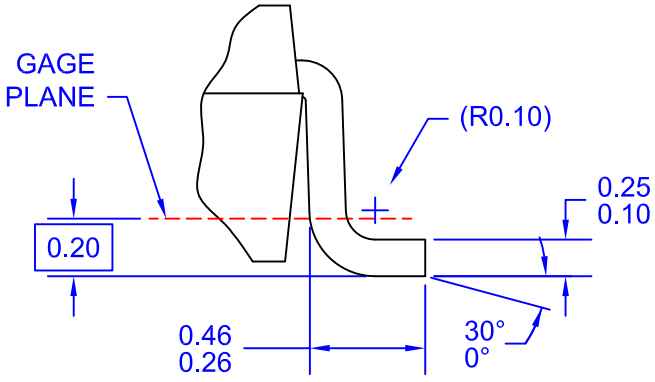
A) THIS PACKAGE CONFORMS TO EIAJ SC-88, 1996.

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.

D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009

E) DRAWING FILENAME: MKT-MAA06AREV7




DETAIL A
SCALE: 60X

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## PRODUCT STATUS DEFINITIONS

### Definition of Terms

| Datasheet Identification | Product Status | Definition |
|---|---|---|
| Advance Information | Formative / In Design | Datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design. |
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Rev. I77