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FDMS86163P

P-Channel PowerTrench[®] MOSFET

-100 V, -50 A, 22 mΩ

Features

- Max $r_{DS(on)}$ = 22 mΩ at $V_{GS} = -10$ V, $I_D = -7.9$ A
- Max $r_{DS(on)}$ = 30 mΩ at $V_{GS} = -6$ V, $I_D = -5.9$ A
- Very low RDS-on mid voltage P-channel silicon technology optimised for low Qg
- This product is optimised for fast switching applications as well as load switch applications
- 100% UIL tested
- RoHS Compliant

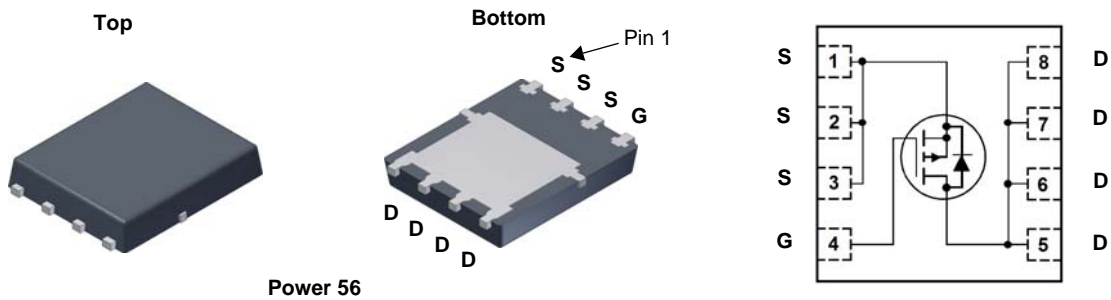


General Description

This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench[®] process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Applications

- Active Clamp Switch
- Load Switch



MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Conditions	Rated Value	Units
V_{DS}	Drain to Source Voltage		-100	V
V_{GS}	Gate to Source Voltage		±25	V
I_D	Drain Current	-Continuous $T_C = 25$ °C	-50	A
		-Continuous $T_A = 25$ °C (Note 1a)	-7.9	
		-Pulsed (Note 4)	-100	
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	486	mJ
P_D	Power Dissipation	$T_C = 25$ °C	104	W
		$T_A = 25$ °C (Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		1.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS86163P	FDMS86163P	Power 56	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = -250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	-100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		-59		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -80\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 25\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250\text{ }\mu\text{A}$	-2	-2.8	-4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		6.2		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -10\text{ V}, I_D = -7.9\text{ A}$		17.8	22	m Ω
		$V_{GS} = -6\text{ V}, I_D = -5.9\text{ A}$		21.3	30	
		$V_{GS} = -10\text{ V}, I_D = -7.9\text{ A}, T_J = 125\text{ }^\circ\text{C}$		29	36	
g_{FS}	Forward Transconductance	$V_{DS} = -10\text{ V}, I_D = -7.9\text{ A}$		29		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -50\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		3070	4085	pF
C_{oss}	Output Capacitance			501	670	pF
C_{rss}	Reverse Transfer Capacitance			21	35	pF
R_g	Gate Resistance		0.1	2.6	5.3	Ω

Switching Characteristics

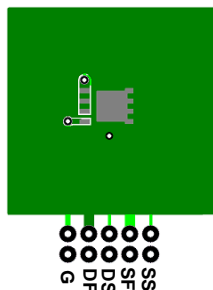
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -50\text{ V}, I_D = -7.9\text{ A}, V_{GS} = -10\text{ V}, R_{GEN} = 6\text{ }\Omega$		17	30	ns	
t_r	Rise Time			8.8	18	ns	
$t_{d(off)}$	Turn-Off Delay Time			33	53	ns	
t_f	Fall Time			6.9	14	ns	
Q_g	Total Gate Charge		$V_{GS} = 0\text{ V to } -10\text{ V}$		42	59	nC
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V to } -6\text{ V}$	$V_{DD} = -50\text{ V}, I_D = -7.9\text{ A}$		26	37	nC
Q_{gs}	Gate to Source Charge				11.8		nC
Q_{gd}	Gate to Drain "Miller" Charge				7.1		nC

Drain-Source Diode Characteristics

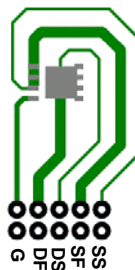
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -7.9\text{ A}$ (Note 2)		-0.81	-1.3	V
		$V_{GS} = 0\text{ V}, I_S = -2\text{ A}$ (Note 2)		-0.75	-1.2	
t_{rr}	Reverse Recovery Time	$I_F = -7.9\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		63	102	ns
Q_{rr}	Reverse Recovery Charge			132	210	nC

Notes:

- $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $50\text{ }^\circ\text{C/W}$ when mounted on a 1 in² pad of 2 oz copper



b) $125\text{ }^\circ\text{C/W}$ when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

3. Starting $T_J = 25\text{ }^\circ\text{C}$; P-ch: L = 3 mH, $I_{AS} = -18\text{ A}$, $V_{DD} = -100\text{ V}$, $V_{GS} = -10\text{ V}$. 100% test at L = 0.1 mH, $I_{AS} = -58\text{ A}$.

4. Pulse Id refers to Figure.11 Forward Bias Safe Operation Area.

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

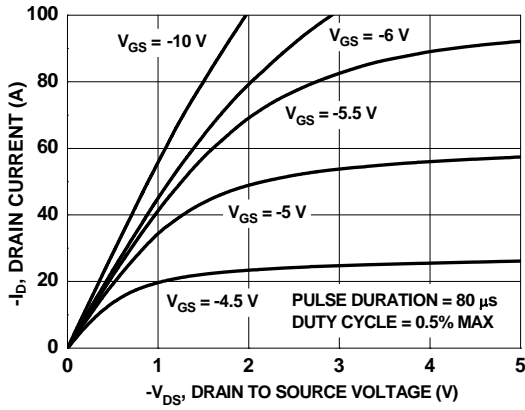


Figure 1. On Region Characteristics

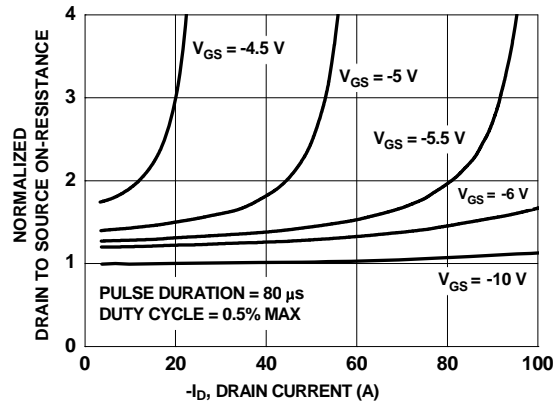


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

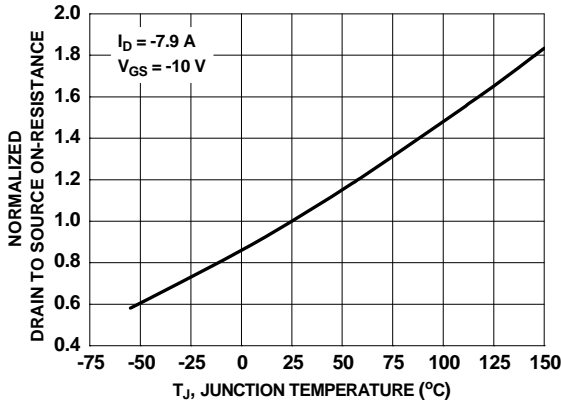


Figure 3. Normalized On Resistance vs Junction Temperature

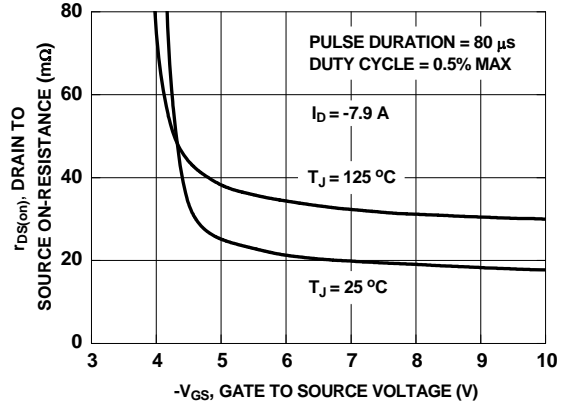


Figure 4. On-Resistance vs Gate to Source Voltage

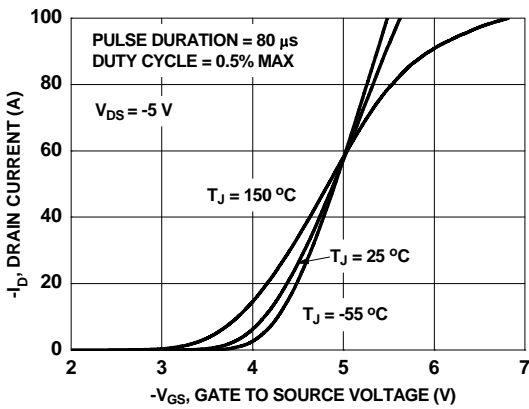


Figure 5. Transfer Characteristics

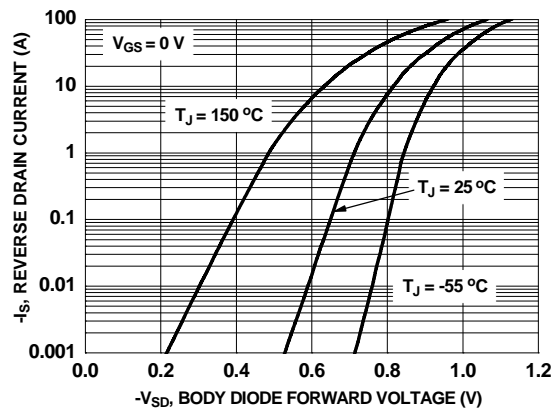


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

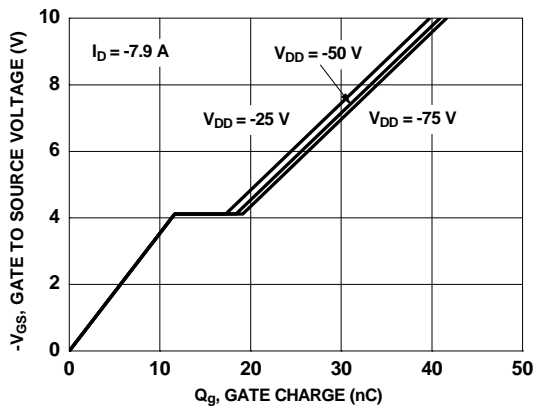


Figure 7. Gate Charge Characteristics

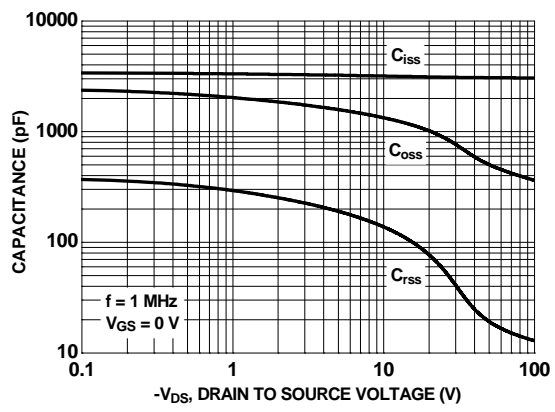


Figure 8. Capacitance vs Drain to Source Voltage

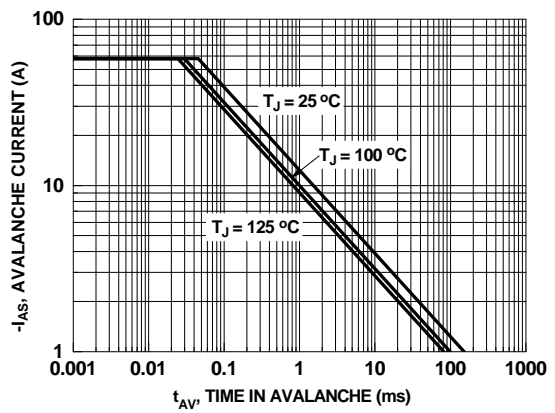


Figure 9. Unclamped Inductive Switching Capability

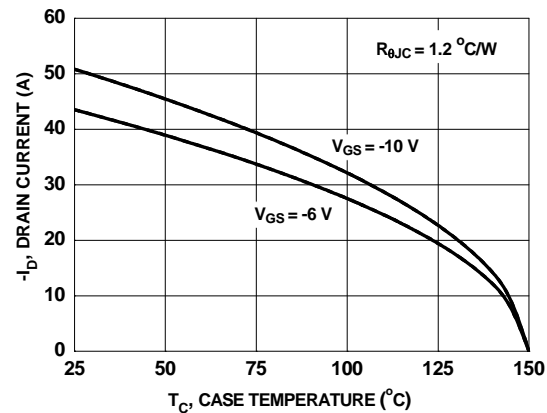


Figure 10. Maximum Continuous Drain Current vs Case Temperature

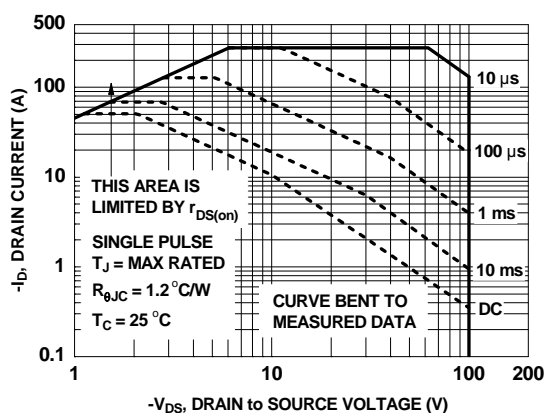


Figure 11. Forward Bias Safe Operating Area

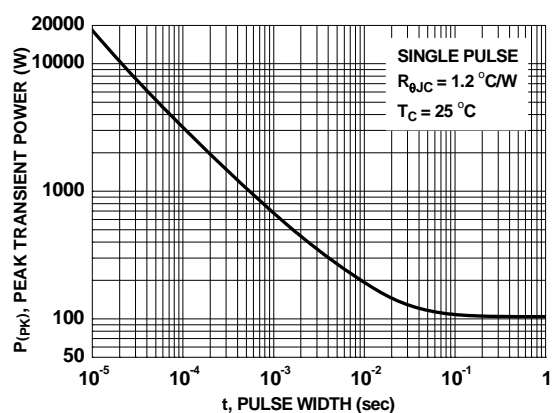


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

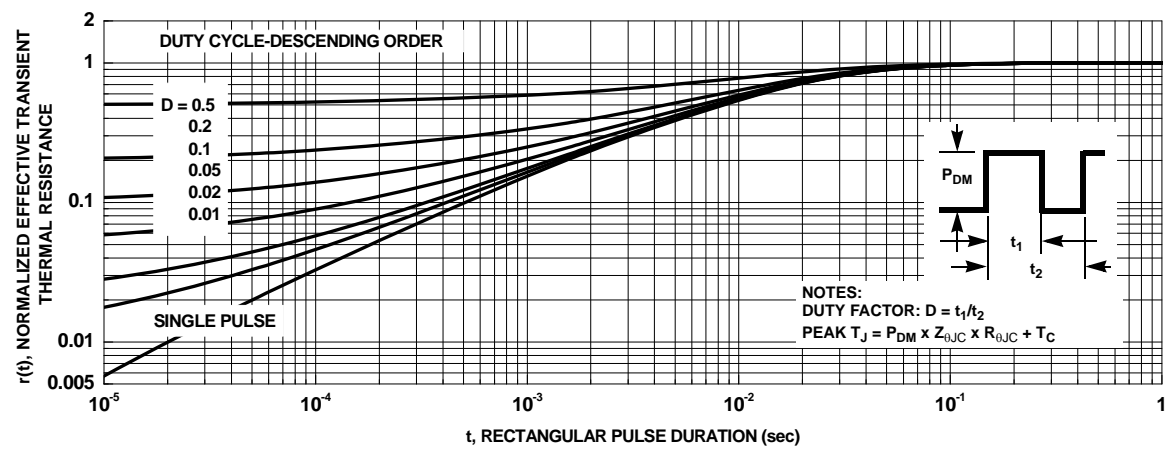
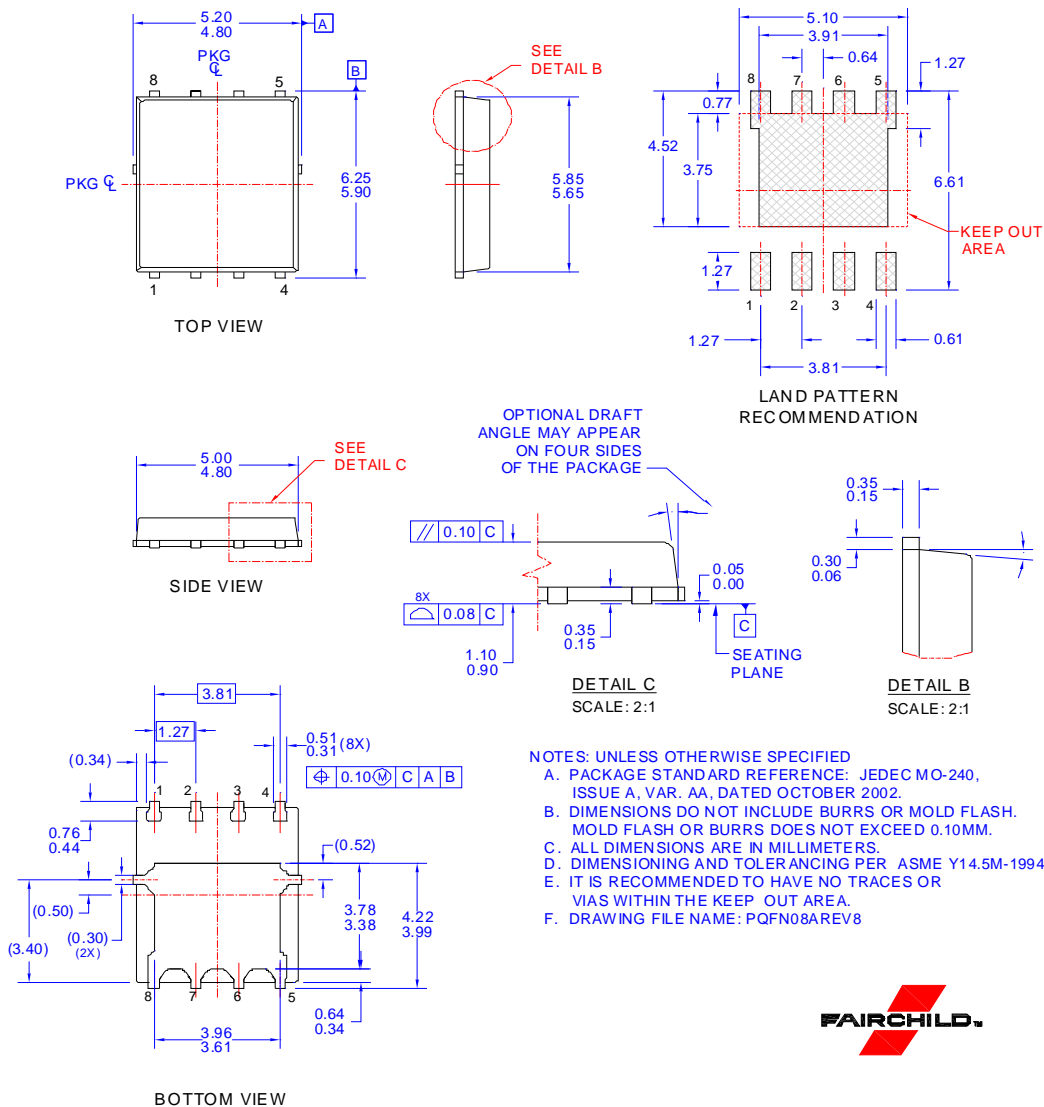


Figure 13. Junction-to-Case Transient Thermal Response Curve

Dimensional Outline and Pad Layout




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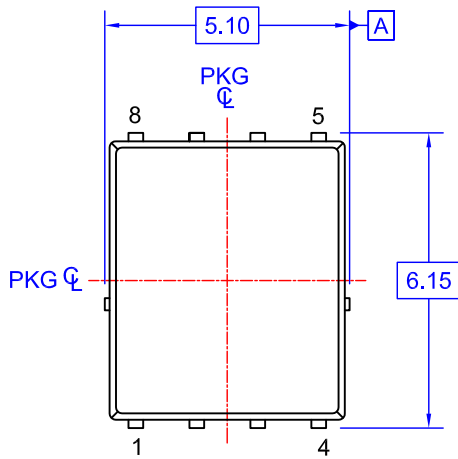
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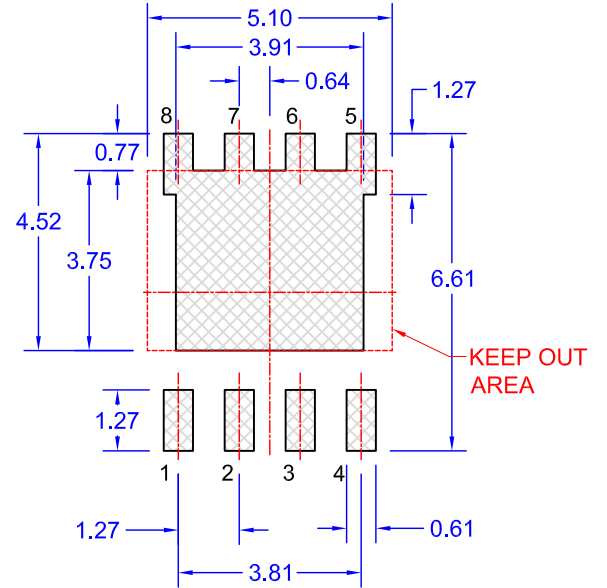
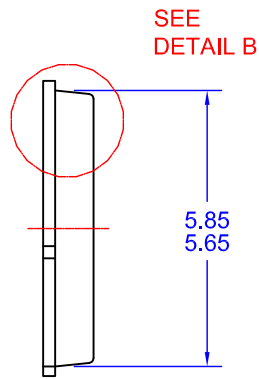
PRODUCT STATUS DEFINITIONS

Definition of Terms

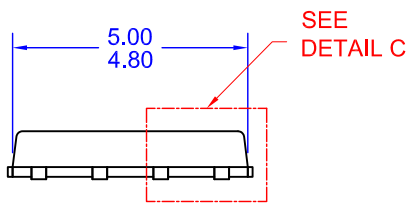
Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.



TOP VIEW

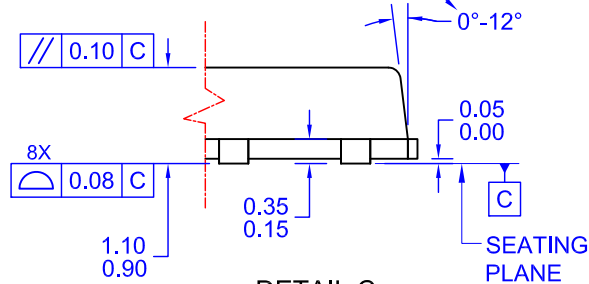


LAND PATTERN RECOMMENDATION

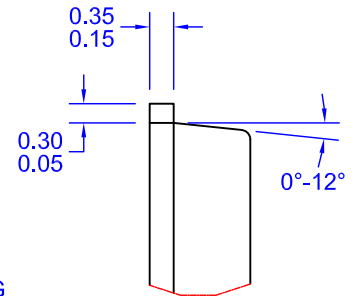


SIDE VIEW

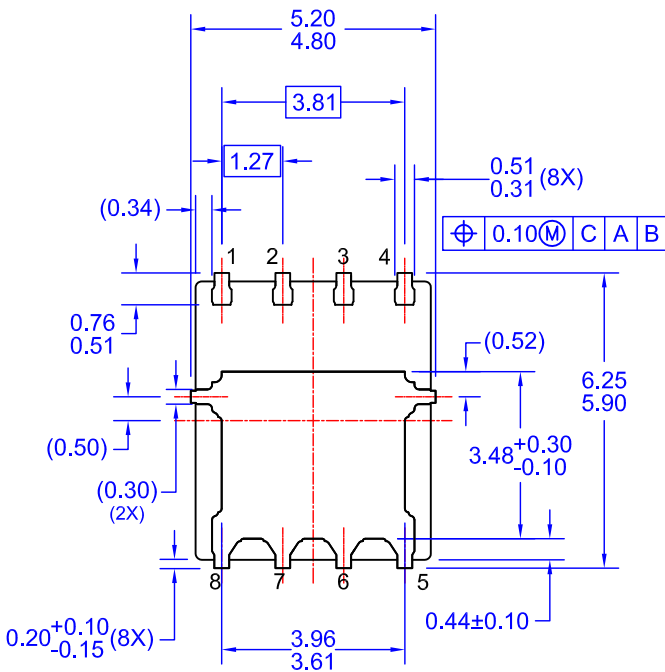
OPTIONAL DRAFT ANGLE MAY APPEAR ON FOUR SIDES OF THE PACKAGE



DETAIL C
SCALE: 2:1



DETAIL B
SCALE: 2:1



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED






- A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA, DATED OCTOBER 2002.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
- F. DRAWING FILE NAME: PQFN08AREV10





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ANTI-COUNTERFEITING POLICY

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Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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