



Is Now Part of



**ON Semiconductor®**

To learn more about ON Semiconductor, please visit our website at  
[www.onsemi.com](http://www.onsemi.com)

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## 74VHC00 Quad 2-Input NAND Gate

### Features

- High Speed:  $t_{PD} = 3.7\text{ns}$  (typ.) at  $T_A = 25^\circ\text{C}$
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (min.)
- Power down protection is provided on all inputs
- Low noise:  $V_{OLP} = 0.8\text{V}$  (max)
- Low power dissipation:  $I_{CC} = 2\mu\text{A}$  (max.) at  $T_A = 25^\circ\text{C}$
- Pin and function compatible with 74HC00


### General Description

The VHC00 is an advanced high-speed CMOS 2-Input NAND Gate fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The internal circuit is composed of 3 stages, including buffer output, which provide high noise immunity and stable output. An input protection circuit insures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

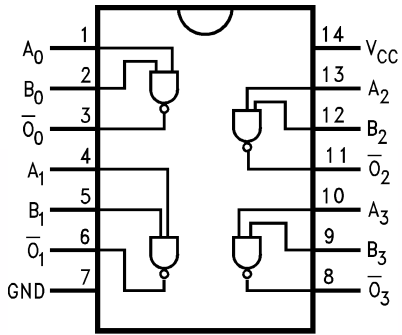
### Ordering Information

Order Number	Package Number	Package Description
74VHC00M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHC00SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC00MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC00N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

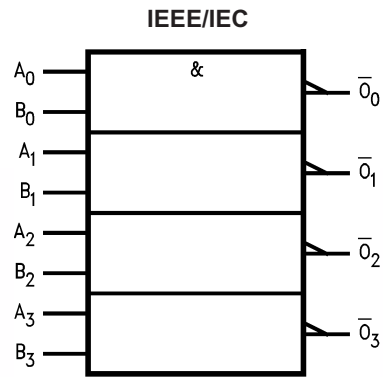
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

 All packages are lead free per JEDEC: J-STD-020B standard.

### Connection Diagram



### Logic Symbol



### Pin Description

Pin Names	Description
$A_n, B_n$	Inputs
$\bar{O}_n$	Outputs

### Truth Table

A	B	$\bar{O}$
L	L	H
L	H	H
H	L	H
H	H	L

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	-0.5V to +7.0V
$V_{IN}$	DC Input Voltage	-0.5V to +7.0V
$V_{OUT}$	DC Output Voltage	-0.5V to $V_{CC} + 0.5V$
$I_{IK}$	Input Diode Current	-20mA
$I_{OK}$	Output Diode Current	$\pm 20mA$
$I_{OUT}$	DC Output Current	$\pm 25mA$
$I_{CC}$	DC $V_{CC}$ /GND Current	$\pm 50mA$
$T_{STG}$	Storage Temperature	-65°C to +150°C
$T_L$	Lead Temperature (Soldering, 10 seconds)	260°C

## Recommended Operating Conditions<sup>(1)</sup>

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	2.0V to +5.5V
$V_{IN}$	Input Voltage	0V to +5.5V
$V_{OUT}$	Output Voltage	0V to $V_{CC}$
$T_{OPR}$	Operating Temperature	-40°C to +85°C
$t_r, t_f$	Input Rise and Fall Time, $V_{CC} = 3.3V \pm 0.3V$ $V_{CC} = 5.0V \pm 0.5V$	0ns/V ~ 100ns/V 0ns/V ~ 20ns/V

### Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

## DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to +85°C		Units	
				Min.	Typ.	Max.	Min.	Max.		
V <sub>IH</sub>	HIGH Level Input Voltage	2.0		1.50			1.50		V	
		3.0–5.5		0.7 × V <sub>CC</sub>			0.7 × V <sub>CC</sub>			
V <sub>IL</sub>	LOW Level Input Voltage	2.0				0.50		0.50	V	
		3.0–5.5				0.3 × V <sub>CC</sub>		0.3 × V <sub>CC</sub>		
V <sub>OH</sub>	HIGH Level Output Voltage	2.0	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50μA	1.9	2.0		1.9		V
		3.0			2.9	3.0		2.9		
		4.5			4.4	4.5		4.4		
		3.0		I <sub>OH</sub> = -4mA	2.58			2.48		
		4.5		I <sub>OH</sub> = -8mA	3.94			3.80		
V <sub>OL</sub>	LOW Level Output Voltage	2.0	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50μA		0.0	0.1		0.1	V
		3.0				0.0	0.1		0.1	
		4.5				0.0	0.1		0.1	
		3.0		I <sub>OL</sub> = 4mA			0.36		0.44	
		4.5		I <sub>OL</sub> = 8mA			0.36		0.44	
I <sub>IN</sub>	Input Leakage Current	0–5.5	V <sub>IN</sub> = 5.5V or GND			±0.1		±1.0	μA	
I <sub>CC</sub>	Quiescent Supply Current	5.5	V <sub>IN</sub> = V <sub>CC</sub> or GND			2.0		20.0	μA	

## Noise Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = 25°C		Units
				Typ.	Limits	
V <sub>OLP</sub> <sup>(2)</sup>	Quiet Output Maximum Dynamic V <sub>OL</sub>	5.0	C <sub>L</sub> = 50pF	0.3	0.8	V
V <sub>OLV</sub> <sup>(2)</sup>	Quiet Output Minimum Dynamic V <sub>OL</sub>	5.0	C <sub>L</sub> = 50pF	-0.3	-0.8	V
V <sub>IHD</sub> <sup>(2)</sup>	Minimum HIGH Level Dynamic Input Voltage	5.0	C <sub>L</sub> = 50pF		3.5	V
V <sub>ILD</sub> <sup>(2)</sup>	Maximum LOW Level Dynamic Input Voltage	5.0	C <sub>L</sub> = 50pF		1.5	V

**Note:**

2. Parameter guaranteed by design.

## AC Electrical Characteristics

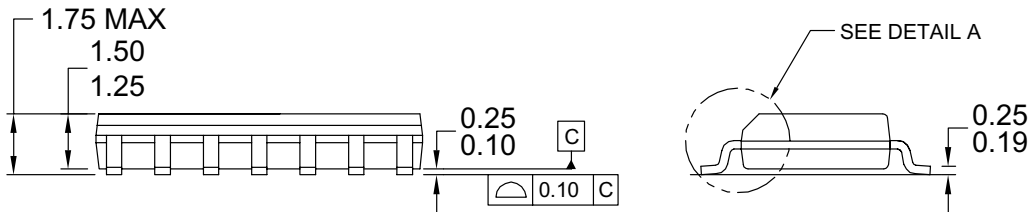
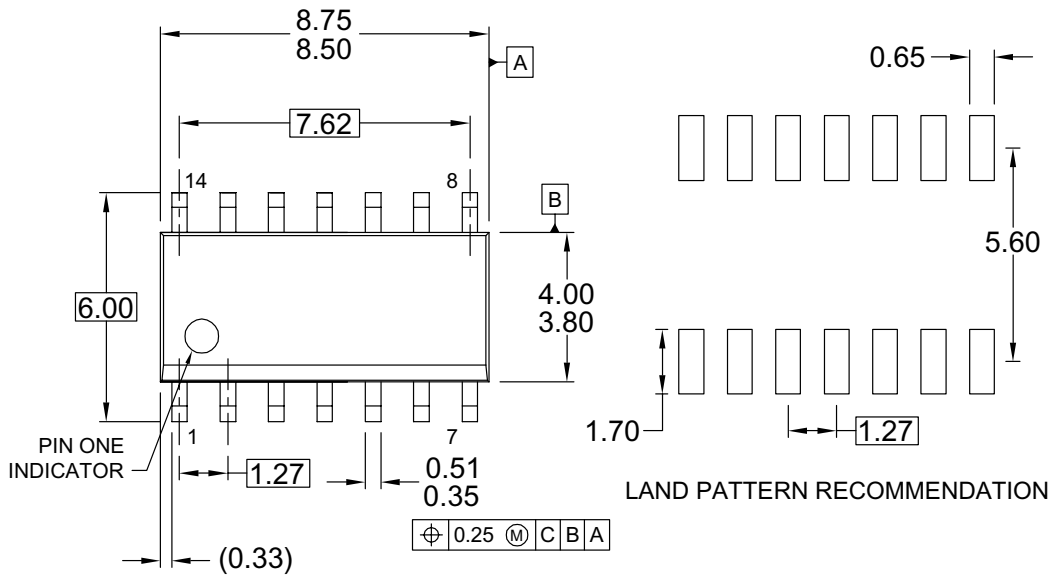
Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay	3.3 ± 0.3	C <sub>L</sub> = 15pF		5.5	7.9	1.0	9.5	ns
			C <sub>L</sub> = 50pF		8.0	11.4	1.0	13.0	
		5.0 ± 0.5	C <sub>L</sub> = 15pF		3.7	5.5	1.0	6.5	ns
			C <sub>L</sub> = 50pF		5.2	7.5	1.0	8.5	
C <sub>IN</sub>	Input Capacitance		V <sub>CC</sub> = Open		4	10		10	pF
C <sub>PD</sub>	Power Dissipation Capacitance		<sup>(3)</sup>		19				pF

**Note:**

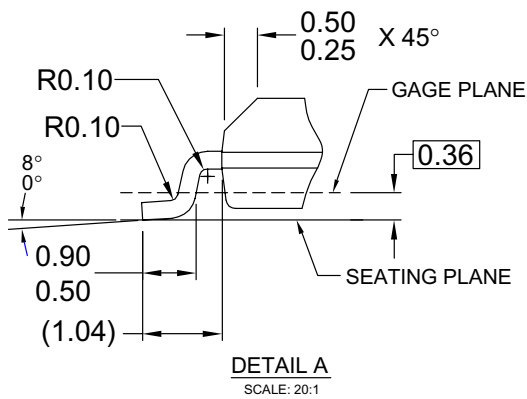
3. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 4 \text{ (per gate).}$$

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED



- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C,
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X145-14M
- E) DRAWING CONFORMS TO ASME Y14.5M-1994
- F) DRAWING FILE NAME: M14AREV13

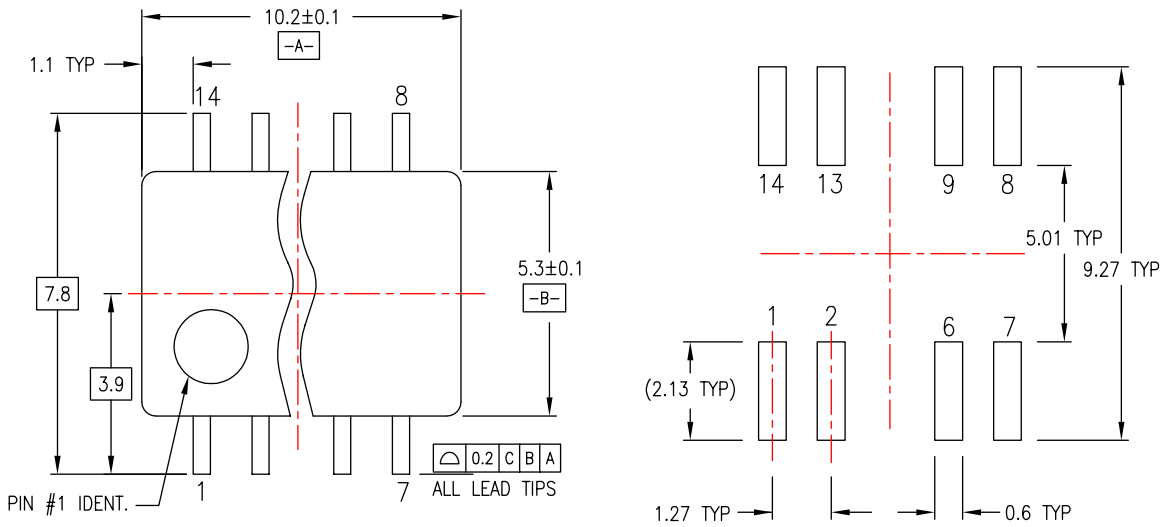
Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

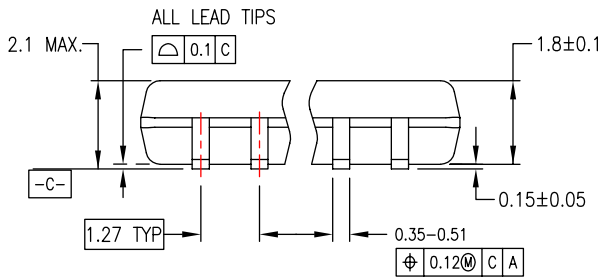
Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>

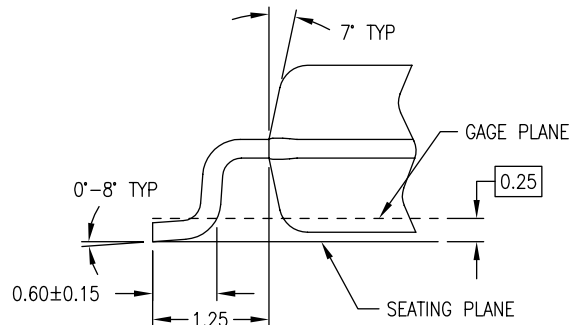
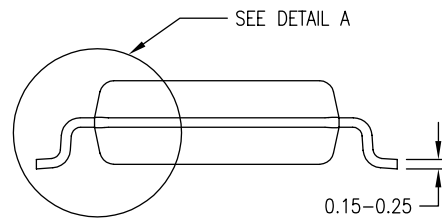
Physical Dimensions (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



DETAIL A

NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DREVC

Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

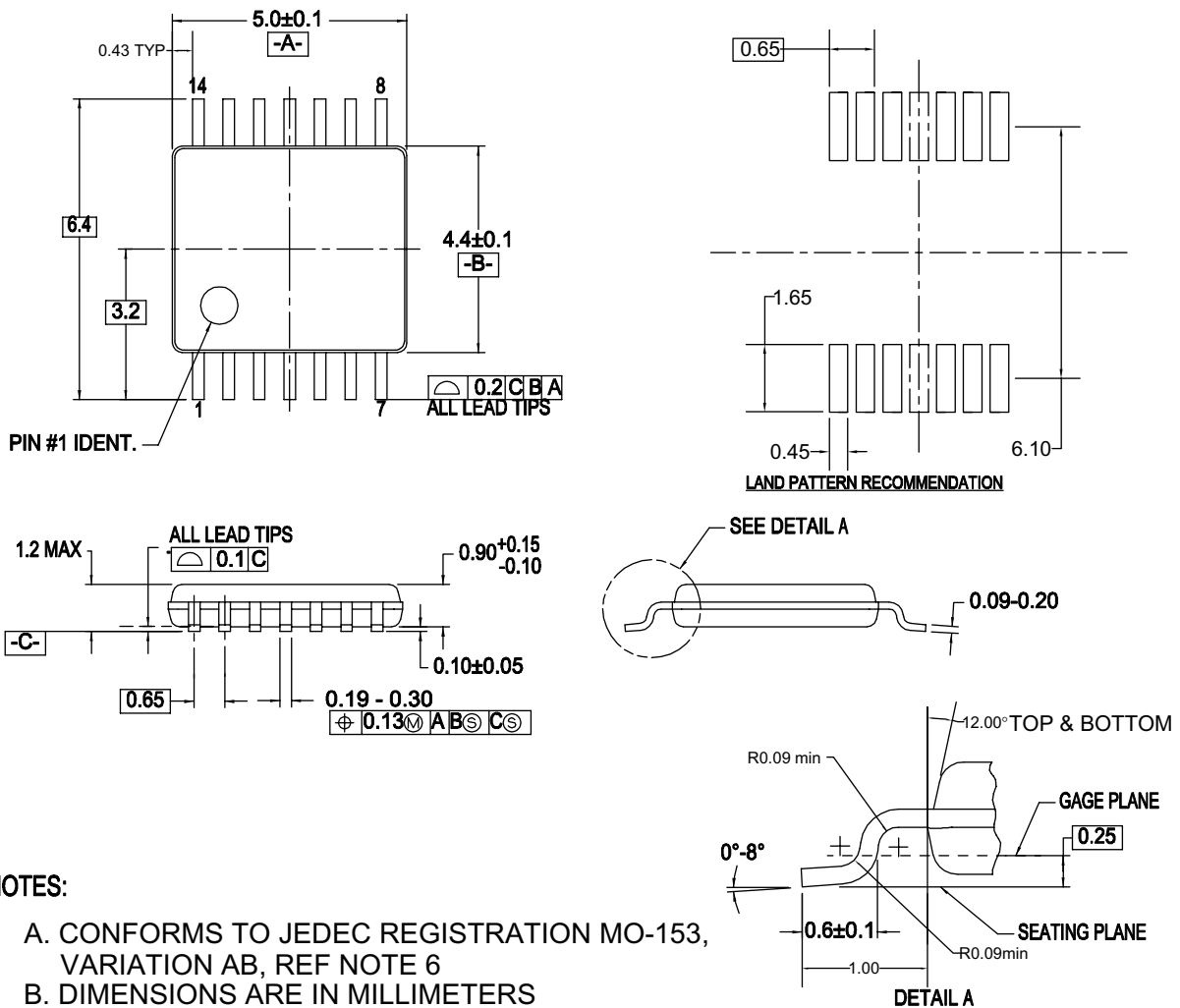
Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>



Physical Dimensions (Continued)



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
- E. LANDPATTERN STANDARD: SOP65P640X110-14M
- F. DRAWING FILE NAME: MTC14REV6

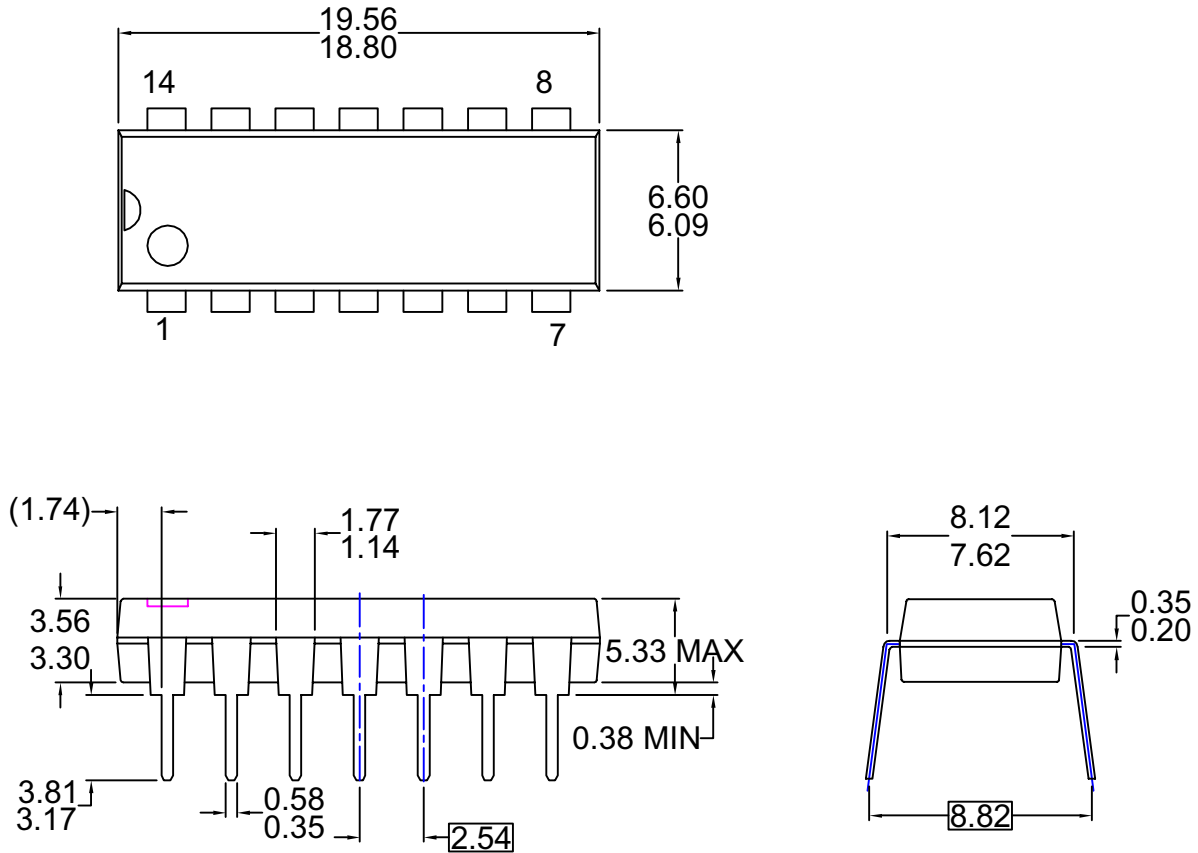
Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>

Physical Dimensions (Continued)



- NOTES: UNLESS OTHERWISE SPECIFIED**  
**THIS PACKAGE CONFORMS TO**  
**A) JEDEC MS-001 VARIATION BA**  
**B) ALL DIMENSIONS ARE IN MILLIMETERS.**  
**C) DIMENSIONS ARE EXCLUSIVE OF BURRS,**  
**MOLD FLASH, AND TIE BAR EXTRUSIONS.**  
**D) DIMENSIONS AND TOLERANCES PER**  
**ASME Y14.5-1994**  
**E) DRAWING FILE NAME: MKT-N14AREV7**

**Figure 4. 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide**

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.



Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>



**TRADEMARKS**

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

- |   |                        |                            |                      |
|---|------------------------|----------------------------|----------------------|
| ACEx®   | FPST™                  | PDP-SPM™                   | SyncFET™             |
| Build it Now™   | FRFET®                 | Power220®                  | SYSTEM GENERAL®      |
| CorePLUS™   | Global Power Resource™ | Power247®                  | The Power Franchise® |
| CROSSVOLT™  | Green FPS™             | POWEREDGE®                 | the power®           |
| CTL™  | Green FPS™ e-Series™   | Power-SPM™                 | franchise            |
| Current Transfer Logic™   | GTO™                   | PowerTrench®               | TinyBoost™           |
| EcoSPARK®   | i-Lo™                  | Programmable Active Droop™ | TinyBuck™            |
| EZSWITCH™ *   | IntelliMAX™            | QFET®                      | TinyLogic®           |
|  ™ | ISOPLANAR™             | QST™                       | TINYOPTO™            |
|  ™ | MegaBuck™              | QT Optoelectronics™        | TinyPower™           |
| Fairchild®  | MICROCOUPLER™          | Quiet Series™              | TinyPWM™             |
| Fairchild Semiconductor®  | MicroFET™              | RapidConfigure™            | TinyWire™            |
| FACT Quiet Series™  | MicroPak™              | SMART START™               | µSerDes™             |
| FACT®   | MillerDrive™           | SPM®                       | UHC®                 |
| FAST®   | Motion-SPM™            | STEALTH™                   | Ultra FRFET™         |
| FastvCore™ *  | OPTOLOGIC®             | SuperFET™                  | UniFET™              |
| FlashWriter® *  | OPTOPLANAR®            | SuperSOT™-3                | VCX™                 |
|   |                        | SuperSOT™-6                |                      |
|   |                        | SuperSOT™-8                |                      |

\* EZSWITCH™ and FlashWriter® are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

**DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Rev. I32