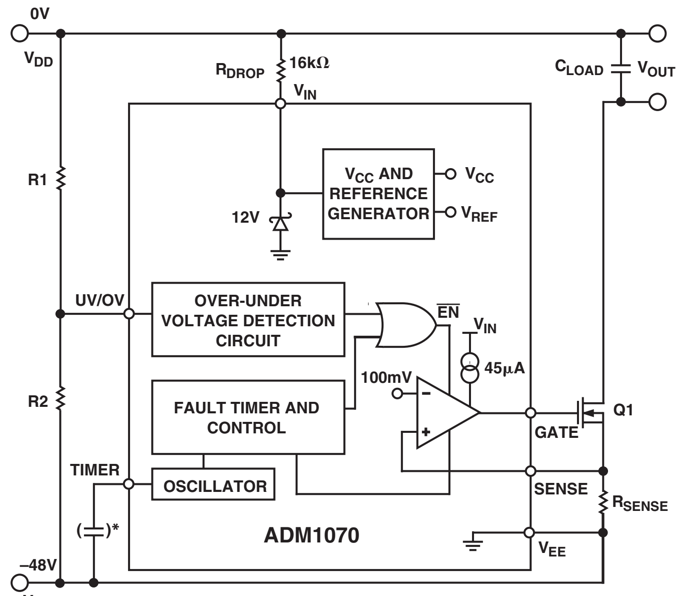
# –48 V Hot Swap Controller

# ADM1070

**FEATURES**
- Allows Safe Board Insertion and Removal from a Live –48 V Backplane
- Typically Operates from –36 V to –80 V
- Tolerates Transients up to –200 V (Limited by External Components)
- Accurate Programmable Linear Current Limit for In-Rush Control and Short Circuit Protection
- Programmable Timeout in Current Limit
- Limited Consecutive Retry:
  - Auto-Restart after Current Limit Timeout
  - Shutdown after Seven Consecutive Auto Restarts
  - Provides Immunity from Step Induced Current Spikes
- Default Timing Provided with no TIMER Capacitor
- Single Pin Undervoltage/Overvoltage Detection
- Programmable Operating Voltage Window
- Programmable Undervoltage/Overvoltage Time Filter
- Small 6-Lead SOT-23 Package

**APPLICATIONS**
- Central Office Switching
- –48 V Distributed Power Systems
- Negative Power Supply Control
- Hot Board Insertion
- Electronic Circuit Breaker
- High Availability Servers
- Programmable Current Limiting Circuit
- –48 V Power Supply Modules

**FUNCTIONAL BLOCK DIAGRAM**




## GENERAL DESCRIPTION

The ADM1070 is a negative voltage hot swap controller that allows a board to be safely inserted and removed from a live –48 V backplane. The part achieves this by providing robust current limiting, protection against transient and nontransient short circuits and overvoltage and undervoltage conditions. The ADM1070 typically operates from a negative voltage of up to –80 V and can tolerate transient voltages of up to –200 V.

In-rush current is limited to a programmable value by controlling the gate drive of an external N-channel FET. The current limit can be controlled by the choice of the sense resistor, $R_{SENSE}$. Added control of the in-rush current is provided by an on-chip timer that uses pulsewidth modulation to allow the maximum current to flow for only 3% of the time. An autorestart occurs after a current limit timeout. After seven successive autorestarts, the fault will be latched and the part goes into shutdown with the result that the external FET is disabled until the power is reset.

The ADM1070 also features single-pin undervoltage and overvoltage detection. The FET is turned off if a nontransient voltage less than the undervoltage threshold, typically –36 V, or greater than the overvoltage threshold, typically –77 V, is detected on the UV/OV Pin. The operating voltage window of the ADM1070 is programmable and is determined by the ratio R1/R2.

Time filtering on the undervoltage and overvoltage detection and current limiting is programmable via the TIMER Pin. An external capacitor connected between the TIMER Pin and $V_{EE}$ determines the undervoltage/overvoltage time filter and the timeout in current limit. If the pin is tied to $V_{EE}$, the time filter values and the current limit timeout revert to default figures.

The ADM1070 is fabricated using BiCMOS technology for minimal power consumption. The part is available in a small 6-Lead SOT-23 package.

REV. 0

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## Documentation

**Application Notes**

- AN-591: ADM1070 Hot Swap Controller

**Data Sheet**

- ADM1070: -48 V Hot Swap Controller Data Sheet

## Reference Materials

**Solutions Bulletins & Brochures**

- Hot Swap And Power Monitoring Bulletin

**Technical Articles**

- Hot Swap Controller Maximizes System Up-Time
- Isolation Architecture, Circuit, and Component Selection in Power Inverter Applications
- Temperature monitor measures three thermal zones

## Design Resources

- ADM1070 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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# ADM1070–SPECIFICATIONS

($V_{DD}$ = 0 V, $V_{EE}$ = –48 V, $R_{DROP}$ = 16 kΩ, $T_A$ = –40°C to +85°C, unless otherwise noted.)

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| BOARD SUPPLY (not connected directly to device) | | | | | |
| Maximum Voltage Range | –200 | –48 | –20 | V | Limited by Voltage Capability of External Components* |
| Typical Operating Voltage Range | –77 | –48 | –36 | V | $R_{DROP}$ = 16 kΩ, R1/R2 = 40* |
| VIN PIN—SHUNT REGULATOR | | | | | |
| Operating Supply Voltage Range, $V_{SS}$ | 11.5 | 12.3 | 13 | V | $I_{SS}$ = 1.5 mA to 4.25 mA |
| Quiescent Supply Current, $I_{SS}$ | 0.4 | 0.85 | 1.3 | mA | $V_{SS}$ = 11.5 V |
| Maximum Shunt Supply Voltage, $V_{SS}$ | | 12.5 | 14 | V | $I_{SS}$ = 20 mA |
| Undervoltage Lockout, $V_{LKO}$ | 7 | 8.5 | 10.5 | V | |
| UV/OV PIN—UNDERVOLTAGE AND OVERVOLTAGE DETECTION | | | | | |
| Undervoltage Falling Threshold, $V_{UVF}$ | 0.81 | 0.86 | 0.91 | V | |
| Undervoltage Rising Threshold, $V_{UVR}$ | 0.86 | 0.91 | 0.96 | V | |
| Undervoltage Hysteresis, $V_{UVH}$ | | 45 | | mV | |
| Overvoltage Falling Threshold, $V_{OVF}$ | 1.85 | 1.93 | 2.01 | V | |
| Overvoltage Rising Threshold, $V_{OVR}$ | 1.89 | 1.97 | 2.05 | V | |
| Overvoltage Hysteresis $V_{OVH}$ | | –45 | | mV | |
| Power-On Reset Delay, $t_{POR}$ | 1.10 | 1.70 | 2.30 | ms | TIMER Pin Tied to $V_{EE}$ ($V_{UVR}$ < UV/OV < $V_{OVF}$) |
| | 0.90 | 1.21 | 1.51 | ms | $C_{TIMER}$ = 470 pF ($V_{UVR}$ < UV/OV < $V_{OVF}$) |
| Voltage Fault Filter Time (UV/OV Out of Voltage Window), $t_{FLT}$ | 1.10 | 1.70 | 2.30 | ms | TIMER Pin Tied to $V_{EE}$ ($V_{UVR}$ < UV/OV < $V_{OVF}$) |
| | 0.90 | 1.21 | 1.51 | ms | $C_{TIMER}$ = 470 pF ($V_{UVR}$ < UV/OV < $V_{OVF}$)* |
| Input Current, $I_{VMON}$ | | | 1.0 | µA | |
| GATE PIN—FET DRIVER | | | | | |
| Maximum Gate Voltage, $V_{GMAX}$ | 11 | 12 | 13 | V | $I_{GATE}$ = –1 µA |
| Minimum Gate Voltage, $V_{GMIN}$ | 0 | | 50 | mV | $I_{GATE}$ = 1 µA |
| Pull-Up Current, $I_{GUP}$ | –20 | –40 | –55 | µA | $V_{GATE}$ = 0 V to 9 V, $V_{SENSE}$ = 0 |
| Pull-Down Current, $I_{GDP}$ | 10 | 30 | | mA | $V_{GATE}$ = $V_{SS}$ |
| Hold-off Impedance, $R_{GOFF}$ | | | 10 | kΩ | $V_{GATE}$ < 2 V, $V_{SS}$ > 11 V |
| | | | 30 | kΩ | $V_{GATE}$ < 2 V, $V_{SS}$ > 2 V |
| SENSE PIN—CURRENT SENSE | | | | | |
| Analog Current Limit Voltage (Rising),$V_{LIM}$ | 90 | 100 | 110 | mV | $I_{GATE}$ = 0 µA to –15 µA |
| Circuit Breaker Limit Voltage (Rising) | 75 | 88 | 100 | mV | |
| Circuit Breaker Limit Voltage (Rising) (With Respect to $V_{LIM}$), $V_{LIMITON}$ | | –12 | | mV | |
| Circuit Breaker Limit Voltage (Falling) | 60 | 79 | 95 | mV | |
| Circuit Breaker Limit Voltage (Falling) (With Respect to $V_{LIM}$), $V_{LIMITOFF}$ | | –21 | | mV | |
| Fast Current Limit Voltage | 107 | 126 | 145 | mV | |
| Fast Current Limit Voltage (With Respect to $V_{LIM}$) | | 26 | | mV | |
| Control Loop Transconductance, ($dI_{GATE}/dV_{SENSE}$) | 1.5 | 2.75 | 4 | µA/mV | $I_{GATE}$ < ±30 µA, $T_A$ = 25°C |
| Maximum Current Limit On Time, $t_{LIMITON}$ | 10 | 14 | 18 | ms | TIMER Pin Tied to $V_{EE}$ ($V_{UVR}$ < UV/OV < $V_{OVF}$) |
| | 7.4 | 9.9 | 12.4 | ms | $C_{TIMER}$ = 470 pF ($V_{UVR}$ < UV/OV < $V_{OVF}$)* |
| Current Limit PWM Off Time | 320 | 450 | 580 | ms | TIMER Pin Tied to $V_{EE}$ ($V_{UVR}$ < UV/OV < $V_{OVF}$)* |
| | 240 | 320 | 400 | ms | $C_{TIMER}$ = 470 pF ($V_{UVR}$ < UV/OV < $V_{OVF}$)* |
| Current Limit PWM Duty Cycle | | 3 | | % | (Typical Only) |
| Number of Consecutive PWM Retry Cycles | | 7 | | | (Typical Only) |

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| SENSE PIN—CURRENT SENSE (continued) | | | | | |
| Continuous Short Circuit Time before Latched Shutdown, $t_{SHORT}$ | 2100 | 2800 | 3500 | ms | TIMER Pin Tied to $V_{EE}$ ($V_{UVR}$ < UV/OV < $V_{OVF}$) |
| | 1500 | 2000 | 2500 | ms | $C_{TIMER}$ = 470 pF ($V_{UVR}$ < UV/OV < $V_{OVF}$)* |
| Operating Sense Voltage Range, $V_{SOP}$ | 0 | 0.11 | | V | |
| Input Current, $I_{SENSE}$ | –500 | | +500 | µA | $V_{SENSE}$ = –2 V to +2 V |
| TIMER PIN—TIMING CONTROL | | | | | |
| Internal Oscillator Default Frequency, $f_{TIMERINT}$ (Not Seen at Pin) | | 9.0 | | kHz | TIMER Pin Tied to $V_{EE}$ |
| External/Internal Selection Threshold, $V_{TIMERTHEI}$ | 0.3 | 0.45 | 0.6 | V | |
| High Trip Threshold, $V_{TIMERTHH}$ | 3.0 | 3.5 | 4.0 | V | |
| Low Trip Threshold, $V_{TIMERTHL}$ | 1.2 | 1.5 | 1.8 | V | |
| Pull-Down Current, $I_{TIMERDN}$ | 15 | 24 | 31 | µA | $V_{TIMER} > V_{TIMERTHH}$ |
| Pull-Up Current, $I_{TIMERUP}$ | –15 | –24 | –31 | µA | $V_{TIMERTHEI} < V_{TIMER} < V_{TIMERTHL}$ |
| Start-Up Current, $I_{TIMERSTART}$ | –12 | –19 | –26 | µA | $V_{TIMER} < V_{TIMERTHEI}$ |

*Not production tested. Guaranteed by design.

Specifications subject to change without notice.

**ABSOLUTE MAXIMUM RATINGS***

(All voltages referred to $V_{EE}$, unless otherwise noted. $T_A$ = 25°C, unless otherwise noted.)

Supply Voltage ($V_{DD}$–$V_{EE}$) . . . . . . . . . . . . . –0.3 V to –200.0 V
Maximum Shunt Supply Voltage, $V_{SS}$ . . . . . . . . . . . . . . . 16 V
SENSE Pin . . . . . . . . . . . . . . . . . . . . . . . . . . . –2 V to +16 V
GATE Pin . . . . . . . . . . . . . . . . . . . . . . . . . . –0.3 V to +16 V
UV/OV Pin . . . . . . . . . . . . . . . . . . . . . . . . . –0.3 V to +15 V
TIMER Pin . . . . . . . . . . . . . . . . . . . . . . . . . –0.3 V to +10 V
Maximum Junction Temperature . . . . . . . . . . . . . . . . . 125°C
Temperature Range . . . . . . . . . . . . . . . . . . . . –40°C to +85°C
Continuous Power Dissipation . . . . . . . . . . . . . . . . . 282 mW
Storage Temperature Range . . . . . . . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . . . . . . . . . 300°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**THERMAL CHARACTERISTICS**

6-Lead SOT-23 Package:
$\theta_{JA}$ = 226.6°C/W, $\theta_{JC}$ = 91.99°C/W

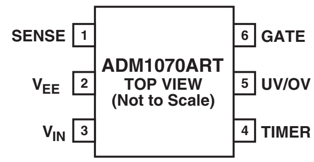
**ORDERING GUIDE**

| Model | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADM1070ART | –40°C to +85°C | 6-Lead | RT-6 |

**CAUTION**

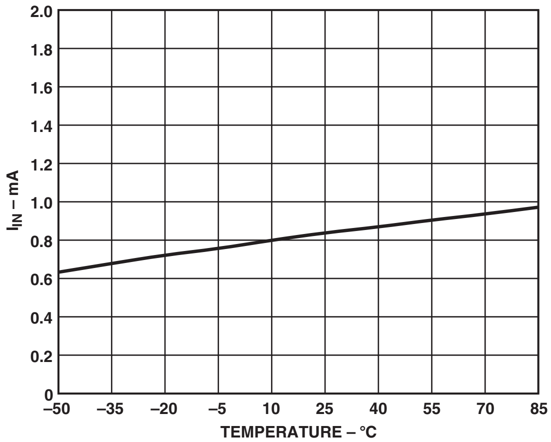
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM1070 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION

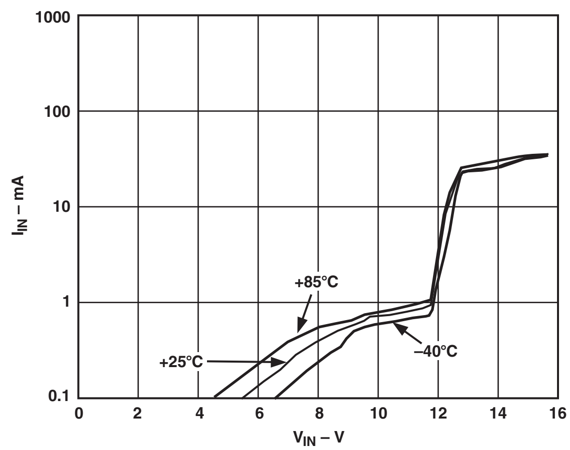



## PIN FUNCTION DESCRIPTION

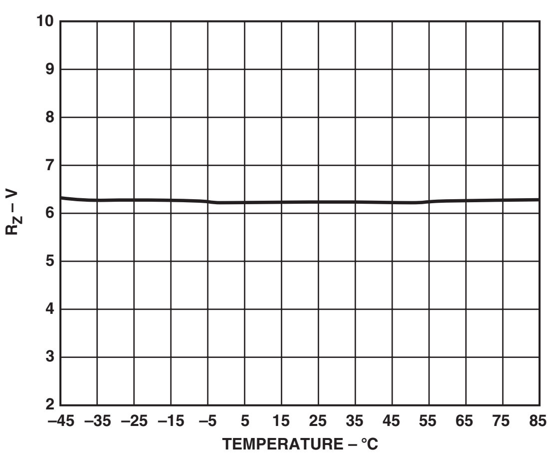
| Pin No. | Mnemonic | Function |
|---|---|---|
| 1 | SENSE | Connection to External FET Source Voltage. A sense resistor is connected in the supply path between the SENSE Pin and $V_{EE}$, and the voltage across this resistor is monitored to detect current faults. This voltage is fed as an input to the linear current regulator. When it reaches 100 mV for a specified period, $t_{ON}$, the regulator reduces the gate voltage and drives the FET as a linear pass device. If current monitoring is not required, this feature can be turned off by shorting the SENSE Pin and $V_{EE}$ together. |
| 2 | $V_{EE}$ | Device Negative Supply Voltage. This pin should be connected to the lower potential of the power supply. |
| 3 | $V_{IN}$ | Shunt Regulated On-Chip Supply, Nominally $V_{EE}$ + 12.3 V. This pin should be current fed through a dropper resistor that is connected to the higher potential of the power supply inputs. |
| 4 | TIMER | Allows User Control over Timing Functions by Determining Frequency of Oscillator. Frequency set by connecting external capacitor to $V_{EE}$. Tying pin directly to $V_{EE}$ causes oscillator to default to internally set value. |
| 5 | UV/OV | Input Pin for Overvoltage and Undervoltage Detection Circuitry. The voltage appearing on the UV/OV Pin is proportional to board supply and is determined by external resistors. When the voltage on UV/OV falls below the undervoltage threshold of 0.86 V, the GATE Pin is driven low. When the voltage appearing at the UV/OV Pin rises above the overvoltage threshold of 1.97 V, the GATE Pin is also driven low. If the external resistor ratio of R1/R2 = 40 is used, then this gives an operating range of –36 V to –77 V. |
| 6 | GATE | Output to External FET Gate Drive. Controlled by linear current regulator. The gate is driven low if an overvoltage or undervoltage fault occurs or if a current fault lasts for longer than the time, $t_{ON}$. When in linear regulation, the GATE Pin voltage is controlled as part of the servo loop. No external compensation is required. When the FET is fully enhanced and the load capacitance has been charged, the GATE Pin reaches a high level of typically 12 V. |



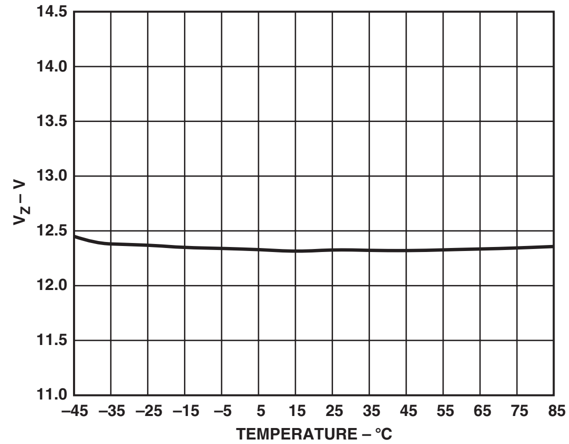

TPC 1. $I_{IN}$ vs. Temperature



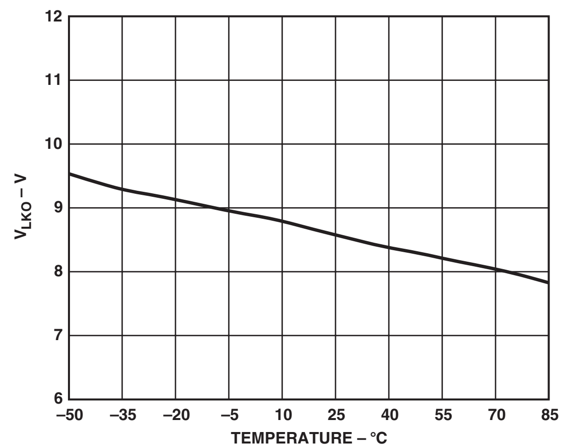

TPC 2. $I_{IN}$ vs. $V_{IN}$



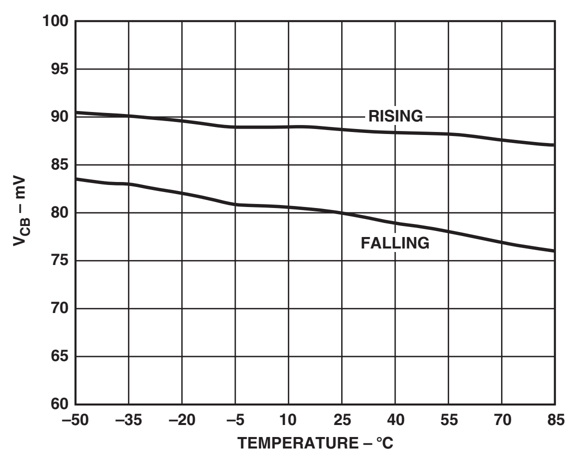

TPC 3. $R_Z$ vs. Temperature



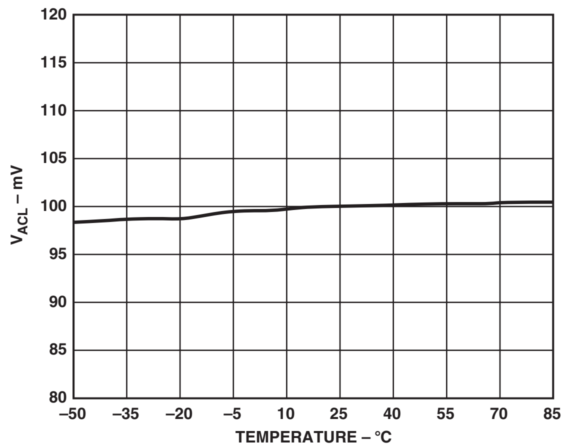

TPC 4. $V_Z$ vs. Temperature



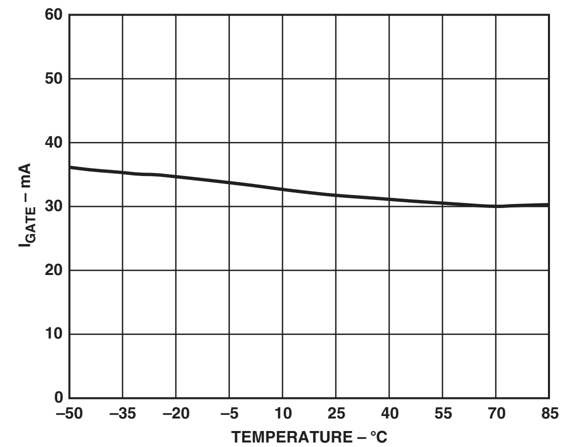

TPC 5. Undervoltage Lockout, $V_{LKO}$ vs. Temperature



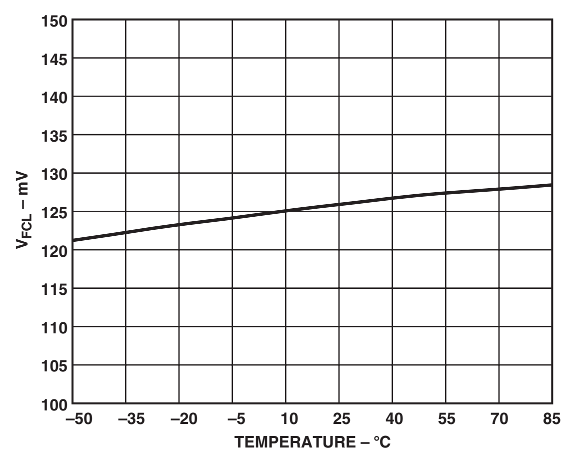

TPC 6. Circuit Breaker Current Limit Voltage, $V_{CB}$ vs. Temperature



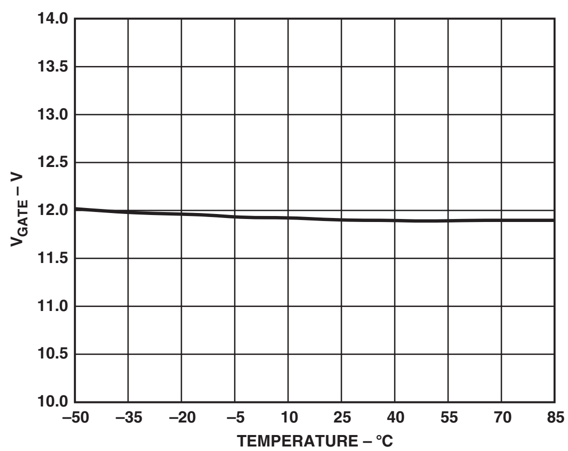

*TPC 7. Analog Current Limit Voltage, $V_{ACL}$ vs. Temperature*



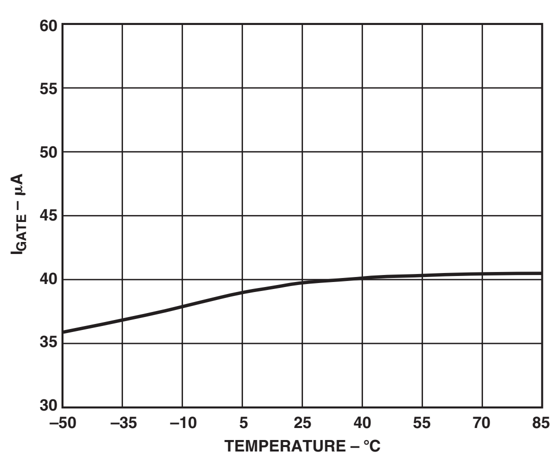

*TPC 10. $I_{GATE}$ (FCL, Sink) vs. Temperature ($V_{GATE}$ = 9 V)*



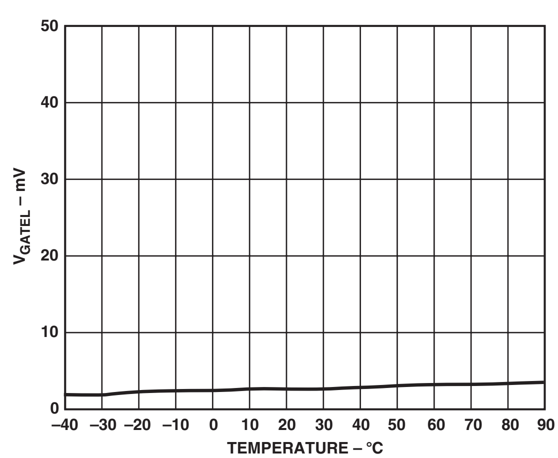

*TPC 8. Fast Current Limit Voltage, $V_{FCL}$ vs. Temperature*



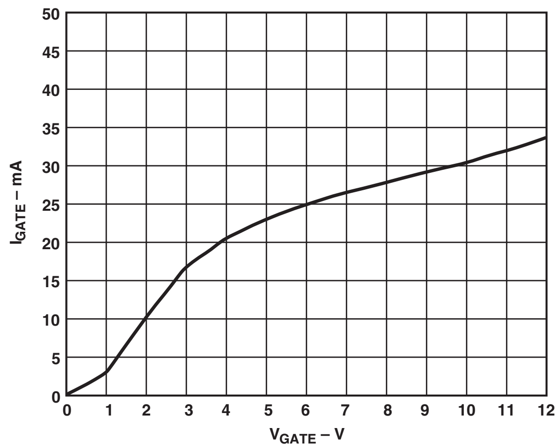

*TPC 11. $V_{GATE}$ vs. Temperature*



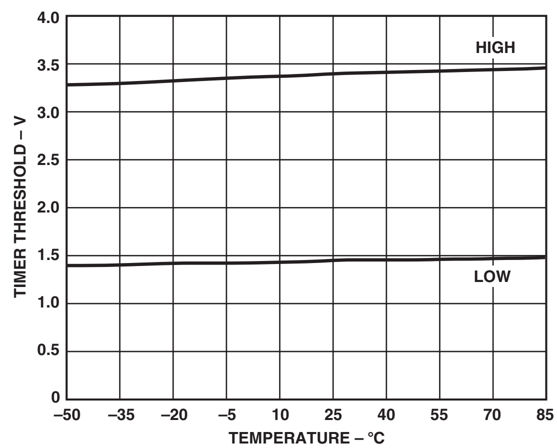

*TPC 9. $I_{GATE}$ (Source) vs. Temperature*



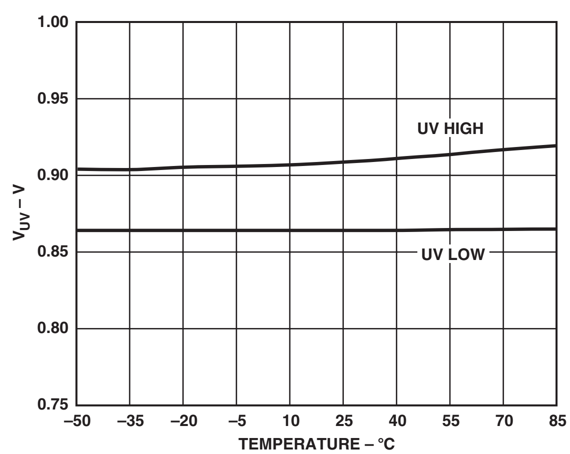

*TPC 12. $V_{GATEL}$ vs. Temperature*



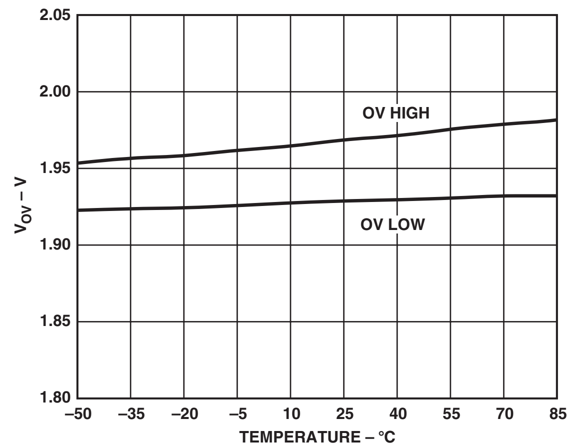

TPC 13. $I_{GATE}$ vs. $V_{GATE}$



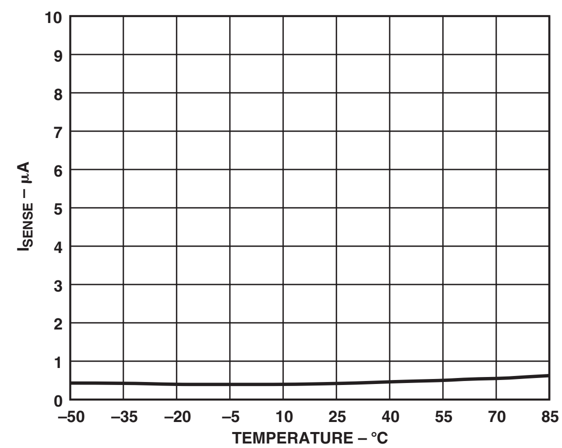

TPC 14. High and Low Timer Thresholds vs. Temperature



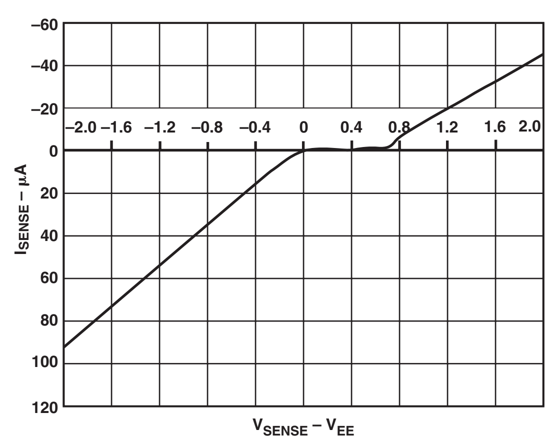

TPC 15. UV Threshold vs. Temperature



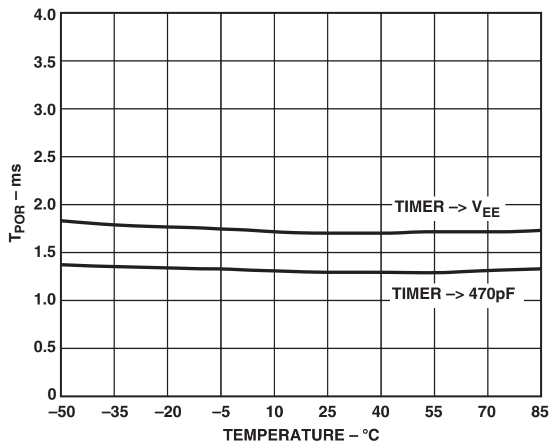

TPC 16. OV Threshold vs. Temperature



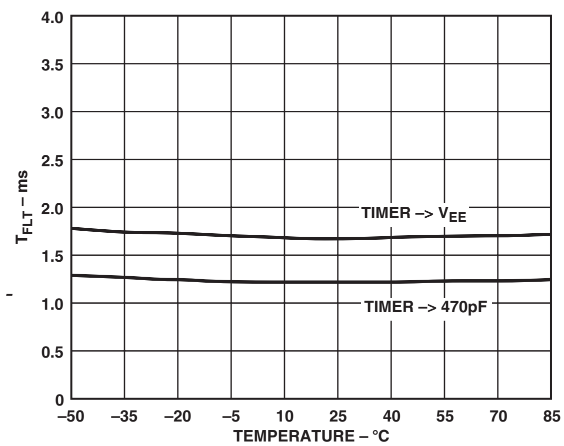

TPC 17. $I_{SENSE}$ vs. Temperature ($V_{SENSE}$ = 50 mV)



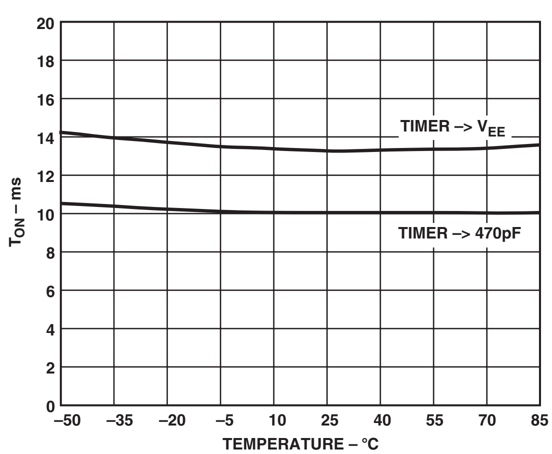

TPC 18. $I_{SENSE}$ vs. ($V_{SENSE} - V_{EE}$)



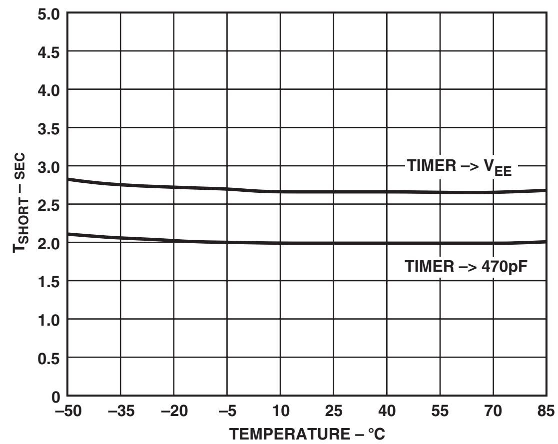

*TPC 19. POR Delay vs. Temperature*



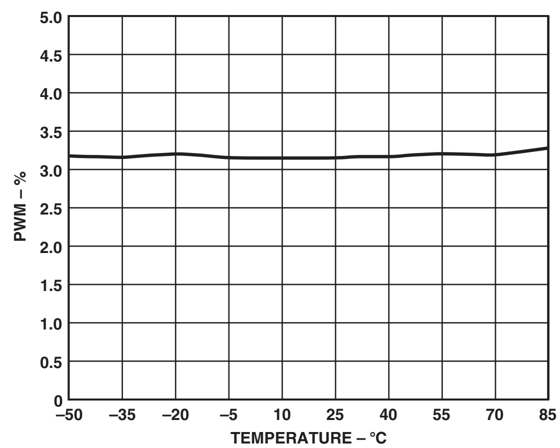

*TPC 20. Voltage Fault Filter Time vs. Temperature*




*TPC 21. Maximum Current Limit On Time vs. Temperature*




*TPC 22. Continuous Short Circuit Time before Shutdown vs. Temperature*




*TPC 23. Current Limit PWM vs. Temperature*

## FUNCTIONAL DESCRIPTION

### HOT CIRCUIT INSERTION

Inserting circuit boards into a live –48 V backplane can cause large transient currents to be drawn as the board capacitance charges up. These transient currents can cause glitches on the system power supply and can permanently damage components on the board.

The ADM1070 is designed to control the manner in which a board's supply voltage is applied so that harmful transient currents do not occur and the board can be safely inserted or removed from a live backplane. Undervoltage, overvoltage, and overcurrent protection are other features of the part. The ADM1070 ensures that the input voltage is stable and within tolerance before being applied to the dc-to-dc converter, which generates the low voltage levels required to power the on-board logic. One such converter is the Artesyn EXQ50. Go to www.artesyn.com for more information.

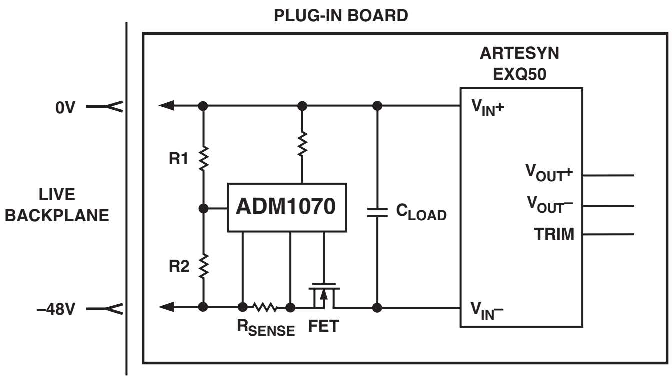



*Figure 1. Topology*

### INITIAL STARTUP

The ADM1070 hot swap controller normally resides on a removable circuit board and controls the manner in which power is applied to the board upon connection. This is achieved using a FET, Q1, in the power path. By controlling the gate voltage of the FET, the surge of current to charge load capacitance can be limited to a safe value when the board makes connection. Note that the ADM1070 can also reside on the backplane itself, and perform the same function from there.

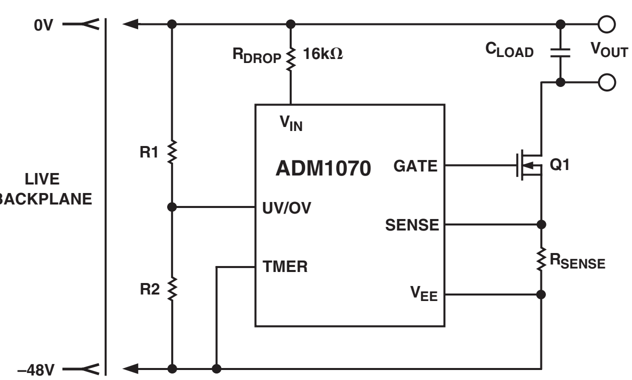



*Figure 2. Circuit Board Connection*

Figure 2 shows how a plug-in module containing the ADM1070 makes connection to the backplane supply. When the board is inserted, the –48 V and 0 V lines connect. This powers up the device with the voltage on $V_{IN}$ exceeding $V_{LKO}$.

When the voltage at the UV/OV Pin exceeds undervoltage rising threshold ($V_{UVR}$) of 0.91 V, it is now inside the operating voltage window. It must stay inside this window for the duration of the power-on reset delay time, $t_{POR}$, which is dependent on the value of $C_T$.

When the device detects that the supply voltage is valid, it ramps up the gate voltage until the FET turns on and the load current increases. The ADM1070 monitors the level of the current flowing through the FET by sensing the voltage across the external sense resistor, $R_{SENSE}$. When the sense voltage reaches 100 mV, the GATE Pin is actively controlled, limiting the load current. In this way, the maximum current permitted to flow through the load is set by the choice of $R_{SENSE}$.

If a change in the level of the supply voltage causes UV/OV to fall below the undervoltage falling threshold of $V_{UVF}$, or rise above the overvoltage rising threshold of $V_{OVR}$, then the gate drive will be disabled.

### BOARD REMOVAL

If the board is removed from a card cage, the voltage at the UV/OV pin falls to zero (i.e., outside operating range) and the gate drive is deasserted, turning off the FET.

### CONTROLLING THE CURRENT

The ADM1070 features a current limiting function that protects against short circuits or excessive supply currents. The flow of current through the load is monitored by measuring the voltage across the sense resistor, which is connected between the SENSE and $V_{EE}$ Pins. There are three different types of protection offered:

1. If the voltage across the sense resistor exceeds the circuit breaker limit voltage of 88 mV (rising) for the current limit on time ($t_{LIMITON}$), then a current fault has occurred and the PWM cycle begins. The FET current is linearly controlled at a maximum of 100 mV/$R_{SENSE}$ (via the gate drive) during $t_{LIMITON}$ (see next section). The gate is then disabled for the duration $t_{OFF}$. This PWM ratio, which will always be 3%, is given by $t_{ON}/t_{OFF}$.

   A unique feature of the ADM1070 is the limited consecutive retry function. An internal fault counter keeps track of the number of successive PWM cycles that occur. The fault counter is incremented after every fault is detected. If the ADM1070 detects seven consecutive current faults, it is apparent that the fault is not a temporary one and the device latches itself off. The fault counter is cleared if a new $t_{ON}$ timeout does not occur within 2 × $t_{OFF}$ of the previous $t_{LIMITON}$ timeout.

2. If a voltage between the SENSE and $V_{EE}$ Pins increases to 100 mV (the analog current limit voltage) during $t_{LIMITON}$, then the ADM1070 takes action to reduce this current to a safer level. The internal analog current limit loop dynamically adjusts the gate drive, keeping the load current at the 100 mV/$R_{SENSE}$ level. The FET now acts as a current source, limiting the load current to the level set by the value of the sense resistor.

   The sense voltage is also above the circuit breaker limit voltage, so the limited consecutive retry function is still operational. If the current fault is not cleared (sense resistor voltage brought below 79 mV) after seven consecutive faults, then the device is latched off.

3. If a serious short circuit occurs on the load side, the –48 V supply can cause massive currents to flow very quickly. Because of this, the gate voltage must be reduced quickly to prevent a catastrophic failure. If the ADM1070 detects a voltage greater than the fast current limit voltage (126 mV) across the sense resistor, it is apparent that a serious short circuit is present and the load current must be reduced as quickly as possible. The fast current limit loop takes over and pulls gate low much faster than in the previous case.

## SENSE RESISTOR

The ADM1070's current limiting function can operate at different current levels. The sense resistor is inserted between the $V_{EE}$ and sense pins, and a current fault occurs whenever the voltage across the sense resistor is greater than 100 mV for longer than the on time, $t_{LIMITON}$. The current limit is determined by selection of the sense resistor, $R_{SENSE}$. Table I shows how the maximum allowable load current ($I_{LOAD(MAX)}$) and the minimum and maximum in-rush currents ($I_{LIMIT(MIN)}$) and $I_{LIMIT(MAX)}$) are related to the value of $R_{SENSE}$.

**Table I. $I_{LOAD(MAX)}$, $I_{LIMIT(MIN)}$, and $I_{LIMIT(MAX)}$ for Different Values of $R_{SENSE}$**

| $R_{SENSE}$ (mΩ) | $I_{LOAD(MAX)}$ (A) | $I_{LIMIT(MIN)}$ (A) | $I_{LIMIT(MAX)}$ (A) |
|---|---|---|---|
| 5 | 12.0 | 18.0 | 22.0 |
| 10 | 6.0 | 9.0 | 11.0 |
| 15 | 4.0 | 6.0 | 7.3 |
| 18 | 3.3 | 5.0 | 6.1 |
| 22 | 2.7 | 4.1 | 5.0 |
| 33 | 1.8 | 2.7 | 3.3 |
| 47 | 1.3 | 1.9 | 2.3 |
| 51 | 1.2 | 1.7 | 2.2 |
| 68 | 0.9 | 1.3 | 1.6 |
| 75 | 0.8 | 1.2 | 1.5 |
| 90 | 0.7 | 1.0 | 1.2 |

## SHUNT REGULATOR

A shunt regulator shunts the ADM1070 $V_{IN}$ Pin. Power is derived from the –48 V supply through the combination of an internal Zener diode and an external shunt resistor, $R_{DROP}$. Table II shows the operational voltage range and power dissipation for different values of $R_{DROP}$. Note that 16 kΩ is the default value for $R_{DROP}$.

**Table II. Minimum and Maximum Allowable Operating Voltages for Different Values of $R_{DROP}$**

| $R_{DROP}$ | Min Allowable $V_{DD}$ Voltage (V) | Max Allowable $V_{DD}$ Voltage (V) | $P_{DROP}$ @ 48 V (W) |
|---|---|---|---|
| 10 kΩ (0.25 W) | 26 | 61 | 0.13 |
| 12 kΩ | 28.6 | 65.8 | 0.11 |
| 14 kΩ | 31.2 | 70.2 | 0.09 |
| 16 kΩ | 33.8 | 74.2 | 0.08 |
| 18 kΩ | 36.4 | 78.1 | 0.07 |
| 20 kΩ | 39 | 81.7 | 0.065 |
| 22 kΩ | 41.6 | 85.2 | 0.06 |
| 10 kΩ (0.5 W) | 26 | 81.7 | 0.13 |
| 12 kΩ | 28.6 | 88.5 | 0.11 |
| 14 kΩ | 31.2 | 94.7 | 0.09 |
| 16 kΩ | 33.8 | 100.4 | 0.08 |
| 18 kΩ | 36.4 | 105.9 | 0.07 |
| 20 kΩ | 39 | 111 | 0.065 |
| 22 kΩ | 41.6 | 115.9 | 0.06 |

## INTERNAL UNDERVOLTAGE LOCKOUT

The $V_{IN}$ Pin is monitored for undervoltage lockout. When the voltage at $V_{IN}$ is above 8.5 V ($V_{LKO}$), the device is enabled. If this voltage drops below 8.5 V, the device is disabled and gate is pulled low. Note that this is unrelated to the undervoltage and overvoltage functions performed at the UV/OV Pin.

## TIMER

The TIMER Pin on the ADM1070 gives the user control over the timing functions on the part. By connecting an external capacitor between the TIMER Pin and $V_{EE}$, the user can set the UV/OV glitch filter time, $t_{FLT}$, the power-on reset delay time, $t_{POR}$, the maximum current on time, $t_{ON}$, the current limit time out, $t_{OFF}$, and the continuous short circuit time before latched shutdown, $t_{SHORT}$ (see Table III). Note that all times are scaled relative to each other and cannot be altered individually (without changing the other times). The default values for these times are selected by tying the TIMER Pin directly to $V_{EE}$.

**Table III. Timer Capacitor Values and Timing Values**

| $C_{TIMER}$ (pF) | $t_{FLT}$ (ms) | $t_{POR}$ (ms) | $t_{LIMITON}$ (ms) | $t_{PWMOFF}$ (ms) | $t_{SHORT}$ (ms) |
|---|---|---|---|---|---|
| 220 | 0.58 | 0.58 | 4.8 | 150 | 1000 |
| 330 | 0.85 | 0.85 | 7.1 | 230 | 1400 |
| 470 | 1.21 | 1.21 | 9.9 | 320 | 2000 |
| Tied to $V_{EE}$ | 1.55 | 1.55 | 12.8 | 410 | 2600 |
| 680 | 1.74 | 1.74 | 14.2 | 450 | 2800 |
| 1000 | 2.54 | 2.54 | 20.8 | 660 | 4100 |
| 2200 | 5.64 | 5.64 | 46.2 | 1465 | 9113 |

**UNDERVOLTAGE/OVERVOLTAGE DETECTION**

The ADM1070 incorporates single-pin overvoltage and undervoltage detection with a programmable operating voltage window. When the voltage on the UV/OV pin rises above the OV rising threshold or falls below the UV falling threshold, a fault signal is generated that disables the linear current regulator and results in the GATE Pin being pulled low. The voltage fault signal is time filtered so that faults of duration less than the UV/OV glitch filter time, $t_{FLT}$, do not force the gate drive low ($t_{FLT}$ is set by the choice of external capacitor $C_T$, see Table III). The filter operates only on the "faulting" edge (i.e., on a high to low transition on the undervoltage monitor and on a low to high transition on the overvoltage monitor). The analog comparators have some hysteresis to provide smooth switching of the comparator inputs.

If the voltage on UV/OV goes out of range (i.e., below 0.86 V or above 1.97 V) gate is pulled low. If the UV/OV voltage subsequently re-enters the operating voltage window, the ADM1070 will restore the gate drive.

The overvoltage and undervoltage thresholds are:

UV turning on = 0.91 V

UV turning off = 0.86 V

OV turning on = 1.97 V

OV turning off = 1.93 V

The undervoltage/overvoltage levels are determined by selection of the resistor ratio R1/R2, (see Table I). These two resistors form a resistor divider that generates the voltage; at the UV/OV Pin, which is proportional to the supply voltage. By choosing this ratio carefully, the ADM1070 can be programmed to apply the supply voltage to the load only when it is within specific thresholds. For example, for R1 = 39 kΩ and R2 = 1 kΩ the typical operating range is 36.4 V to 76.8 V. The undervoltage and overvoltage shutdown thresholds are 34.4 V and 77.2 V for this resistor ratio. 1% resistors should be used to maintain the accuracy of these threshold levels.

Voltage Divider:

$V_{UV/OV} = V_{SS}(R2/(R1 + R2))$

For R2 = 1 kΩ:

$V_{SS} = V_{UV/OV}(R1 + 1)$

And for R1 = 39 kΩ:

$V_{SS} = 40\ V_{UV/OV}$

Operating Range:

UV => 40(0.91) = 36.4 V

OV => 40(1.93) = 77.2 V

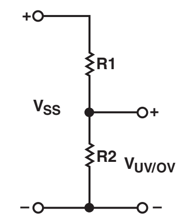



*Figure 3. Voltage Divider*

UV/OV Shutdown Levels:

UV => 40(0.86) = 34.4 V

OV => 40(1.97) = 78.8 V

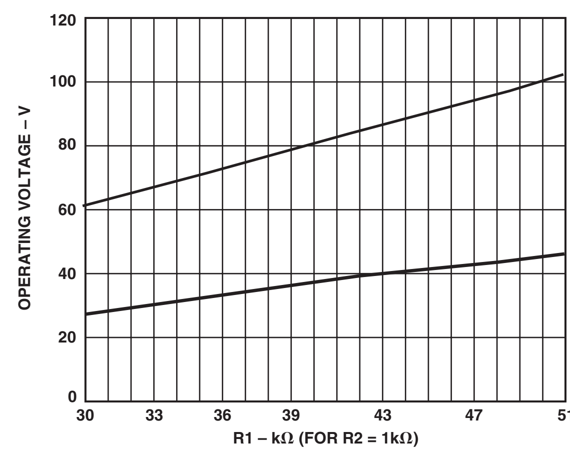



*Figure 4. Operating Voltage Window vs. Resistance Ratio*

**Table IV. Resistance Ratios and Operating Voltage Windows**

| Resistor Ratio | Undervoltage | | Overvoltage | |
|---|---|---|---|---|
| **R1 (for R2 = 1 kΩ)** | **$V_{UV}$ (Falling)** | **$V_{UV}$ (Rising)** | **$V_{OV}$ (Falling)** | **$V_{OV}$ (Rising)** |
| **kΩ** | **V** | **V** | **V** | **V** |
| 30 | 26.7 | 28.2 | 59.8 | 61.0 |
| 33 | 29.2 | 31.0 | 65.6 | 67.0 |
| 36 | 31.8 | 33.7 | 71.4 | 72.9 |
| 39 | 34.4 | 36.4 | 77.2 | 78.8 |
| 43 | 37.8 | 40.0 | 84.9 | 86.7 |
| 47 | 41.3 | 43.7 | 92.6 | 94.6 |
| 51 | 44.7 | 46.4 | 100.4 | 102.4 |

## FUNCTIONALITY AND TIMING

**Live Insertion**

The timing waveforms associated with the live insertion of a plug-in board using the ADM1070 are shown in the following figures. When the board connects the GND-$V_{EE}$ potential climbs to 48 V. As this voltage is applied, the voltage at the $V_{IN}$ Pin ramps above the undervoltage lockout ($V_{LKO}$) of 8.5 V to a constant 12.3 V and is held at this level with the shunt resistor and external resistor combination at the $V_{IN}$ Pin.

When UV/OV crosses the undervoltage rising threshold of 0.91 V, it is now inside the operating voltage window and the –48 V supply must be applied to the load. After a time delay, $t_{POR}$, the ADM1070 begins to ramp up the gate drive. When the voltage on the SENSE Pin reaches 100 mV (the analog current limit) the gate drive is held constant. When the board capacitance is fully charged, the sense voltage begins to drop below the analog current limit voltage and the gate voltage is free to ramp up further. The gate voltage eventually reaches its maximum value of 12.3 V (as set by $V_{IN}$).

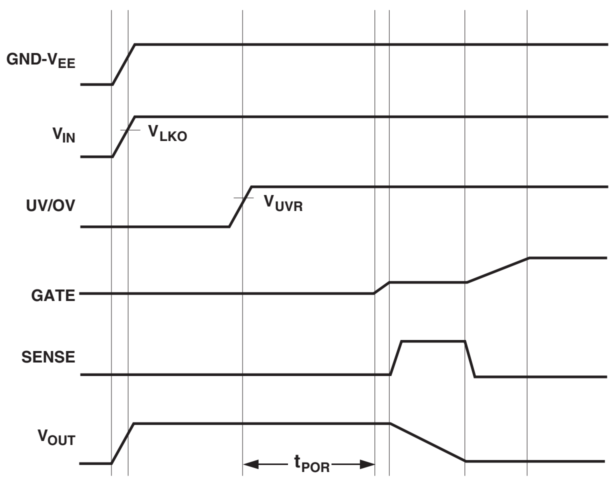



*Figure 5. Timing Waveforms Associated with a Live Insertion Event*

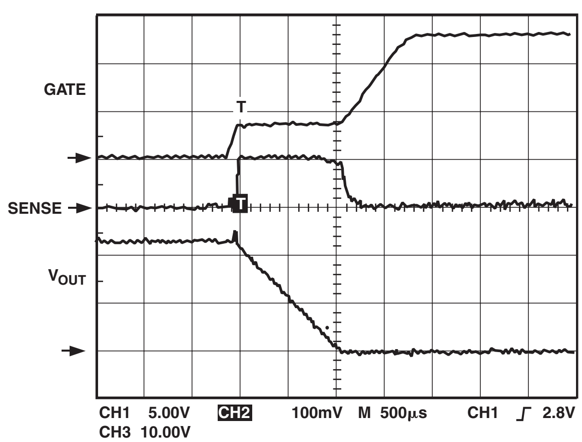



*Figure 6. Start-Up Sequence*

## OVERVOLTAGE AND UNDERVOLTAGE

The waveforms for an overvoltage glitch are shown below. When UV/OV glitches above the overvoltage rising threshold of 1.97 V, an overvoltage condition is detected and the gate voltage is pulled low. UV/OV begins to drop a back toward the operating voltage window and the gate drive is restored when the overvoltage falling threshold of 1.93 V is reached. Figure 7 illustrates the ADM1070's operation in an overvoltage situation.

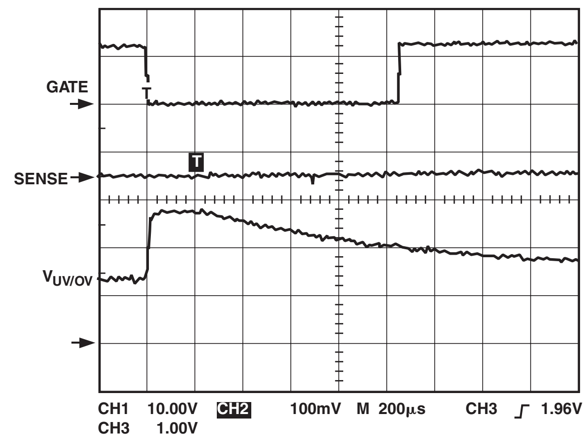



*Figure 7. Timing Waveforms Associated with an Overvoltage Glitch*

An undervoltage glitch is dealt with in a similar way. When $V_{UV/OV}$ falls below the undervoltage falling threshold of 0.86 V, the gate voltage is pulled low. If UO/UV subsequently rises back above the undervoltage rising threshold of 0.91 V, then the gate voltage is restored. Figure 8 illustrates the ADM1070's operation in an undervoltage situation.

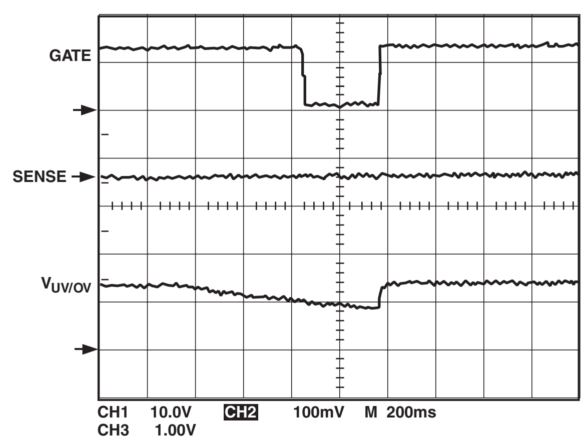



*Figure 8. Timing Waveforms Associated with an Undervoltage Glitch*

## CURRENT FAULT PLOTS

Some timing waveforms associated with current over faults are shown in the following figures. Figure 9 shows how a current glitch (of approximately 500 µs) is dealt with when the output is shorted after power-up. The gate voltage is at a constant 12.3 V before the glitch occurs. When the short circuit occurs, the sense voltage rises sharply as the load current ramps up quickly. When the sense voltage reaches 100 mV ($V_{ACL}$), the ADM1070 reduces the gate voltage to stop the load current from increasing any further. When $V_{SENSE}$ drops back below $V_{ACL}$, the gate voltage is increased again.

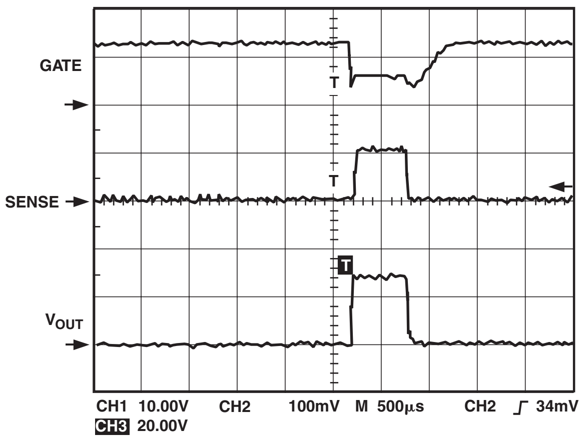



*Figure 9. Timing Waveforms Associated with a Current Glitch*

The plots shown illustrate the operation of the ADM1070's unique limited consecutive retry function. Figure 10 highlights what happens when a current fault occurs for more than 14 ms (default $t_{LIMITON}$ when TIMER Pin tied to $V_{EE}$) and a current fault is registered. In this case, gate is previously low and the part is being powered up into a current fault situation (shorted load). When power is applied, gate is allowed to ramp until sense reaches 100 mV. gate is then held constant to keep sense at this level. After $t_{ON}$, the PWM cycle begins and gate is reduced to zero.

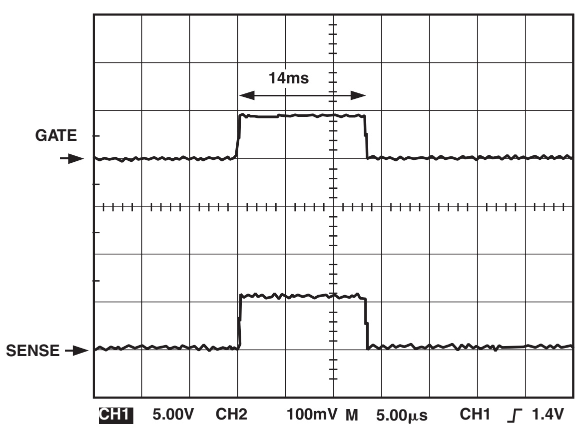



*Figure 10. Timing Waveforms Associated with a Current Fault*

Figure 11 shows a current fault on a wider timebase. The first spike on the sense line represents the first current fault. The sense voltage is allowed to ramp up to 100 mV before the gate voltage is reduced to compensate. The gate and sense voltages remain at these levels until the $t_{ON}$ time has expired. A current fault is then registered and the gate voltage, and therefore the sense voltage, are then both held low for the time period $t_{OFF}$. Note that the PWM ratio ($t_{ON}/t_{OFF}$) is equal to 3%. The cycle then restarts and the sense voltage is free to ramp up to 100 mV again (it will if the fault is still present). This cycle repeats itself a total of seven times. Figure 12 shows the seven consecutive faults occurring on an even wider timebase. If the ADM1070 detects seven consecutive current faults, the part then latches off (after a total time $t_{SHORT}$).

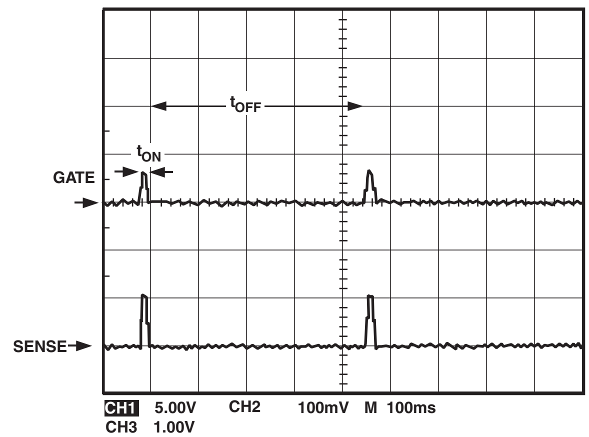



*Figure 11. Illustration of the PWM Ratio ($t_{ON}/t_{OFF}$)*

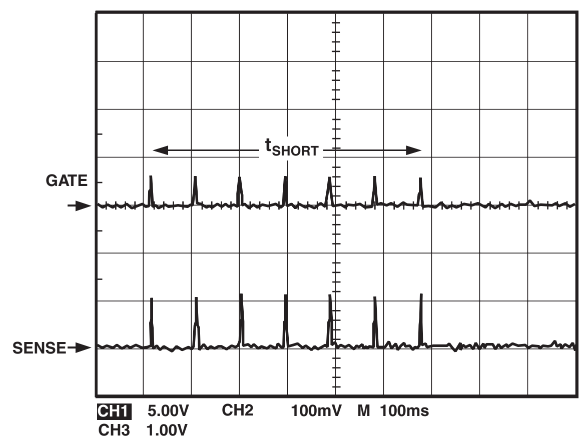



*Figure 12. Illustration of the Limited Consecutive Retry Function (Seven Retries and Latch Off)*

Figure 13 shows the behavior of ADM1070 when a temporary current fault occurs followed by a permanent current fault. When the first overcurrent fault occurs, the first 100 mV spike on the sense line can be seen. During the $t_{OFF}$ time, this current fault corrects itself. After this time period, a no fault condition is detected and the limited consecutive counter is reset. GATE is reasserted. When the overcurrent fault returns permanently, the limited consecutive retry counter detects seven consecutive faults and the part latches off.

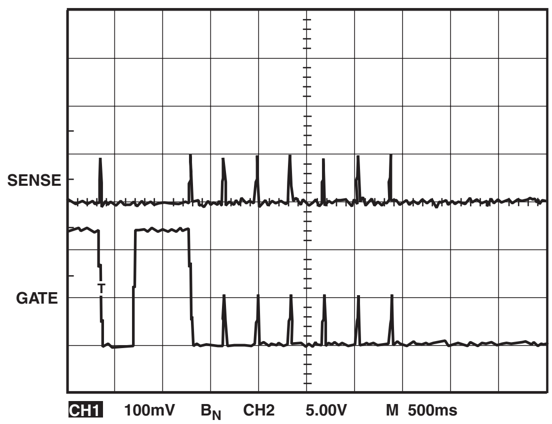



*Figure 13. Illustration of the PWM Ratio ($t_{ON}/t_{OFF}$)*

In this way, the ADM1070 prevents nuisance shutdowns from transient shorts of up to three seconds (typically), but will provide latched shut-down protection from permanently shorted loads.

**KELVIN SENSE RESISTOR CONNECTION**

When using a low value sense resistor for high current measurement, the problem of parasitic series resistance can arise. The lead resistance can be a substantial fraction of the rated resistance, making the total resistance a function of lead length. This problem can be avoided by using a Kelvin sense connection. This type of connection separates the current path through the resistor and the voltage drop across the resistor. Figure 14 shows the correct way to connect the sense resistor between the SENSE and $V_{EE}$ Pins of the ADM1070.

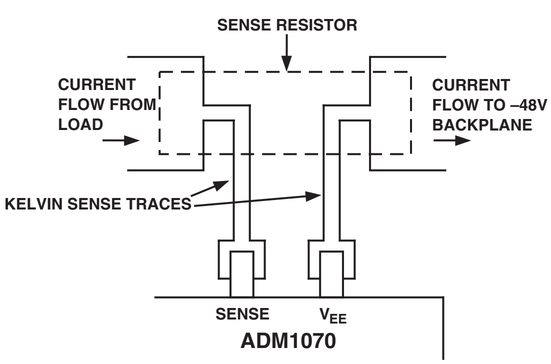



*Figure 14. Kelvin Sensing with the ADM1070*

**UV/OV AS ENABLE PIN**

Connecting an open collector output to the UV/OV Pin means that a TTL signal can be used to disable the part. In Figure 15, the open collector output connects to $\overline{EN}$. Driving the base of the open collector device high enough to cause the UV/OV Pin to be pulled below the undervoltage falling threshold of 0.86 V typical will cause the pass transistor Q1 to be turned off.

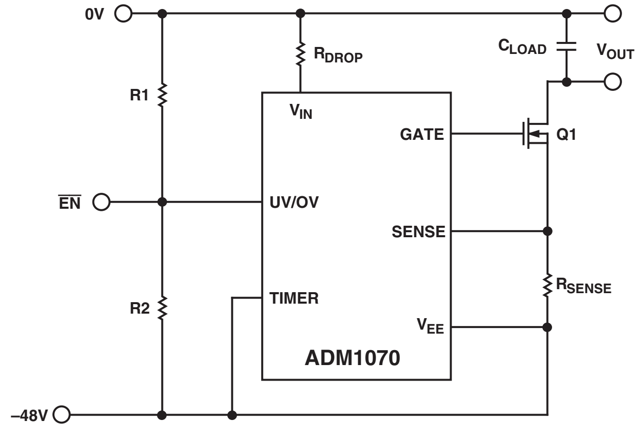
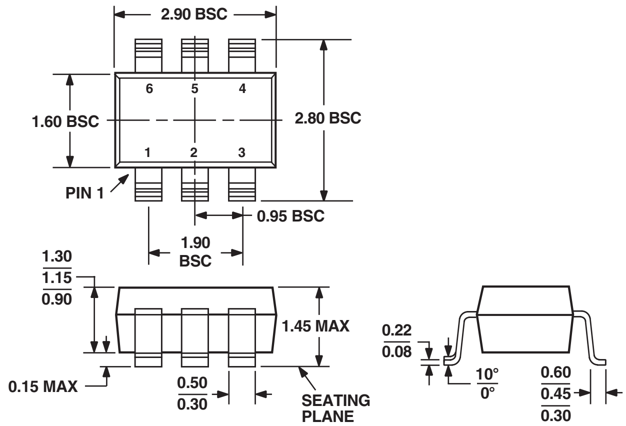



*Figure 15. UV/OV Used as Enable Input*

## OUTLINE DIMENSIONS

### 6-Lead Plastic Surface-Mount Package [SOT-23] (RT-6)

Dimensions shown in millimeters

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