Triple Differential Receiver with Adjustable Line Equalization

Data Sheet **AD8123**

FEATURES

- **Compensates cables to 300 meters for wideband video**
- **Fast rise and fall times**
  - **4.9 ns with 2 V step at 150 meters of UTP cable**
  - **8.0 ns with 2 V step at 300 meters of UTP cable**
- **55 dB peak gain at 100 MHz**
- **Two frequency response gain adjustment pins**
  - **High frequency peaking adjustment (V_{PEAK})**
  - **Broadband flat gain adjustment (V_{GAIN})**
- **Pole location adjustment pin (V_{POLE})**
  - **Compensates for variations between cables**
  - **Can be optimized for either UTP or coaxial cable**
- **DC output offset adjust (V_{OFFSET})**
- **Low output offset voltage: 24 mV**
- **Compensates both RGB and YPbPr**
- **Two on-chip comparators with hysteresis**
  - **Can be used for common-mode sync extraction**
- **Available in 40-lead, 6 mm × 6 mm LFCSP**

APPLICATIONS

- **Keyboard-video-mouse (KVM)**
- **Digital signage**
- **RGB video over UTP cables**
- **Professional video projection and distribution**
- **HD video**
- **Security video**

FUNCTIONAL BLOCK DIAGRAM

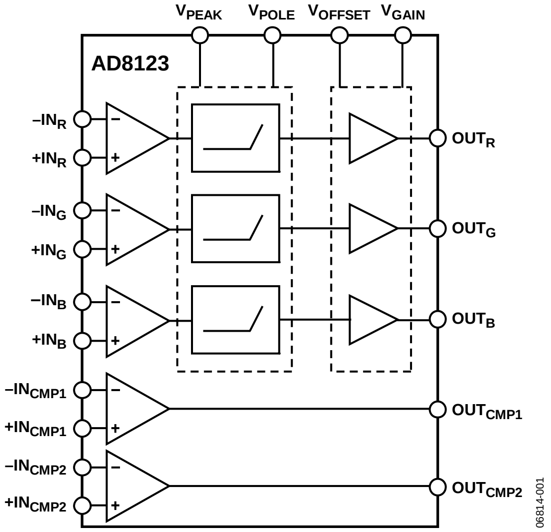


Figure 1.

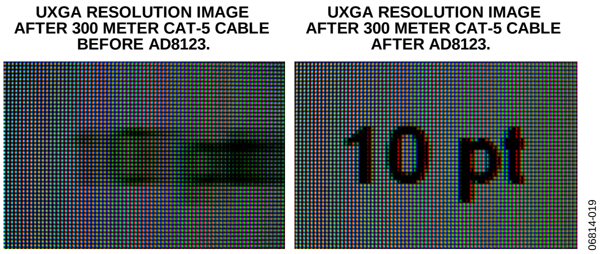
GENERAL DESCRIPTION

The AD8123 is a triple, high speed, differential receiver and equalizer that compensates for the transmission losses of UTP and coaxial cables up to 300 meters in length. Various gain stages are summed together to best approximate the inverse frequency response of the cable. Logic circuitry inside the AD8123 controls the gain functions of the individual stages so that the lowest noise can be achieved at short-to-medium cable lengths. This technique optimizes its performance for low noise, short-to-medium range applications, while at the same time provides the high gain bandwidth required for long cable equalization (up to 300 meters). Each channel features a high impedance differential input that is ideal for interfacing directly with the cable.

The AD8123 has three control pins for optimal cable compensation, as well as an output offset adjust pin. Two voltage-controlled pins are used to compensate for different cable lengths; the V_{PEAK} pin controls the amount of high frequency peaking and the V_{GAIN} pin adjusts the broadband flat gain, which compensates for the low frequency flat cable loss.

For added flexibility, an optional pole adjustment pin, V_{POLE}, allows movement of the pole locations, allowing for the compensation of different gauges and types of cable as well as variations between different cables and/or equalizers. The V_{OFFSET} pin allows the dc voltage at the output to be adjusted, adding flexibility for dc-coupled systems.

The AD8123 is available in a 6 mm × 6 mm, 40-lead LFCSP and is rated to operate over the extended temperature range of −40°C to +85°C.


UXGA RESOLUTION IMAGE AFTER 300 METER CAT-5 CABLE BEFORE AD8123.

UXGA RESOLUTION IMAGE AFTER 300 METER CAT-5 CABLE AFTER AD8123.

Figure 2. UXGA Resolution Images Before and After the AD8123

Rev. B **Document Feedback**

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REVISION HISTORY

1/16— Rev. A to Rev. B

Added Figure 2 Caption ... 1
Changes to Figure 4 and Table 4 ... 6
Updated Outline Dimensions ... 16
Changes to Ordering Guide ... 16

11/07—Rev. 0 to Rev. A

Changes to Features ... 1
Changes to Ordering Guide ... 16

8/07—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_S = ±5 V, R_L = 150 Ω, Belden Cable (BL-7987R), V_{OFFSET} = 0 V, V_{PEAK}, V_{GAIN}, and V_{POLE} are set to recommended settings shown in Figure 17, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
PEAKING PERFORMANCE (NO CABLE)					
Peak Frequency	V_{PEAK} = 2 V, V_{GAIN} = 0.6 V, V_{POLE} = 1 V		100		MHz
	V_{PEAK} = 2 V, V_{GAIN} = 0.6 V, V_{POLE} = 2 V		105		MHz
Peak Gain	V_{PEAK} = 2 V, V_{GAIN} = 0.6 V, V_{POLE} = 1 V		45		dB
	V_{PEAK} = 2 V, V_{GAIN} = 0.6 V, V_{POLE} = 2 V		55		dB
DYNAMIC PERFORMANCE					
10% to 90% Rise/Fall Time	V_{OUT} = 2 V step, 150 meters Cat-5		4.9		ns
	V_{OUT} = 2 V step, 300 meters Cat-5		8.0		ns
Settling Time to 2%	V_{OUT} = 2 V step, 150 meters Cat-5		36		ns
	V_{OUT} = 2 V step, 300 meters Cat-5		106		ns
−3 dB Large Signal Bandwidth	V_{OUT} = 1 V p-p, <10 meters Cat-5		120		MHz
	V_{OUT} = 2 V p-p, <10 meters Cat-5		110		MHz
	V_{OUT} = 2 V p-p, 150 meters Cat-5		78		MHz
	V_{OUT} = 2 V p-p, 300 meters Cat-5		43		MHz
Integrated Output Voltage Noise	150 meter setting, integrated to 160 MHz		2.5		mV rms
	300 meter setting, integrated to 160 MHz		24		mV rms
INPUT DC PERFORMANCE					
Input Voltage Range	−IN and +IN		±3.0		V
Maximum Differential Voltage Swing			4		V p-p
Voltage Gain	$\Delta V_O/\Delta V_I$, V_{GAIN} set for 0 meters of cable		1		V/V
Common-Mode Rejection Ratio (CMRR)	At dc, V_{PEAK} = V_{GAIN} = V_{POLE} = 0 V		−86		dB
	At dc, V_{PEAK} = V_{GAIN} = V_{POLE} = 2 V		−67		dB
	At 1 MHz, V_{PEAK} = V_{GAIN} = V_{POLE} = 2 V		−52		dB
Input Resistance	Common mode		4.4		MΩ
	Differential		3.7		MΩ
Input Capacitance	Common mode		1.0		pF
	Differential		0.5		pF
Input Bias Current			2.4		µA
V_{OFFSET} Pin Current			28.9		µA
V_{GAIN} Pin Current			0.5		µA
V_{PEAK} Pin Current			0.4		µA
V_{POLE} Pin Current			0.4		µA
ADJUSTMENT PINS					
V_{PEAK} Input Voltage Range	Relative to GND		0 to 2		V
V_{POLE} Input Voltage Range	Relative to GND		0 to 2		V
V_{GAIN} Input Voltage Range	Relative to GND		0 to 2		V
V_{OFFSET} to OUT Gain	OUT/V_{OFFSET}, range limited by output swing		1		V/V
Maximum Flat Gain	V_{GAIN} = 2 V		2		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	150 Ω load		−3.75 to +3.69		V
	1 kΩ load		−3.66 to +3.69		V
Output Offset Voltage	Referred to output, V_{PEAK} = V_{GAIN} = V_{POLE} = 0 V		24		mV
	Referred to output, V_{PEAK} = V_{GAIN} = V_{POLE} = 2 V		32		mV
Output Offset Voltage Drift	Referred to output		33		µV/°C

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Voltage Range		±4.5		±5.5	V
Positive Quiescent Supply Current			132		mA
Negative Quiescent Supply Current			126		mA
Supply Current Drift, I_{CC}/I_{EE}			80		μA/°C
Positive Power Supply Rejection Ratio	DC, referred to output		−51		dB
Negative Power Supply Rejection Ratio	DC, referred to output		−63		dB
Power Down, V_{IH} (Minimum)	Minimum Logic 1 voltage		1.1		V
Power Down, V_{IL} (Maximum)	Maximum Logic 0 voltage		0.8		V
Positive Supply Current, Powered Down	$V_{PEAK} = V_{GAIN} = V_{POLE} = 0$ V		1.1		μA
Negative Supply Current, Powered Down	$V_{PEAK} = V_{GAIN} = V_{POLE} = 0$ V		0.7		μA
COMPARATORS					
Output Voltage Levels	V_{OH}/V_{OL}		3.33/0.043		V
Hysteresis	V_{HYST}		70		mV
Propagation Delay	$t_{PD, LH}/t_{PD, HL}$		17.5/10.0		ns
Rise/Fall Times	t_{RISE}/t_{FALL}		9.3/9.3		ns
Output Resistance			0.03		Ω
OPERATING TEMPERATURE RANGE		−40		+85	°C

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	11 V
Power Dissipation	See Figure 3
Input Voltage (Any Input)	V_{S-} − 0.3 V to V_{S+} + 0.3 V
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for the device soldered in a circuit board in still air.

Table 3. Thermal Resistance with the Underside Pad Connected to the Plane

Package Type/PCB Type	θ_{JA}	Unit
40-Lead LFCSP/4-Layer	29	°C/W

Maximum Power Dissipation

The maximum safe power dissipation in the AD8123 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8123. Exceeding a junction temperature of 175°C for an extended time can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The power dissipation due to each load current is calculated by multiplying the load current by the voltage difference between the associated power supply and the output voltage. The total power dissipation due to load currents is then obtained by taking the sum of the individual power dissipations. RMS output voltages must be used when dealing with ac signals.

Airflow reduces θ_{JA}. In addition, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA}. The exposed paddle on the underside of the package must be soldered to a pad on the PCB surface that is thermally connected to a solid plane (usually the ground plane) to achieve the specified θ_{JA}.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 40-lead LFCSP (29°C/W) on a JEDEC standard 4-layer board with the underside paddle soldered to a pad that is thermally connected to a PCB plane. θ_{JA} values are approximations.

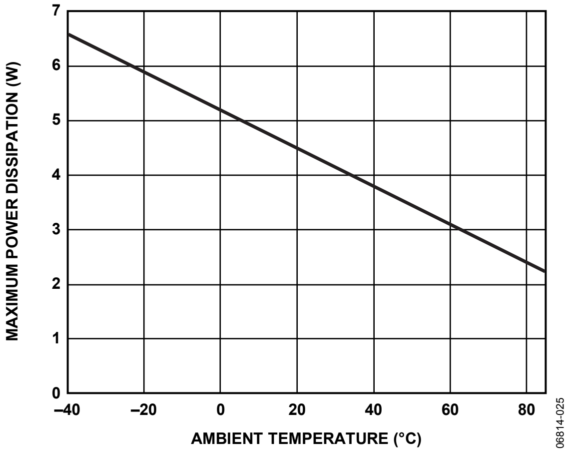
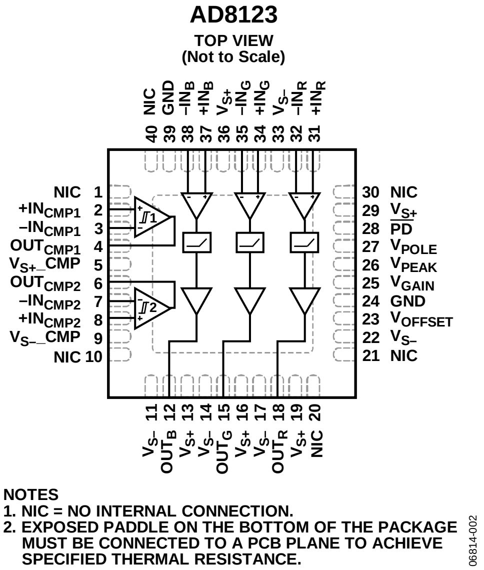


Figure 3. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NIC = NO INTERNAL CONNECTION.
2. EXPOSED PADDLE ON THE BOTTOM OF THE PACKAGE MUST BE CONNECTED TO A PCB PLANE TO ACHIEVE SPECIFIED THERMAL RESISTANCE.

Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 10, 20, 21, 30, 40	NIC	No Internal Connection.
2	+IN$_{CMP1}$	Positive Input, Comparator 1.
3	−IN$_{CMP1}$	Negative Input, Comparator 1.
4	OUT$_{CMP1}$	Output, Comparator 1.
5	V$_{S+}$_CMP	Positive Power Supply, Comparator. Must be connected to V$_{S+}$.
6	OUT$_{CMP2}$	Output, Comparator 2.
7	−IN$_{CMP2}$	Negative Input, Comparator 2.
8	+IN$_{CMP2}$	Positive Input, Comparator 2.
9	V$_{S−}$_CMP	Negative Power Supply, Comparator. Must be connected to V$_{S−}$.
11, 14, 17, 22, 33	V$_{S−}$	Negative Power Supply, Equalizer Sections.
12	OUT$_B$	Output, Blue Channel.
13, 16, 19, 29, 36	V$_{S+}$	Positive Power Supply, Equalizer Sections.
15	OUT$_G$	Output, Green Channel.
18	OUT$_R$	Output, Red Channel.
23	V$_{OFFSET}$	Output Offset Control Voltage.
24, 39	GND	Signal Ground Reference.
25	V$_{GAIN}$	Broadband Flat Gain Control Voltage.
26	V$_{PEAK}$	Equalizer High Frequency Boost Control Voltage.
27	V$_{POLE}$	Equalizer Pole Location Adjustment Control Voltage.
28	$\overline{PD}$	Power Down.
31	+IN$_R$	Positive Input, Red Channel.
32	−IN$_R$	Negative Input, Red Channel.
34	+IN$_G$	Positive Input, Green Channel.
35	−IN$_G$	Negative Input, Green Channel.
37	+IN$_B$	Positive Input, Blue Channel.
38	−IN$_B$	Negative Input, Blue Channel.
	EPAD	Exposed Paddle. Exposed paddle on the bottom of the package must be connected to a PCB plane to achieve specified thermal resistance.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±5 V, R_L = 150 Ω, Belden Cable (BL-7987R), V_{OFFSET} = 0 V, V_{PEAK}, V_{GAIN}, and V_{POLE} are set to recommended settings shown in Figure 17, unless otherwise noted.

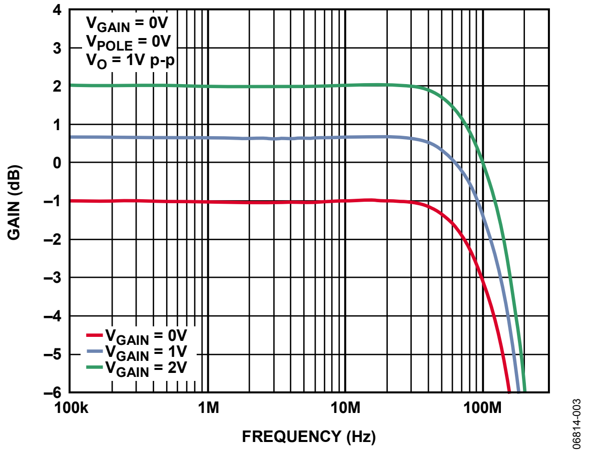


Figure 5. Frequency Response for Various V_{GAIN} Without Cable

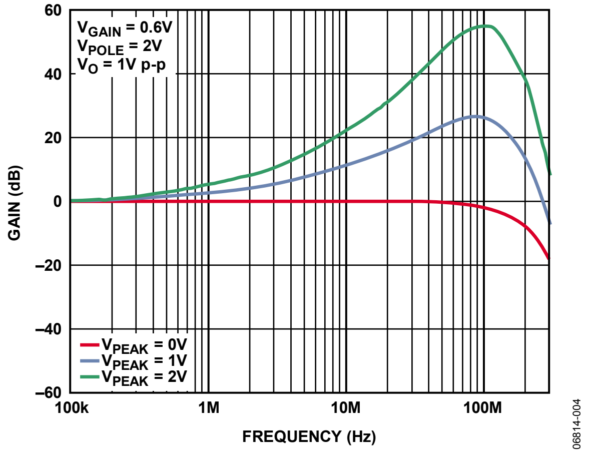


Figure 6. Frequency Response for Various V_{PEAK} Without Cable

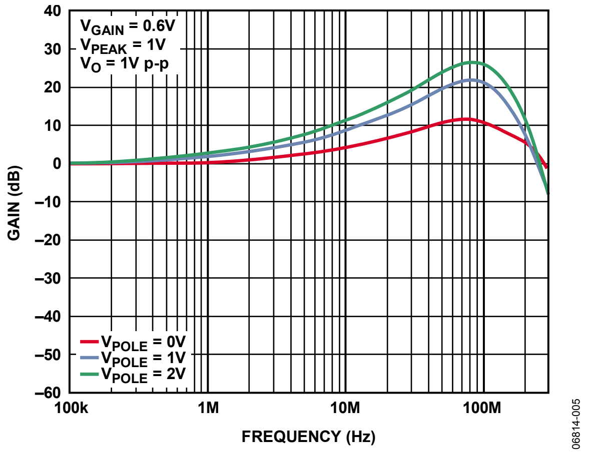


Figure 7. Frequency Response for Various V_{POLE} Without Cable

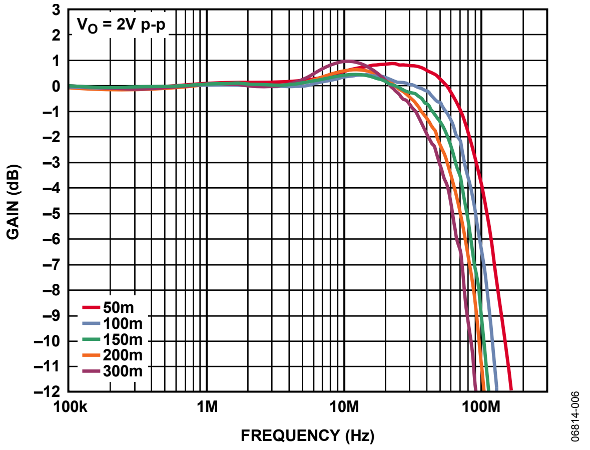


Figure 8. Equalized Frequency Response for Various Cable Lengths

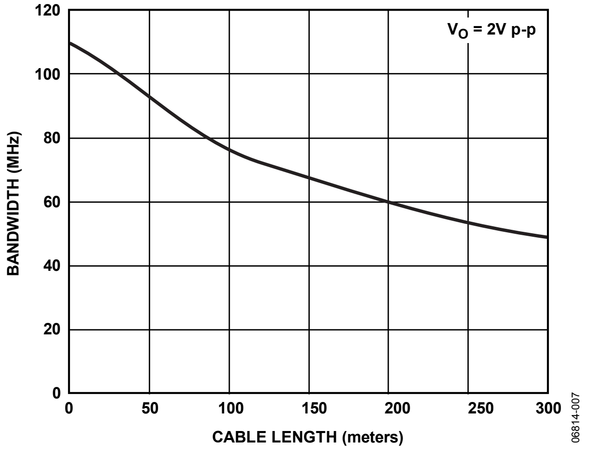


Figure 9. Equalized –3 dB Bandwidth vs. Cable Length

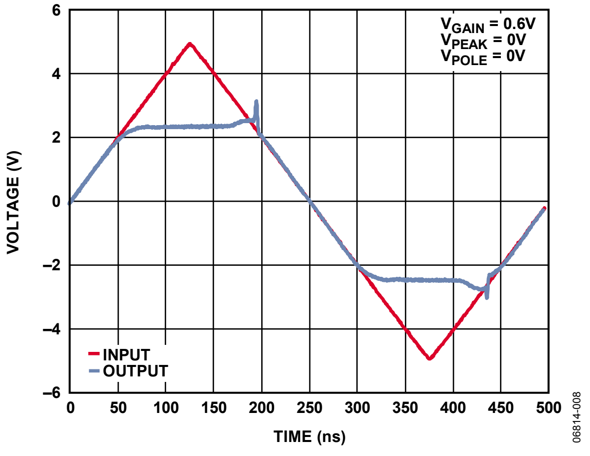


Figure 10. Overdrive Recovery

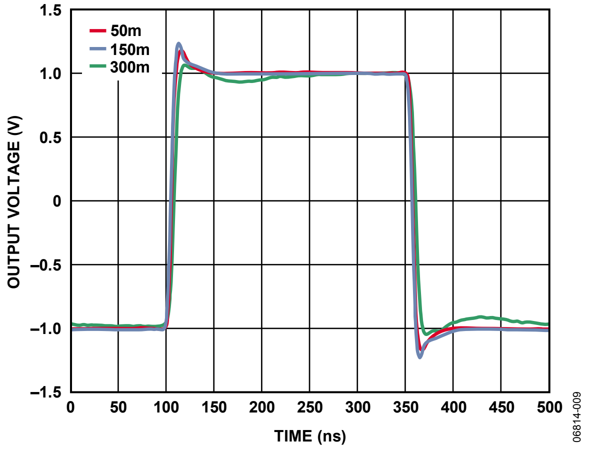


Figure 11. Pulse Response for Various Cable Lengths (2 MHz)

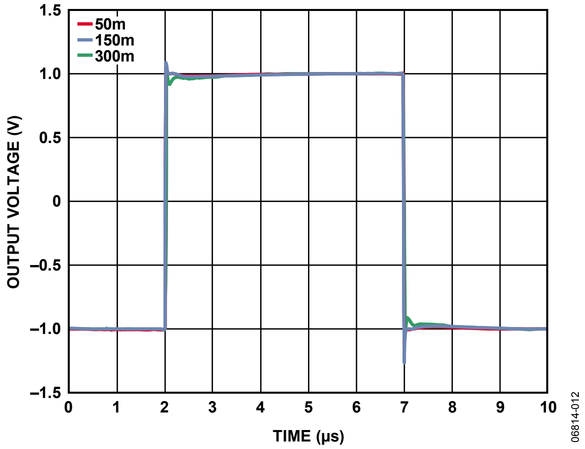


Figure 14. Pulse Response for Various Cable Lengths (100 kHz)

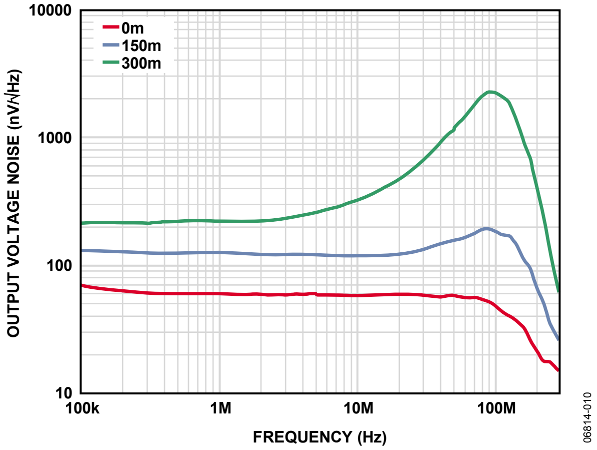


Figure 12. Output Voltage Noise vs. Frequency for Various Cable Length

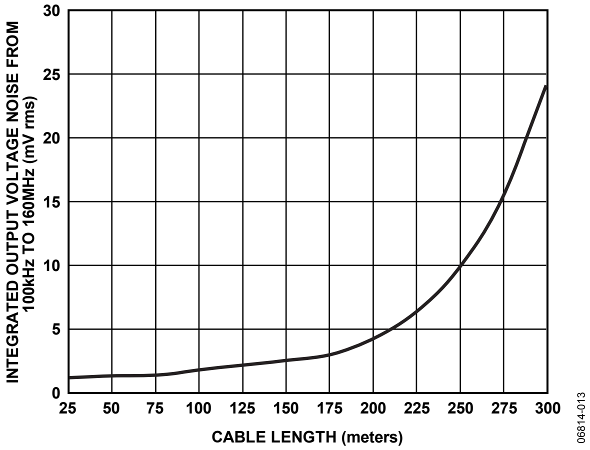


Figure 15. Integrated Output Voltage Noise vs. Cable Length

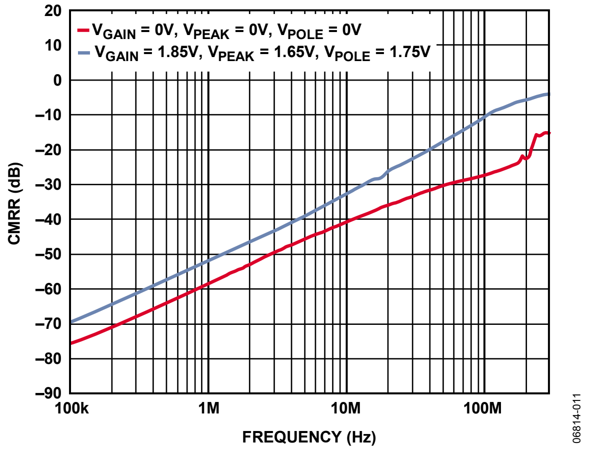


Figure 13. CMRR vs. Frequency

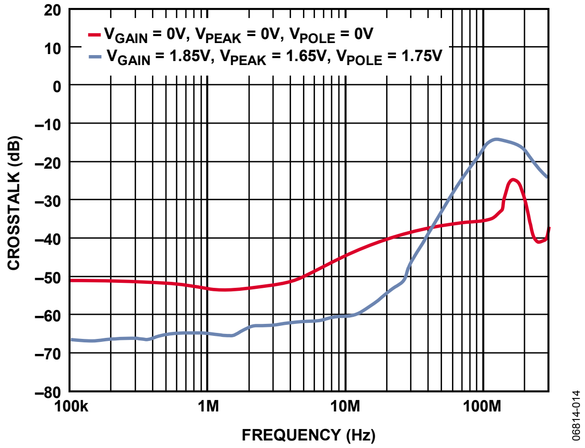


Figure 16. Crosstalk vs. Frequency

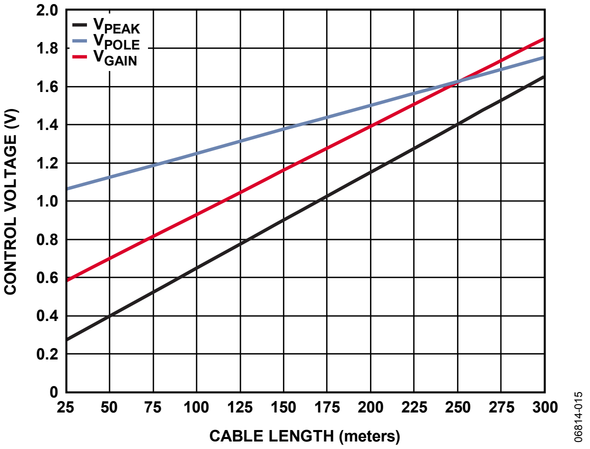


Figure 17. Recommended Settings for UTP Cable

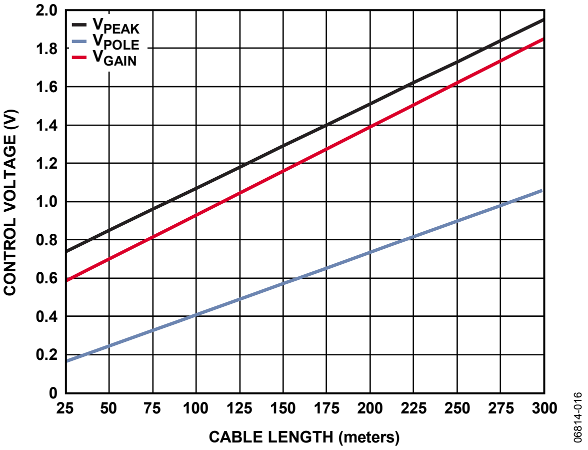


Figure 18. Recommended Settings for Coaxial Cable

THEORY OF OPERATION

The AD8123 is a unity-gain, triple, wideband, low noise analog line equalizer that compensates for losses in UTP and coaxial cables up to 300 meters in length. The 3-channel architecture is targeted at high resolution RGB applications but can be used in HD YPbPr applications as well.

Three continuously adjustable control voltages, common to the RGB channels, are available to the designer to provide compensation for various cable lengths as well as for variations in the cable itself. The V_{PEAK} input is used to control the amount of high frequency peaking. V_{PEAK} is the primary control that is used to compensate for frequency and cable-length dependent, high frequency losses that are present due to the skin effect of the cable. A second control pin, V_{GAIN}, is used to adjust broadband gain to compensate for low frequency flat losses present in the cable. A third control, V_{POLE}, is used to move the positions of the equalizer poles and can be linearly derived from V_{PEAK}, as illustrated in the Typical Performance Characteristics and Applications Information sections, for UTP and coaxial cables. Finally, an output offset adjust control, V_{OFFSET}, allows the designer to shift the output dc level.

The AD8123 has a high impedance differential input that makes termination simple and allows dc-coupled signals to be received directly from the cable. The AD8123 input can also be used in a single-ended fashion in coaxial cable applications. For differential systems that require very high CMRR, a triple differential receiver, such as the AD8143 or AD8145, can be placed in front of the AD8123.

The AD8123 has a low impedance output that is capable of driving a 150 Ω load. For systems where the AD8123 has to drive a high impedance capacitive load, it is recommended that a small series resistor be placed between the output and load to buffer the capacitance. The resistor should not be so large as to reduce the overall bandwidth to an unacceptable level.

The AD8123 is designed such that systems that use short-to-medium-length cables do not pay a noise penalty for excess gain that they do not require. The high gain is only available for longer length systems where it is required. This feature is built into the V_{PEAK} control and is transparent to the user.

Two comparators are provided on-chip that can be used for sync pulse extraction in systems that use sync-on-common mode encoding. Each comparator has very low output impedance and can therefore be used in a source-only cable termination scheme by placing a series resistor equal to the cable characteristic impedance directly on the comparator output. Additional details are provided in the Applications Information section.

INPUT COMMON-MODE VOLTAGE RANGE CONSIDERATIONS

When using the AD8123 as a receiver, it is important to ensure that its input common-mode voltage stays within the specified range. The received common-mode level is calculated by adding the common-mode level of the driver, the single-ended peak amplitude of the received signal, the amplitude of any sync pulses, and the other induced common-mode signals, such as ground shifts between the driver and the AD8123 and pickup from external sources, such as power lines and fluorescent lights. See the Applications Information section for more details.

APPLICATIONS INFORMATION

BASIC OPERATION

The AD8123 is easy to apply because it contains everything on-chip needed for cable loss compensation. Figure 20 shows a basic application circuit (power supplies not shown) with common-mode sync pulse extraction that is compatible with the common-mode sync pulse encoding technique used in the AD8134, AD8147, and AD8148 triple differential drivers. If sync extraction is not required, the terminations can be single 100 Ω resistors, and the comparator inputs can be left floating. In Figure 20, the AD8123 is feeding a high impedance input, such as a delay line or crosspoint switch, and the additional gain of two that makes up for double termination loss is not required.

COMPARATORS

In addition to general-purpose applications, the two on-chip comparators can be used to extract video sync pulses from the received common-mode voltages or to receive differential digital information. Built-in hysteresis helps to eliminate false triggers from noise. The Sync Pulse Extraction Using Comparators section describes the sync extraction details.

The comparator outputs have nearly 0 Ω output impedance and are designed to drive source-terminated transmission lines. The source termination technique uses a resistor in series with each comparator output such that the sum of the comparator source resistance (≈0 Ω) and the series resistor equals the transmission line characteristic impedance. The load end of the transmission line is high impedance. When the signal is launched into the source termination, its initial value is one-half of its source value because its amplitude is divided by two in the voltage divider formed by the source termination and the transmission line. At the load, the signal experiences nearly 100% positive reflection due to the high impedance load and is restored to nearly its full value. This technique is commonly used in PCB layouts that involve high speed digital logic.

Figure 19 shows how to apply the comparators with source termination when driving a 50 Ω transmission line that is high impedance at its receive end.

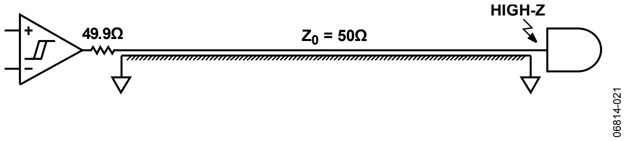


Figure 19. Using Comparator with Source Termination

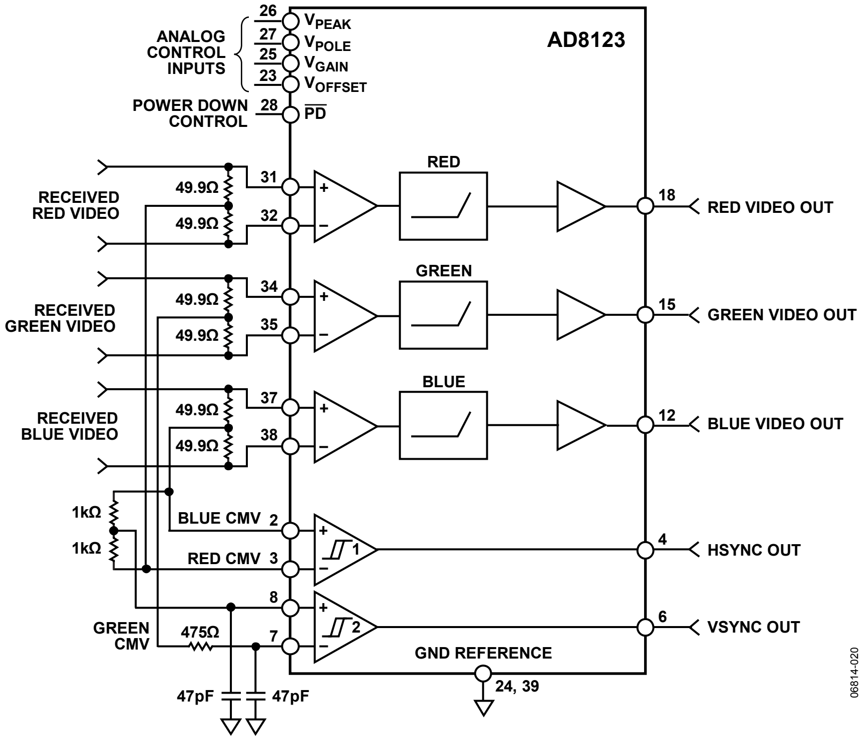


Figure 20. Basic Application Circuit with Common-Mode Sync Extraction

SYNC PULSE EXTRACTION USING COMPARATORS

The AD8123 is useful in many systems that transport computer video signals, which are typically comprised of red, green, and blue (RGB) video signals and separate horizontal and vertical sync signals. Because the sync signals are separate and not embedded in the color signals, it is advantageous to transmit them using a simple scheme that encodes them among the three common-mode voltages of the RGB signals. The AD8134, AD8147, and AD8148 triple differential drivers are natural complements to the AD8123 because they perform the sync pulse encoding with the necessary circuitry on-chip.

The sync encoding equations follow:

$$Red\ V_{CM} = \frac{K}{2}\left[V - H\right] \tag{1}$$

$$Green\ V_{CM} = \frac{K}{2}\left[-2\ \mathrm{V}\right] \tag{2}$$

$$Blue\ V_{CM} = \frac{K}{2}\left[V + H\right] \tag{3}$$

where:
Red V_{CM}, *Green* V_{CM}, and *Blue* V_{CM} are the transmitted common-mode voltages of the respective color signals.
K is an adjustable gain constant that is set by the driver.
V and H are the vertical and horizontal sync pulses, defined with a weight of −1 when the pulses are in their low states, and a weight of +1 when they are in their high states.

The AD8134 and AD8146/AD8147/AD8148 data sheets contain further details regarding the encoding scheme. Figure 20 illustrates how the AD8123 comparators can be used to extract the horizontal and vertical sync pulses that are encoded on the RGB common-mode voltages by the aforementioned drivers.

USING THE V_{PEAK}, V_{POLE}, V_{GAIN}, AND V_{OFFSET} INPUTS

The V_{PEAK} input is the main peaking control and is used to compensate for the low-pass roll-off in the cable response. The V_{POLE} input is a secondary frequency response shaping control that shifts the positions of the equalizer poles. The V_{GAIN} input controls the wideband flat gain and is used to compensate for the low frequency cable loss that is nominally flat. The V_{OFFSET} input is used to produce an offset at the AD8123 output. The output offset is equal to the voltage applied to the V_{OFFSET} input, limited by the output swing limits.

The V_{PEAK} and V_{POLE} controls can be used independently or they can be coupled to form a single peaking control. While Figure 17 and Figure 18 show recommended settings vs. cable length, designers may find other combinations that they prefer. These two controls give designers extra freedom, as well as the ability to compensate for different cable types (such as UTP and coaxial cable), as opposed to having only a single frequency shaping control.

In some cases, as would likely be with automatic control, the V_{PEAK} control is derived from a low impedance source, such as an op amp. Figure 21 shows how to derive V_{POLE} from V_{PEAK} in a UTP application according to the recommended curves shown in Figure 17, when V_{PEAK} originates from a low impedance source. Clearly, the 5 V supply must be clean to provide a clean V_{POLE} voltage.

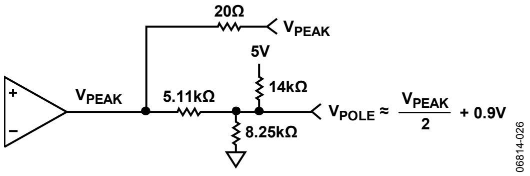


Figure 21. Deriving V_{POLE} from V_{PEAK} with Low-Z Source for UTP Cable

The 20 Ω series resistor in the V_{PEAK} path provides capacitive load buffering for the op amp. This value can be modified, depending on the actual capacitive load.

In automatic equalization circuits that place the control voltages inside feedback loops, attention must be paid to the poles produced by the summing resistors and load capacitances.

The peaking can also be adjusted by a mechanical or digitally controlled potentiometer. In these cases, if the resistance of the potentiometer is a couple of orders of magnitude lower than the values of the resistors used to develop V_{POLE}, its resistance can be ignored. Figure 22 shows how to use a 500 Ω potentiometer with the resistor values shown in Figure 21 scaled up by a factor of 10.

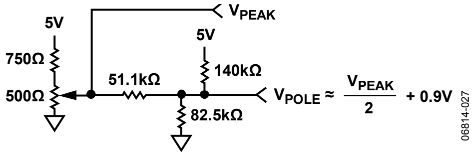


Figure 22. Deriving V_{POLE} from V_{PEAK} with Potentiometer for UTP Cable

Many potentiometers have wide tolerances. If a wide tolerance potentiometer is used, it may be necessary to change the value of the 750 Ω resistor to obtain a full swing for V_{PEAK}.

The V_{GAIN} input is essentially a contrast control and can be set by adjusting it to produce the correct amplitude of a known test signal (such as a white screen) at the AD8123 output.

V_{GAIN} can also be derived from V_{PEAK} according to the linear relationships shown in Figure 17 and Figure 18. Figure 23 shows how to derive V_{POLE} and V_{GAIN} from V_{PEAK} in a UTP application that originates from a low-Z source.

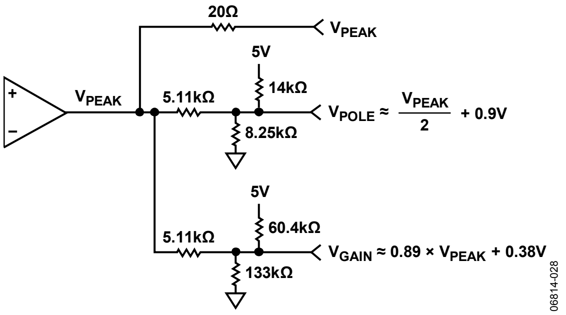


Figure 23. Deriving V_{POLE} and V_{GAIN} from V_{PEAK} with Low-Z Source for UTP Cable

USING THE AD8123 WITH COAXIAL CABLE

The V_{POLE} control allows the AD8123 to be used with other types of cable, including coaxial cable. Figure 18 presents the recommended settings for V_{PEAK}, V_{POLE}, and V_{GAIN} when the AD8123 is used with good quality 75 Ω video cable. Figure 24 shows how to derive V_{POLE} and V_{GAIN} from V_{PEAK} in a coaxial cable application where V_{PEAK} originates from a low-Z source.

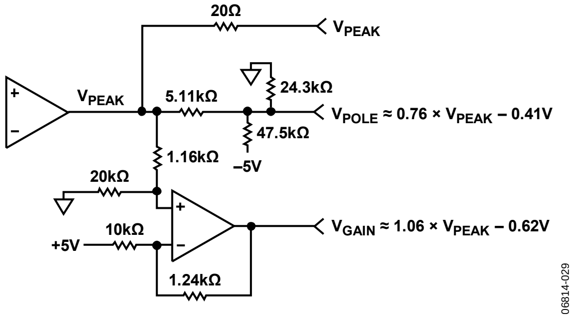


Figure 24. Deriving V_{POLE} and V_{GAIN} from V_{PEAK} with Low-Z Source for Coaxial Cable

The op amp in the circuit that develops V_{GAIN} is required to insert the offset of −0.62 V with a gain from V_{PEAK} to V_{GAIN} that is close to unity. A passive offset circuit would require an offset injection voltage that is much larger in magnitude than the available −5 V supply. Clearly, the V_{GAIN} control voltage can also be developed independently.

The AD8123 differential input can accept signals carried over unbalanced cable, as shown in Figure 25, for an unbalanced 75 Ω coaxial cable termination.

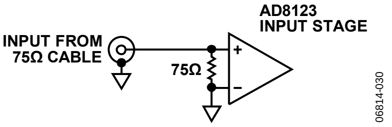


Figure 25. Terminating a 75 Ω Cable

DRIVING 75 Ω VIDEO CABLE WITH THE AD8123

When the RGB outputs must drive a 75 Ω line rather than a high impedance load, an additional gain of two is required to make up for the double termination loss (75 Ω source and load terminations). There are two options available for this.

One option is to place the additional gain of 2 at the drive end by using the AD8148 triple differential driver to drive the cable. The AD8148 has a fixed gain of 4 instead of the usual gain of 2 and thereby provides the required additional gain of 2 without having to add additional amplifiers to the signal chain. The AD8148 also contains sync-on-common-mode encoding. If sync-on-common-mode is not required, it can be deactivated on the AD8148 by connecting its SYNC LEVEL input to ground.

The other option is to include a triple gain-of-2 buffer, such as the ADA4862-3, on the AD8123 RGB outputs, as shown in Figure 26 for one channel (power supplies not shown). The ADA4862-3 provides the gain of 2 that compensates for the double-termination loss.

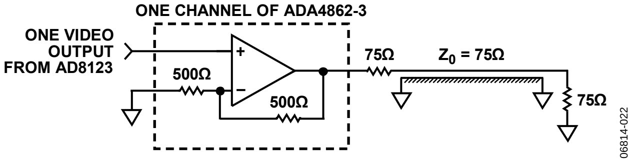


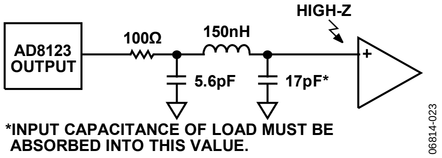
Figure 26. Using ADA4862-3 on AD8123 Outputs

DRIVING A CAPACITIVE LOAD

When driving a high impedance capacitive input, it is necessary to place a small series resistor between each of the three AD8123 video outputs and the load to buffer the input capacitance of the device being driven. Clearly, the resistor value must be small enough to preserve the required bandwidth.

FILTERING THE RGB OUTPUTS

In some cases, it is desirable to place low-pass filters on the AD8123 video outputs to reduce high frequency noise. A 3-pole Butterworth filter with cutoff frequency in the neighborhood of 140 MHz is sufficient in most applications. Figure 27 and Figure 28 present filters for the high impedance load case (driving a delay line, crosspoint switch, ADA4862-3) and the double-termination case (75 Ω source and load resistances), respectively. In the high impedance load case, the load capacitance must be absorbed in the capacitor that is placed across the load. For example, in Figure 27, if the high-Z load were the input to an ADA4862-3, which has an input capacitance of 2 pF, the filter capacitor value in parallel with the input would be 15 pF to obtain 17 pF.



*INPUT CAPACITANCE OF LOAD MUST BE ABSORBED INTO THIS VALUE.

Figure 27. 140 MHz Low-Pass Filter on AD8123 Output Feeding High-Z Load

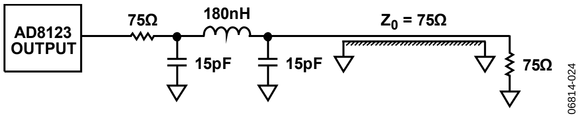


Figure 28. 135 MHz Low-Pass Filter on AD8123 Output Feeding Doubly Terminated Load

These filters are by no means the only choices but are presented here as examples. In the high-Z load case, it is important to keep the filter source resistance large enough to buffer the capacitive loading presented by the first capacitor in the filter.

POWER SUPPLY FILTERING

External power supply filtering between the system power supplies and the AD8123 is required in most applications to prevent supply noise from contaminating the received signal as well as to prevent unwanted feedback through the supplies that could cause instability. Figure 29 shows that the AD8123 power supply rejection decreases with increasing frequency. These plots are for the lowest control settings and shift upward as the peaking is increased.

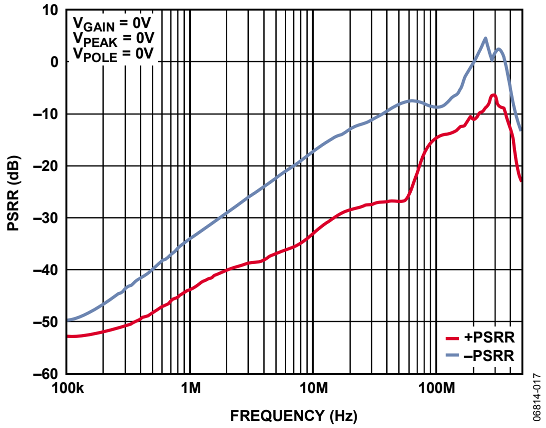


Figure 29. AD8123 PSRR vs. Frequency

A suitable filter that uses a surface-mount ferrite bead is shown in Figure 30, and its frequency response is shown in Figure 31. Because the frequency response was taken using a 50 Ω network analyzer and with only one 0.1 μF capacitor on the AD8123 side, the actual amount of rejection provided by the filter in a real-world application will be different from that shown in Figure 31. The general shape of the rejection curve, however, matches Figure 31, providing substantially increased overall PSRR from approximately 5 MHz to 500 MHz, where it is most needed. One filter is required on each of the two supplies (not one filter per supply pin).

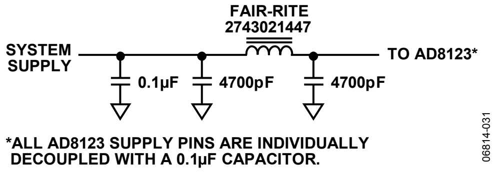


Figure 30. Power Supply Filter

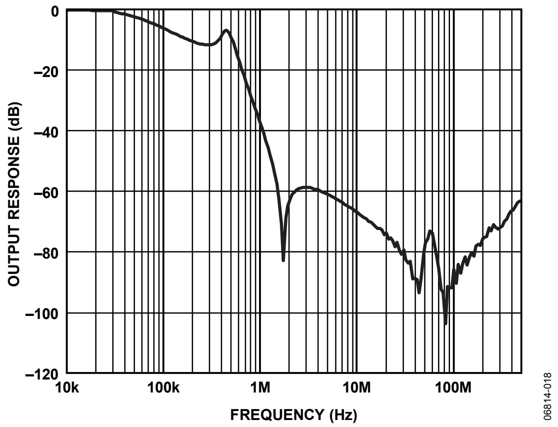


Figure 31. Power Supply Filter Frequency Response in a 50 Ω System

LAYOUT AND POWER SUPPLY DECOUPLING CONSIDERATIONS

Standard high speed PCB layout practices must be adhered to when designing with the AD8123. A solid ground plane is required and controlled impedance traces must be used when interconnecting the high speed signals. Source termination resistors on all of the outputs must be placed as close as possible to the output pins.

The exposed paddle on the underside of the AD8123 must be connected to a pad that connects to at least one PCB plane. Use several thermal vias to make the connection between the pad and the plane(s).

High quality 0.1 μF power supply decoupling capacitors must be placed as close as possible to all of the supply pins. Use small surface-mount ceramic capacitors for these. Tantalum capacitors are recommended for bulk supply decoupling.

INPUT COMMON-MODE RANGE

Most applications that use the AD8123 as a receiver use a driver (such as one from the AD8146/AD8147/AD8148 family, the AD8133, or the AD8134) powered from ±5 V supplies. This places the common-mode voltage on the line nominally at 0 V relative to the ground potential at the driver and provides optimum immunity from any common-mode anomalies picked up along the cable (including ground shifts between the driver and receiver ends). In many of these applications, the AD8123 input voltage range of typically ±3.0 V is sufficient. If wider input range is required, the AD8143 triple receiver (input common-mode range equals ±10.5 V on ±12 V supplies) can be placed in front of the AD8123. Figure 32 illustrates how this is done for one channel.

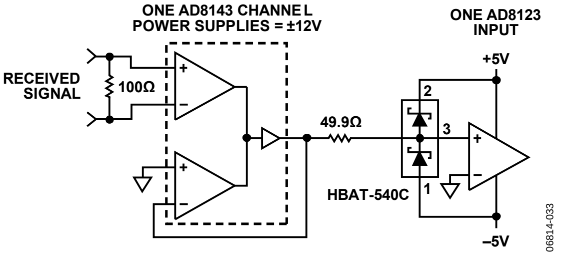


Figure 32. Optional Use of AD8143 in Front of AD8123 for Wide Input Common-Mode Range

The Schottky diodes are required to protect the AD8123 from any AD8143 outputs that may exceed the AD8123 input limits. The 49.9 Ω resistor limits the fault current and produces a pole at approximately 800 MHz with the effective diode capacitance of 3 pF and the AD8123 input capacitance of 1 pF. The pole drops the response by only 0.07 dB at 100 MHz and therefore has a negligible effect on the signal.

When using a single 5 V supply on the driver side, the common-mode voltage at the driver is typically midsupply, or V_{CM} = 2.5 V. The largest received differential video signal is approximately 700 mV p-p, and this therefore adds 175 mV_{PEAK} to the common-mode voltage, resulting in a worst-case peak voltage of 2.675 V on an AD8123 input (presuming there is no ground shift between driver and receiver). This is within the AD8123 input voltage swing limits, and such a system works well as long as the difference in ground potential between driver and receiver does not cause the input voltage swing to exceed its specified limits.

When used, common-mode sync signals are generally applied with a peak deviation of 500 mV and thereby increase the common-mode level from 2.675 V to 3.175 V. This common-mode level exceeds the specified input voltage swing limits of ±3.0 V; therefore, the AD8123 cannot be used with a system that uses common-mode sync encoding with 500 mV sync peak deviation and 2.5 V common-mode line level. While it is possible to operate a driver powered from a single 5 V supply at a common-mode voltage of <2.5 V to obtain a received voltage swing that is within the specified limits, there is not much margin for other shifts in the common-mode level due to interference pickup and differing ground potentials. There are two ways to increase the common-mode range of the overall system. One is to power the driver from ±5 V supplies, and the other is to place an AD8143 in front of the AD8123, as shown in Figure 32. These techniques can be combined or applied separately.

SMALL SIGNAL FREQUENCY RESPONSE

Though the AD8123 large signal frequency response (V_O = 1 V p-p) is of most concern, occasionally designers are interested in the small signal frequency response. The AD8123 frequency response for V_O = 300 m V p-p is shown in Figure 33 for 200 meter and 300 meter cable lengths.

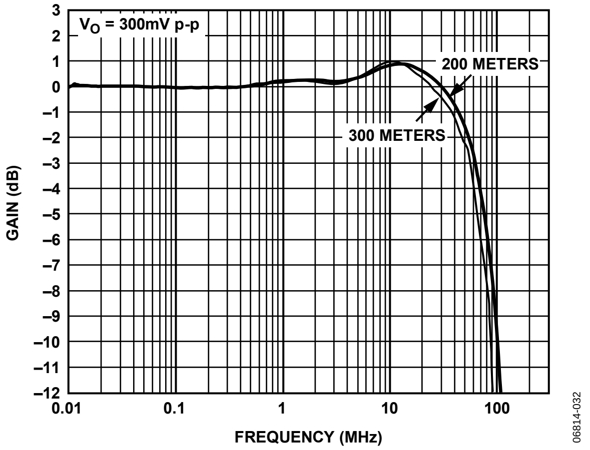
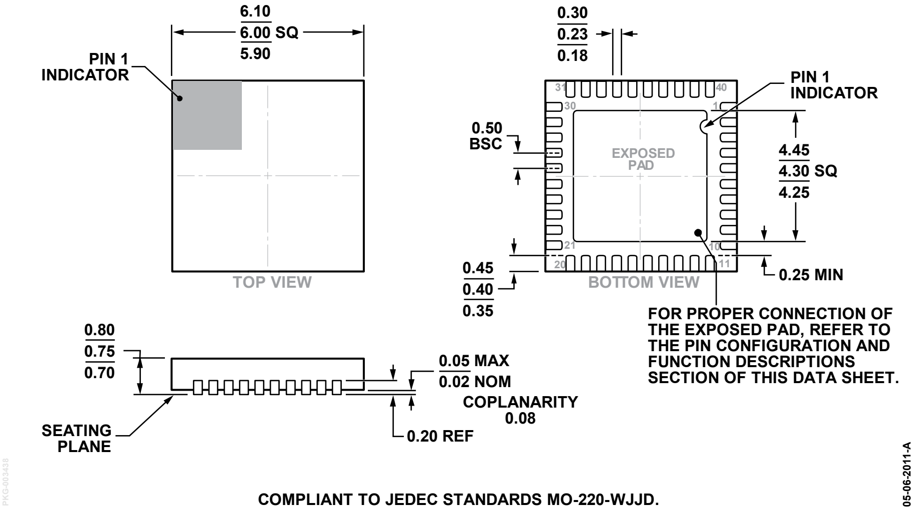


Figure 33. Small Signal Frequency Response for Various Cable Lengths

POWER-DOWN

The power-down feature is intended to be used to reduce power consumption when a particular device is not in use and does not place the output in a high-Z state when asserted. The input logic levels and supply current in power-down mode are presented in the Power Supply section of Table 1.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WJJD.

Figure 34. 40-Lead Lead Frame Chip Scale Package [LFCSP]
6 mm × 6 mm Body and 0.75 mm Package Height
(CP-40-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8123ACPZ	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package (LFCSP)	CP-40-10
AD8123ACPZ-R7	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package (LFCSP)	CP-40-10
AD8123ACPZ-RL	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package (LFCSP)	CP-40-10

[1] Z = RoHS Compliant Part.

D06814-0-1/16(B)