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May 2012

FAN6862R / FAN6862L
Highly Integrated Green-Mode PWM Controller

Features

- Low Startup Current: 8μA
- Low Operating Current in Green Mode: 3mA
- Peak-Current-Mode Operation with Cycle-by-Cycle Current Limiting
- PWM Frequency Continuously Decreasing with Burst Mode at Light Loads
- V_{DD} Over-Voltage Protection (OVP)
- Constant Output Power Limit (Full AC Input Range)
- Over-Temperature Protection (OTP)
- Fixed PWM Frequency (65KHz) with Frequency Hopping
- Feedback Open-Loop Protection with 56ms Delay
- Soft-Start Time: 5ms
- 400mA Driving Capability

Applications

General-purpose switch-mode power supplies and flyback power converters, including:

- Power Adapters
- Open-Frame SMPS
- SMPS with Surge-Current Output, such as for Printers, Scanners, and Motor Drivers

Description

A highly integrated PWM controller, FAN6862R/L provides several features to enhance the performance of flyback converters. To minimize standby power consumption, a proprietary green-mode function provides off-time modulation to continuously decrease the switching frequency under light-load conditions. Under zero-load conditions, the power supply enters burst mode, which completely shuts off PWM output. Output restarts just before the supply voltage drops below the UVLO lower limit. This green-mode function enables power supplies to meet international power conservation requirements.

The FAN6862R/L is designed for SMPS and integrates a frequency-hopping function that helps reduce EMI emission of a power supply with minimum line filters. The built-in synchronized slope compensation is proprietary sawtooth compensation for constant output power limit over universal AC input range. The gate output is clamped at 18V to protect the external MOSFET from over-voltage damage.

Other protection functions include V_{DD} over-voltage protection, over-temperature protection, and overload protection. For over-temperature protection, an external NTC thermistor can be applied to sense the ambient temperature. When OVP, OTP, or OLP is activated, an internal protection circuit switches off the controller.

Part Number	OVP	OTP	OLP
FAN6862RTY	Auto Restart	Auto Restart	Auto Restart
FAN6862LTY	Latch	Latch	Latch

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN6862RTY	-40 to +105°C	6-Pin SSOT-6	Tape & Reel
FAN6862LTY	-40 to +105°C	6-Pin SSOT-6	Tape & Reel

Typical Application

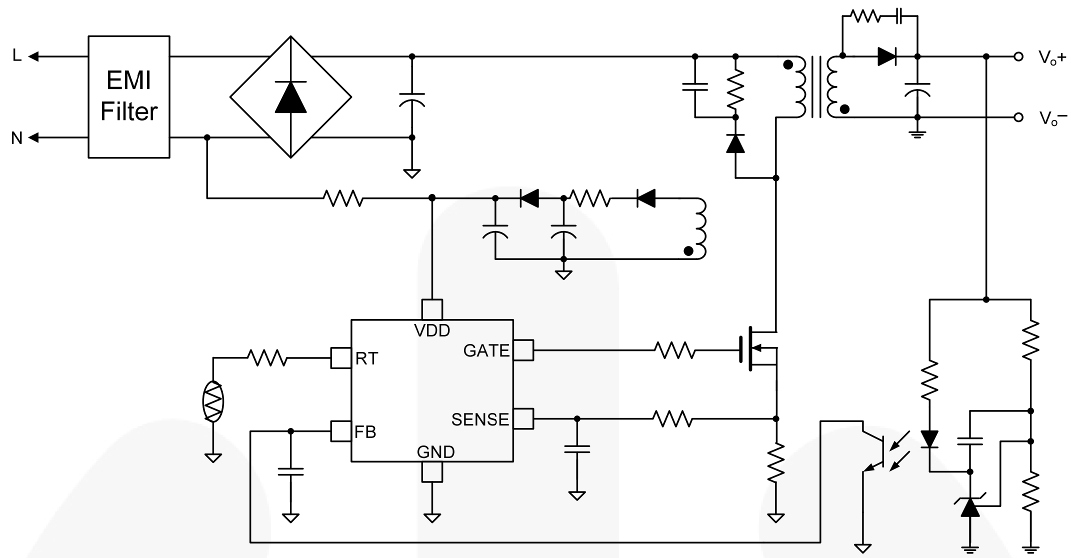

Figure 1. Typical Application

Block Diagram

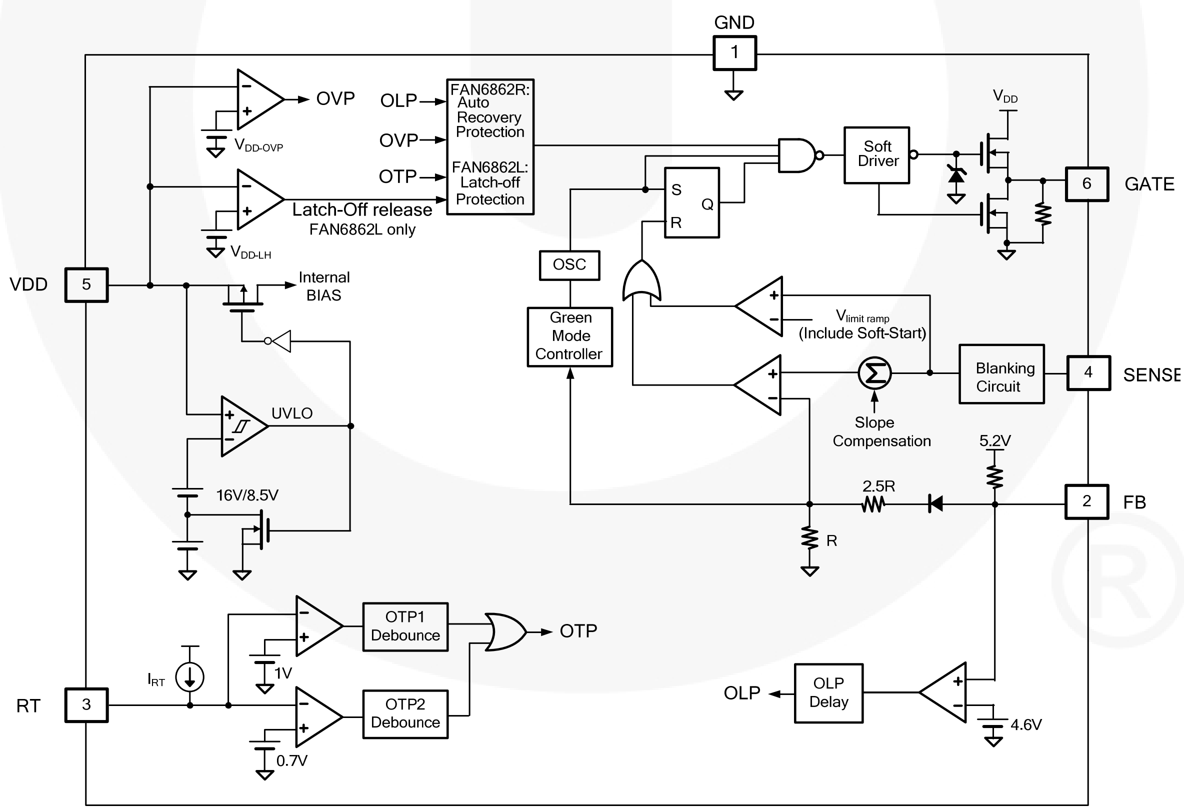

Figure 2. Block Diagram

Marking Information

Figure 3. Top Mark

Pin Configuration

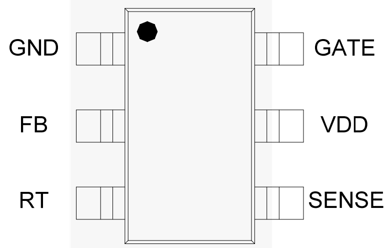

Figure 4. Pin Assignments

Pin Definitions

Pin #	Name	Function	Description
1	GND	Ground	Ground
2	FB	Feedback	The FB pin provides the output voltage regulation signal. It provides feedback to the internal PWM comparator for control of the duty cycle. This pin also provide for OLP: if V_{FB} is larger than the trigger level and remains for a long time, the controller stops and restarts.
3	RT	Temperature Detection	An external NTC thermistor is connected from this pin to GND for over-temperature protection. The impedance of the NTC decreases at high temperatures. Once the voltage of the RT pin drops below a threshold, PWM output is disabled.
4	SENSE	Current Sense	This pin senses the voltage across a resistor. When the voltage reaches the internal threshold, PWM output is disabled. This activates over-current protection. This pin also provides current amplitude information for current-mode control.
5	VDD	Power Supply	Power supply
6	GATE	Driver Output	The totem-pole output driver for driving the power MOSFET.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. All voltage values, except differential voltages, are given with respect to GND pin.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply Voltage		30	V
V_L	Input Voltage to FB, SENSE, RT Pin	-0.3	7.0	V
P_D	Power Dissipation at T_A<50°C		300	mW
Θ_{JC}	Thermal Resistance (Junction-to-Case)		115	°C/W
T_J	Operating Junction Temperature	-40	+150	°C
T_{STG}	Storage Temperature Range	-55	+150	°C
T_L	Lead Temperature, Wave Soldering, 10 Seconds		+260	°C
ESD	Human Body Model, JESD22-A114		3.00	kV
	Charge Device Model, JESD22-C101		1.25	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T_A	Operating Ambient Temperature	-40	+105	°C

Electrical Characteristics

V_{DD} = 15V and T_A = 25°C unless otherwise noted.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DD} Section						
V_{DD-OP}	Continuously Operating Voltage				24	V
V_{DD-ON}	Turn-On Threshold Voltage		15	16	17	V
V_{DD-OFF}	Turn-Off Voltage		7.5	8.5	9.5	V
V_{DD-OVP}	V_{DD} Over-Voltage Protection (Latch-Off)		24	25	26	V
V_{DD-LH}	Threshold Voltage for Latch-Off Release		3	4	5	V
I_{DD-ST}	Startup Current	V_{DD-ON}–0.16V		8	30	μA
I_{DD-OP}	Normal Operating Supply Current	C_L=1nF		3	4	mA
I_{DD-BM}	Green-Mode Operating Supply Current	GATE Open, V_{FB}=V_{FB-G}			2.5	mA
V_{DD-OVP}	V_{DD} Over-Voltage Protection		24	25	26	V
$t_{D-VDDOVP}$	V_{DD} OVP Debounce Time			30	50	μs
I_{DD-LH}	Latch-Off Holding Current	V_{DD}=5V		40	65	μA
Feedback Input Section						
A_V	Input-Voltage to Current-Sense Attenuation		1/4.0	1/3.5	1/3.0	V/V
Z_{FB}	Input Impedance			5.5		kΩ
$V_{FB-OPEN}$	FB Pin Open Voltage		5.0	5.2	5.4	V
V_{FB-OLP}	Threshold Voltage for Open-Loop Protection		4.3	4.6	4.9	V
t_{D-OLP}	Open-Loop Protection Delay Time		53	56	60	ms
Current Sense Section						
t_{PD}	Delay to Output			100	250	ns
t_{LEB}	Leading-Edge Blanking Time		270	360		ns
V_{STHFL}	Flat Threshold Voltage for Current Limit	Duty>51%	0.47	0.50	0.53	V
V_{STHVA}	Valley Threshold Voltage for Current Limit	Duty=0%	0.41	0.44	0.47	V
V_{SLOPE}	Slope Compensation	Duty=DCY_{MAX}		0.273		V
$t_{SOFT-START}$	Period During Startup Time		2.50	4.00	5.25	ms
Oscillator Section						
f_{OSC}	Normal PWM Frequency — Center Frequency	V_{FB}>V_{FB-N}	62	65	68	kHz
	Normal PWM Frequency — Hopping Range	V_{FB}≥V_{FB-N}	±3.7	±4.2	±4.7	kHz
	Normal PWM Frequency — Hopping Range[*1]	V_{FB}=V_{FB-G}		±2.9		kHz
t_{hop-1}	Hopping Period 1[*1]	V_{FB}≥V_{FB-N}		4.4		ms
t_{hop-3}	Hopping Period 3[*1]	V_{FB}=V_{FB-G}		11.5		ms
f_{OSC-G}	Green Mode Minimum Frequency		18.0	22.5	25.0	kHz
V_{FB-N}	FB Threshold Voltage For Frequency Reduction		2.3	2.5	2.7	V
V_{FB-G}	FB Voltage at f_{OSC-G}		1.9	2.1	2.3	V
V_{FB-ZDC}	FB Threshold Voltage for Zero Duty			1.7		V
f_{DV}	Frequency Variation vs. V_{DD} Deviation	V_{DD}=11.5V to 20V	0	0.02	2.00	%
f_{DT}	Frequency Variation vs. Temperature Deviation	T_A= -40 to +105°C			2	%

Continued on the following page…

Electrical Characteristics (Continued)

V_{DD} = 15V and T_A = 25°C unless otherwise noted.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
PWM Output Section						
DCY_{MAX}	Maximum Duty Cycle		65	70	75	%
V_{OL}	Output Voltage Low	V_{DD}=15V, I_O=50mA			1.5	V
V_{OH}	Output Voltage High	V_{DD}=8V, I_O=50mA	6			V
t_R	Rising Time	C_L=1nF		150	200	ns
t_F	Falling Time	C_L=1nF		35	80	ns
V_{CLAMP}	Gate Output Clamping Voltage	V_{DD}=20V	15.0	16.5	18.0	V
Over-Temperature Protection (OTP) Section						
I_{RT}	Output Current of RT Pin		92	100	108	μA
V_{OTP}	Threshold Voltage for Over-Temperature Protection	T_A=25°C	0.97	1.02	1.07	V
t_{DOTP}	Over-Temperature Debounce Time	$V_{FB}=V_{FB-N}$	15	17	19	ms
		$V_{FB}=V_{FB-G}$ (1)		51		ms
V_{OTP2}	2nd Threshold Voltage for Over-Temperature Protection	T_A=25°C	0.60	0.70	0.75	V
t_{DOTP2}	2nd Over-Temperature Debounce Time		80	100	190	μs

Note:
1. Guarantee by design.

Typical Performance Characteristics

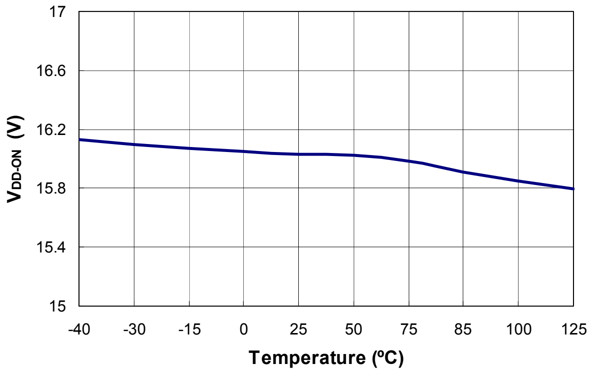

Figure 5. Turn-On Threshold Voltage (V_{DD-ON}) vs. Temperature

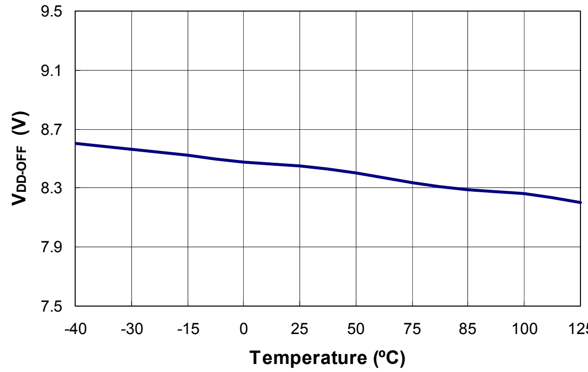

Figure 6. Turn-Off Threshold Voltage (V_{DD-OFF}) vs. Temperature

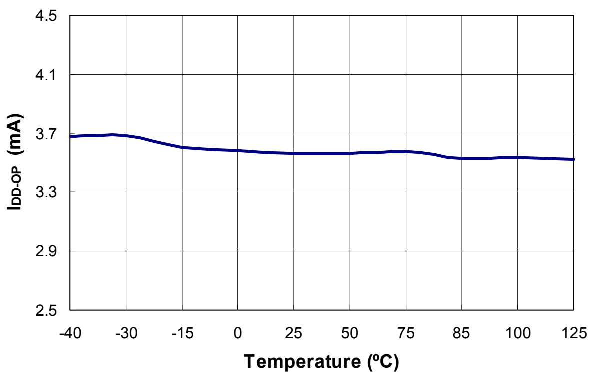

Figure 7. Operating Current (I_{DD-OP}) vs. Temperature

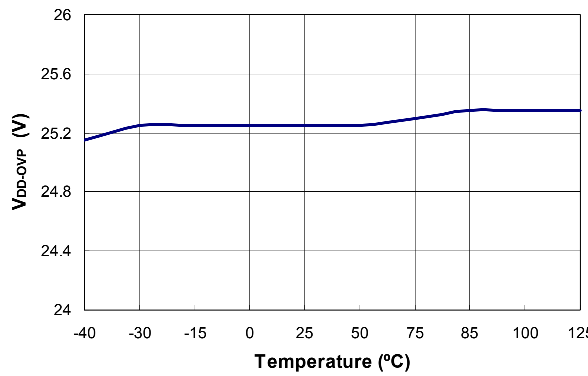

Figure 8. V_{DD} Over-Voltage Protection (V_{DD-OVP}) vs. Temperature

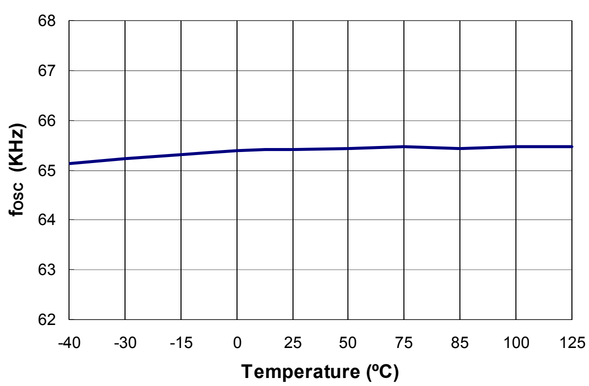

Figure 9. Center Frequency (f_{OSC}) vs. Temperature

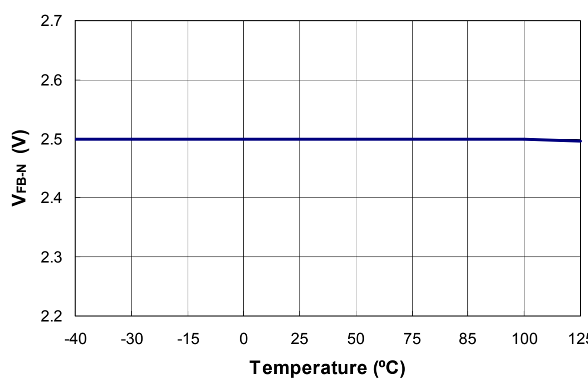

Figure 10. FB Threshold Voltage for Frequency Reduction (V_{FB-N}) vs. Temperature

Typical Performance Characteristics (Continued)

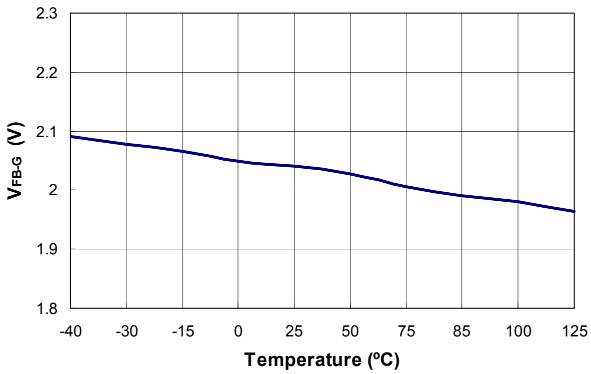

Figure 11. FB Voltage at f_{OSC-G} (V_{FB-G}) vs. Temperature

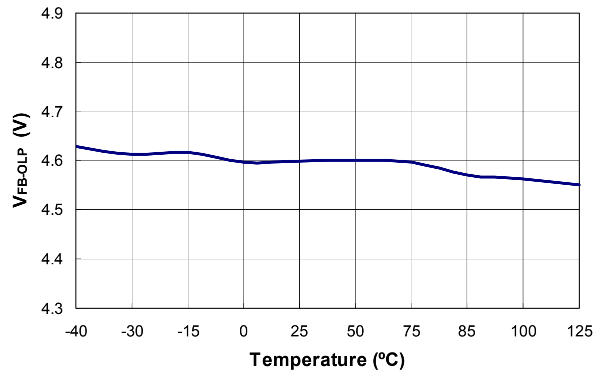

Figure 12. Threshold Voltage for Open-Loop Protection (V_{FB-OLP}) vs. Temperature

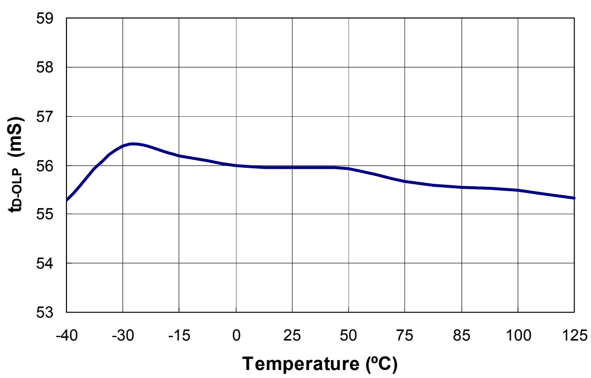

Figure 13. Open-Loop Protection Delay Time (t_{D-OLP}) vs. Temperature

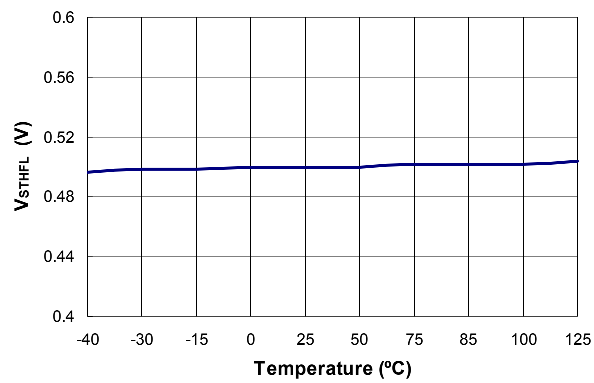

Figure 14. Flat Threshold Voltage for Current Limit (V_{STHFL}) vs. Temperature

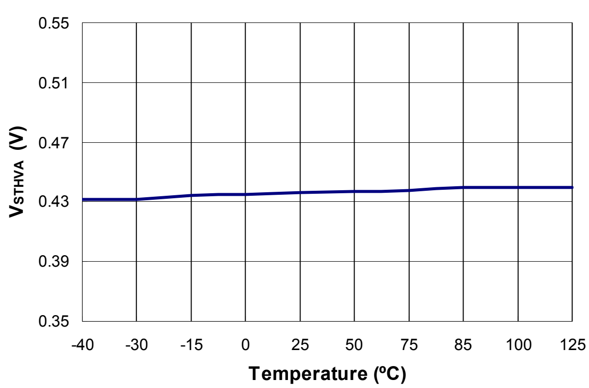

Figure 15. Valley Threshold Voltage for Current Limit (V_{STHVA}) vs. Temperature

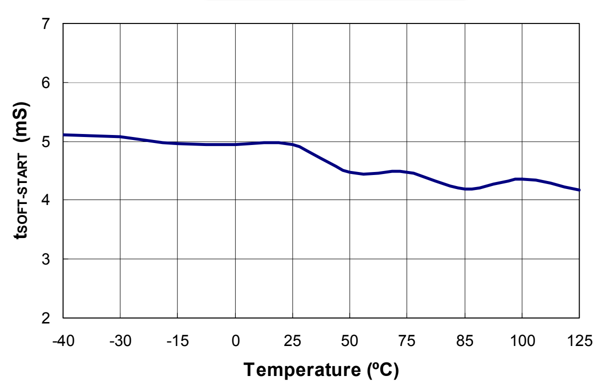

Figure 16. Period during Startup ($t_{SOFT-START}$) vs. Temperature

Typical Performance Characteristics (Continued)

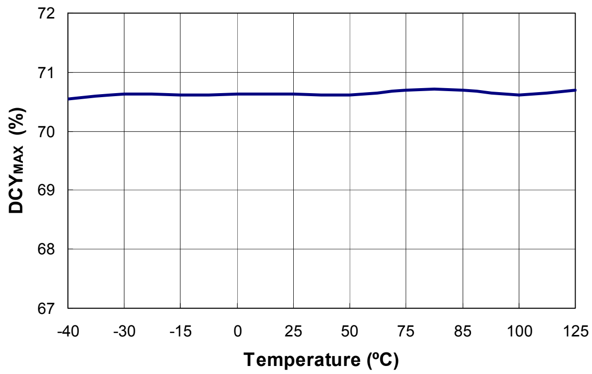

Figure 17. Maximum Duty Cycle (DCY_{MAX}) vs. Temperature

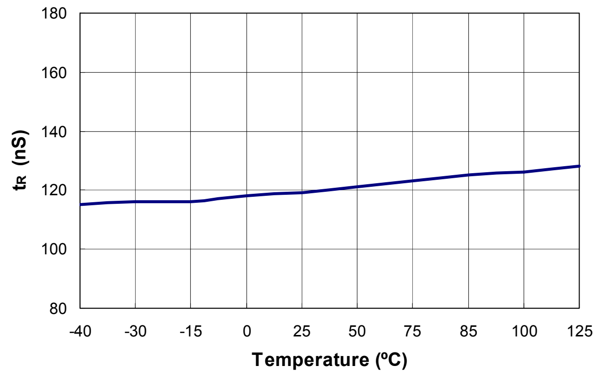

Figure 18. Rising Time (t_R) vs. Temperature

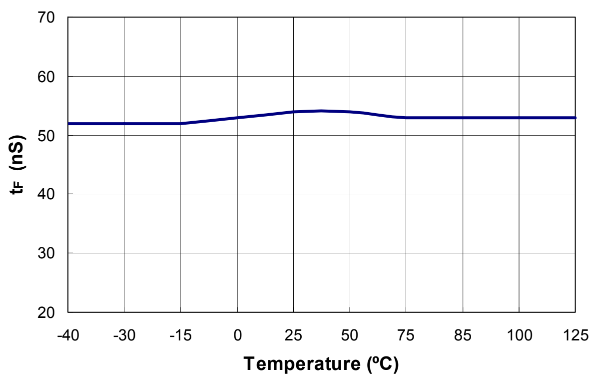

Figure 19. Falling Time (t_F) vs. Temperature

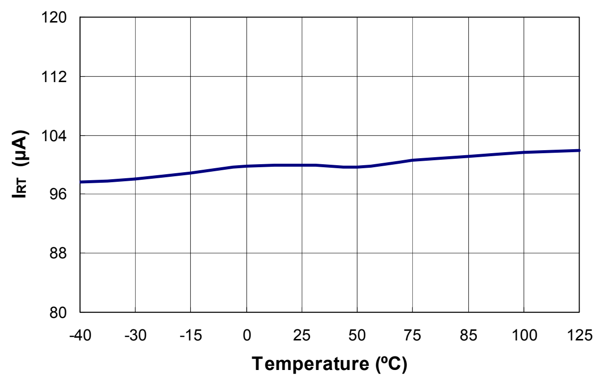

Figure 20. Output Current of RT Pin (I_{RT}) vs. Temperature

Operation Description

Startup Operation

Figure 21 shows a typical startup circuit and transformer auxiliary winding for a typical application. Before FAN6862R/L begins switching operation, it consumes only startup current (typically 8μA) and the current supplied through the startup resistor charges the V_{DD} capacitor (C_{DD}). When V_{DD} reaches the turn-on voltage of 16V ($V_{DD\text{-}ON}$), FAN6862R/L begins switching and the current consumed increases to 3mA. Then the power required is supplied from the transformer auxiliary winding. The large hysteresis of V_{DD} (8.5V) provides more holdup time, which allows using a small capacitor for V_{DD}. The startup resistor is typically connected to AC line for a fast reset of latch protection.

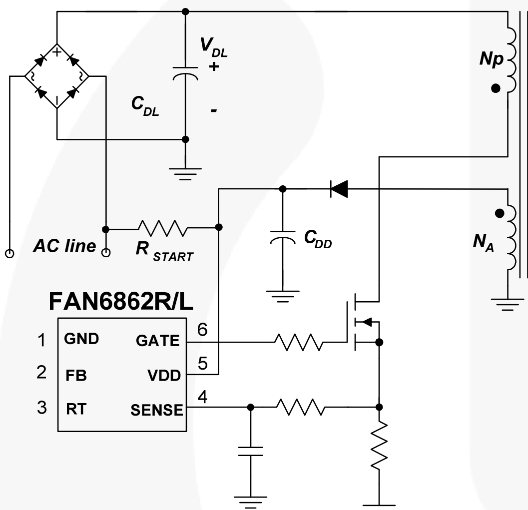

Figure 21. Startup Circuit

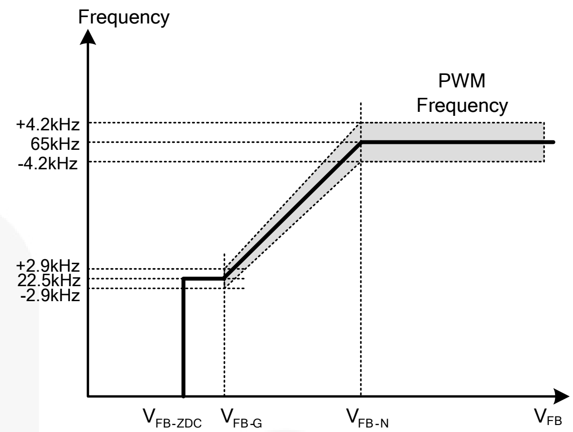

Figure 22. PWM Frequency

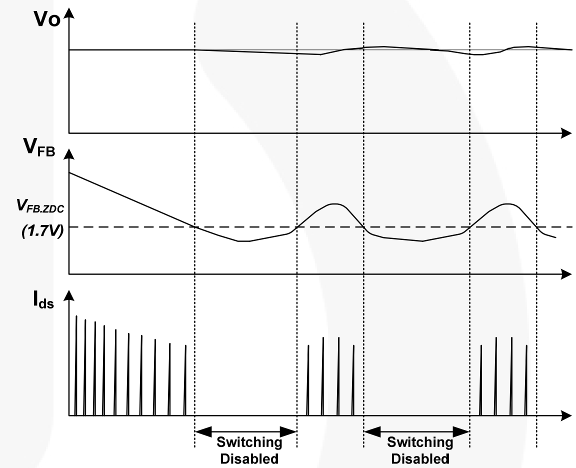

Figure 23. Burst-Mode Operation

Green-Mode Operation

The FAN6862R/L uses feedback voltage (V_{FB}) as an indicator of the output load and modulates the PWM frequency, as shown in Figure 22, such that the switching frequency decreases as load decreases. In heavy-load conditions, the switching frequency is 65KHz. Once V_{FB} decreases below $V_{FB\text{-}N}$ (2.5V), the PWM frequency starts to linearly decrease from 65KHz to 22.5kHz to reduce the switching losses. As V_{FB} decreases below $V_{FB\text{-}G}$ (2.1V), the switching frequency is fixed at 22.5kHz and FAN6862R/L enters "deep" green mode, where the operating current decreases to 2.5mA (maximum), further reducing the standby power consumption. As V_{FB} decreases below $V_{FB\text{-}ZDC}$ (1.7V), FAN6862R/L enters burst-mode operation. When V_{FB} drops below $V_{FB\text{-}ZDC}$, switching stops and the output voltage starts to drop, which causes the feedback voltage to rise. Once V_{FB} rises above $V_{FB\text{-}ZDC}$, switching resumes. Burst mode alternately enables and disables switching, thereby reducing switching loss in standby mode, as shown in Figure 23.

Frequency Hopping

EMI reduction is accomplished by frequency hopping, which spreads the energy over a wider frequency range than the bandwidth measured by the EMI test equipment. An internal frequency hopping circuit changes the switching frequency between 60.8kHz and 69.2kHz with a period of 4.4ms, as shown in Figure 24.

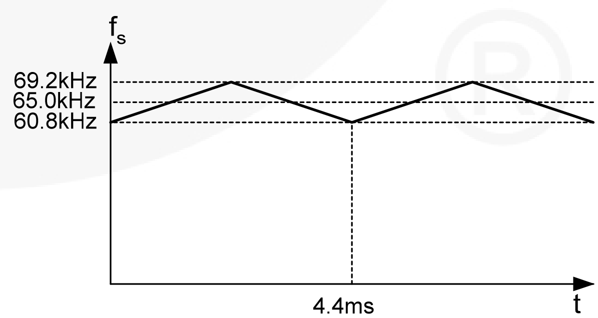

Figure 24. Frequency Hopping

Protections

Self-protective functions include V_{DD} Over-Voltage Protection (OVP), Open-Loop / Overload Protection (OLP), Over-Current Protection (OCP), Short-Circuit Protection, and Over-Temperature Protection (OTP). FAN6862R uses auto-restart mode protections and FAN6862L uses latch-mode protections.

Auto-Restart Mode Protection: Once a fault condition is detected, switching is terminated and the MOSFET remains off. This causes V_{DD} to fall because no more power is delivered from auxiliary winding. When V_{DD} falls to $V_{DD\text{-}OFF}$ (8.5V), the protection is reset and the operating current reduces to startup current, which causes V_{DD} to rise. FAN6862R resumes normal operation when V_{DD} reaches $V_{DD\text{-}ON}$ (16V). In this manner, the auto-restart can alternately enable and disable the switching of the MOSFET until the fault condition is eliminated (*see Figure 25*).

Latch-Mode Protection: Once this protection is triggered, switching is terminated and the MOSFET remains off. The latch is reset only when V_{DD} is discharged below 4V by unplugging AC power line.

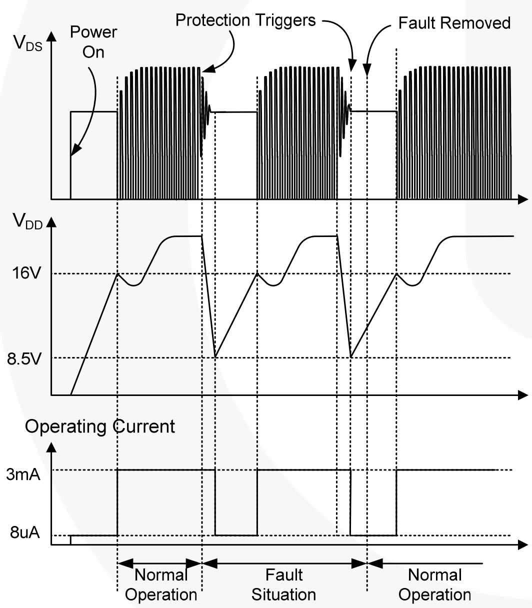

Figure 25. Auto-Restart Operation

Over-Current Protection (OCP)

FAN6862R/L has over-current protection thresholds. It is for pulse-by-pulse current limit, which turns off the MOSFET for the remainder of the switching cycle when the sensing voltage of MOSFET drain current reaches the threshold. The other threshold is for the over-current protection, which shuts down the MOSFET gate when the sensing voltage of MOSFET drain current is above the threshold longer than the shutdown delay (56ms).

Open-Loop / Overload Protection (OLP)

When the upper branch of the voltage divider for the shunt regulator (KA431 shown) is broken, as shown in Figure 26, no current flows through the opto-coupler transistor, which pulls up the feedback voltage to 5.2V.

When the feedback voltage is above 4.6V longer than 56ms, OLP is triggered. This protection is also triggered when the SMPS output drops below the nominal value longer than 56ms due to the overload condition.

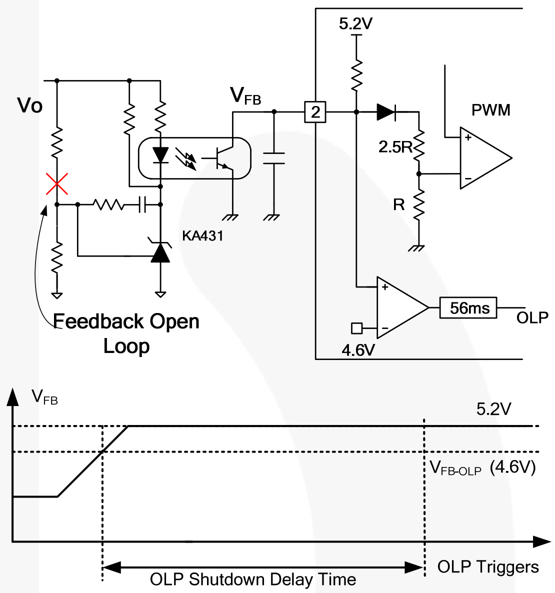

Figure 26. OLP Operation

V_{DD} Over-Voltage Protection (OVP)

V_{DD} over-voltage protection prevents IC damage caused by over voltage on the VDD pin. The OVP is triggered when V_{DD} reaches 25V. A debounce time (typically 30μs) prevents false triggering by switching noise.

Over-Temperature Protection (OTP)

The OTP circuit is composed of current source and voltage comparators. Typically, an NTC thermistor is connected between the RT and GND pins. Once the voltage of this pin drops below a threshold of 1.02V, PWM output is disabled after t_{DOTP} debounce time. If this pin drops below 0.7V, it triggers the latch-off protection immediately after t_{DOTP2} debounce time.

Constant Output Power Limit

FAN6862R/L has saw-limiter for pulse-by-pulse current limit, which guarantees almost constant power limit over different line voltages of universal input range.

The conventional pulse-by-pulse current limiting scheme has a constant threshold for current limit comparator, which results in a higher power limit for high line voltage. FAN6862R/L has a sawtooth current limit threshold that increases progressively within a switching cycle, which provides lower current limit for high line and makes the actual power limit level almost constant over different line voltages of universal input range, as shown in Figure 27.

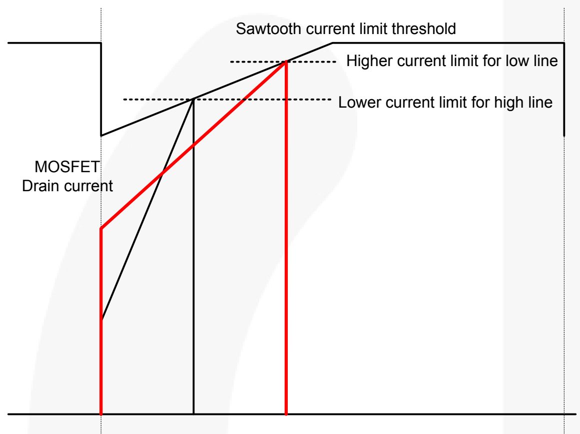

Figure 27. Sawtooth Current Limiter

Leading-Edge Blanking (t_{LEB})

Each time the power MOSFET is switched on, a turn-on spike occurs across the sense-resistor caused by primary-side capacitance and secondary-side rectifier reverse recovery. To avoid premature termination of the switching pulse, a leading-edge blanking time is built in. During this blanking period (360ns), the PWM comparator is disabled and cannot switch off the gate driver. Thus, RC filter with a small RC time constant is enough for current sensing.

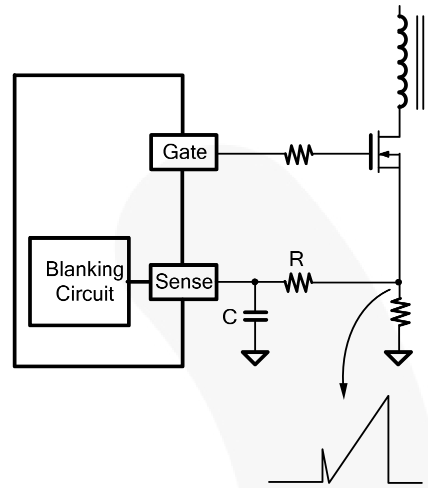

Figure 28. Current Sense R-C Filter

Soft-Start

The FAN6862R/L has an internal soft-start circuit that increases pulse-by-pulse current-limit comparator inverting input voltage slowly after it starts. The typical soft-start time is 5ms. The pulsewidth to the power MOSFET is progressively increased to establish the correct working conditions for transformers, rectifier diodes, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. It also helps prevent transformer saturation and reduces the stress on the secondary diode during startup.

Typical Application Circuit (Netbook Adapter by Flyback)

Application	Fairchild Devices	Input Voltage Range	Output
Netbook Adapter	FAN6862R/L	90~265V_{AC}	19V/2.1A (40W)

Features

- High efficiency (>85.3% at full load) meeting EPS regulation with enough margin
- Low standby (Pin<0.15W at no-load condition)
- Soft-start time: 5ms

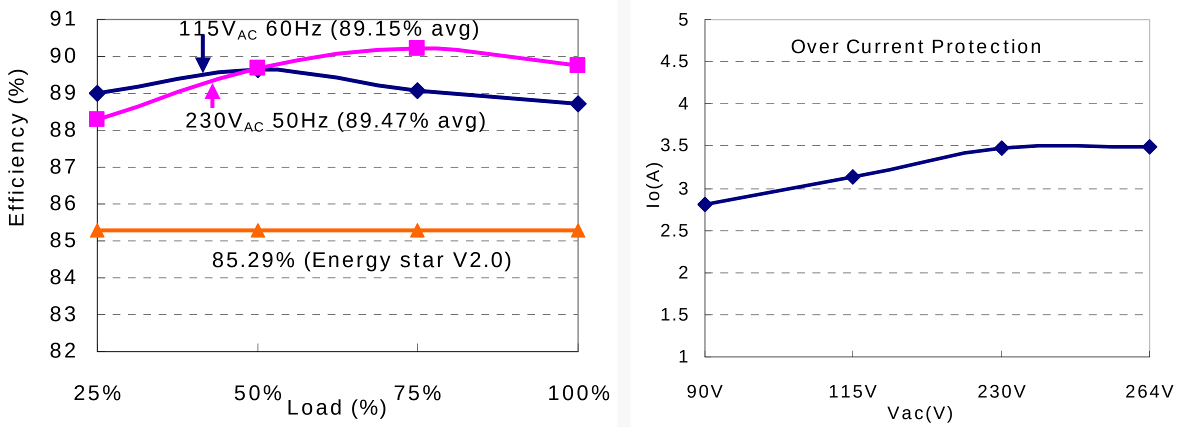

Figure 29. Measured Efficiency and Over-Current Protection

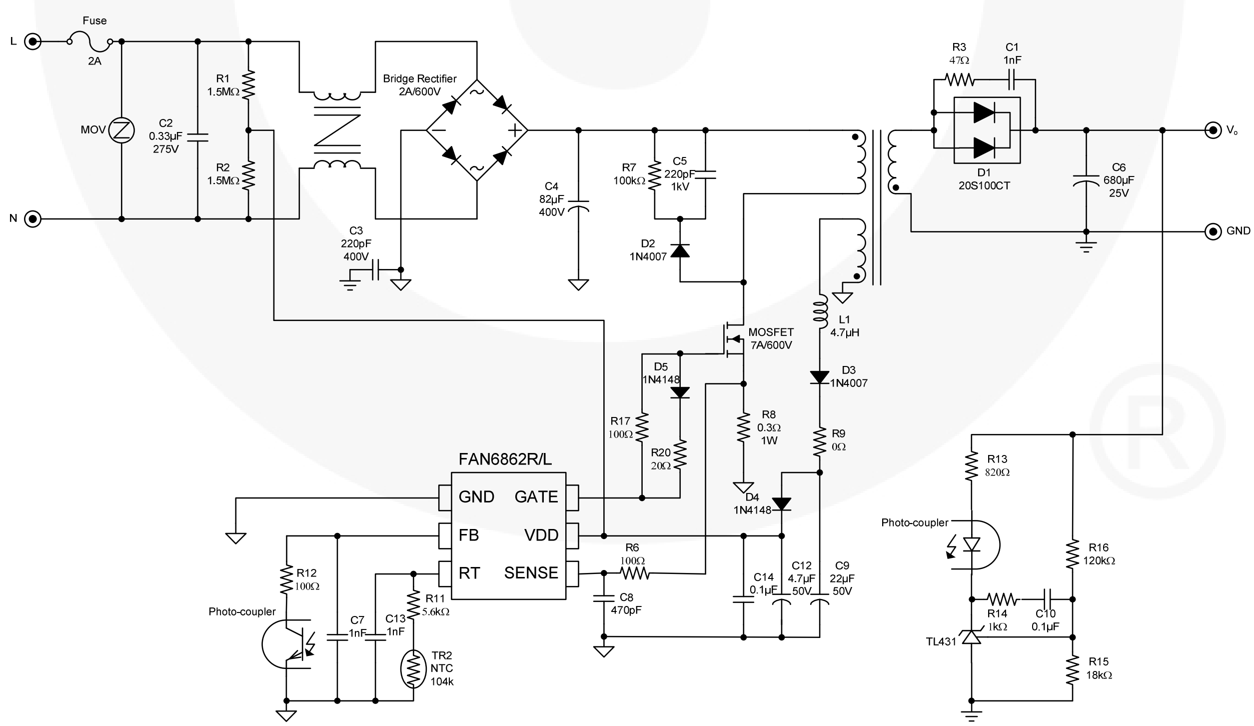

Figure 30. Schematic of Typical Application Circuit

Typical Application Circuit (Continued)

Transformer Specification

- Core: RM 8
- Bobbin: RM 8

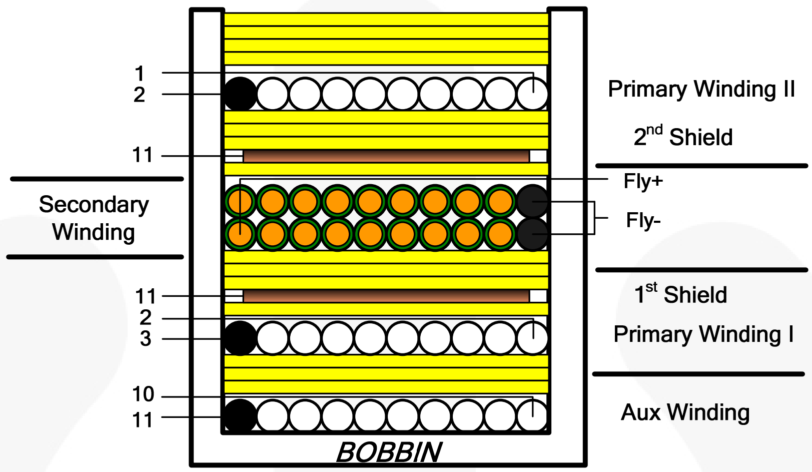

Figure 31. Transformer Diagram

NO	Terminal		WIRE	Ts	INSULATION	BARRIER	
	S	F			Ts	Primary	Secondary
N1	11	10	0.25*1	9	3		
N2	3	2	0.25* 1	33	1		
	11		COPPER SHIELD	1.2	3		
N3	Fly-	Fly+	0.5* 2	12	1		
	11		COPPER SHIELD	1.2	3		
N4	2	1	0.25 * 1	33	4		
			CORE ROUNDING TAPE		3		

	Pin	Specification	Remark
Primary-Side Inductance	3–1	920μH ±5%	100kHz, 1V
Primary-Side Effective Leakage	3–1	15μH Maximum	Short One of the Secondary Windings

Physical Dimensions

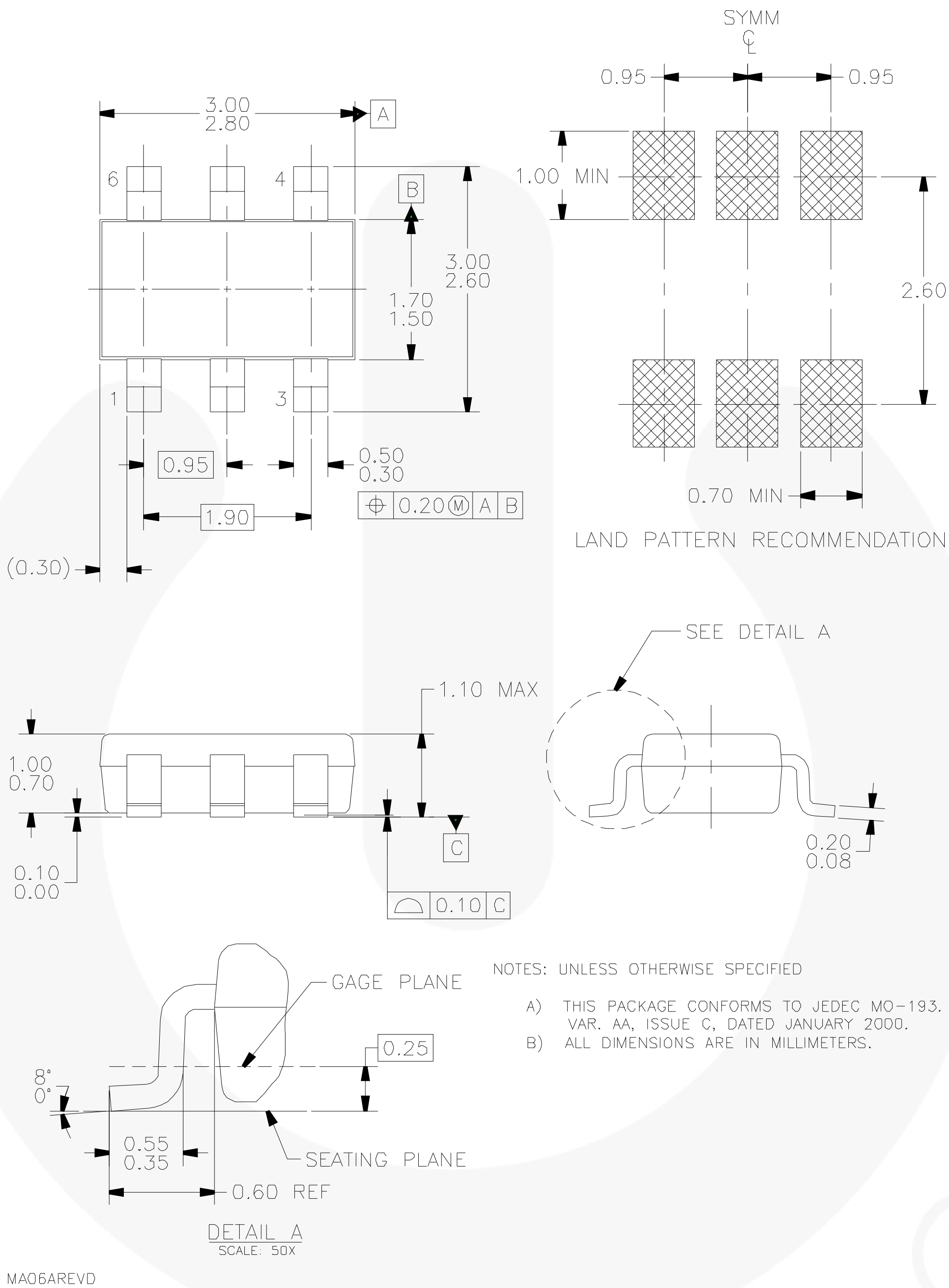

Figure 32. 6-Pin, SUPERSOT6 "SSOT-6", JEDEC MO-193, 1.6mm Wide Package

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