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June 2014

# FDMA430NZ

# Single N-Channel 2.5V Specified PowerTrench® MOSFET

**30V**, **5.0A**, **40m** $\Omega$ 

# **General Description**

This Single N-Channel MOSFET has been designed using Fairchild Semiconductor's advanced Power Trench process to optimize the  $\rm R_{DS}(on)$  @V $_{GS}=2.5V$  on special MicroFET leadframe.

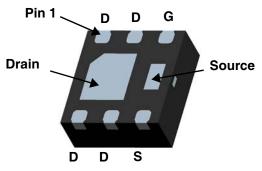
# **Applications**

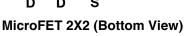
■ Li-Ion Battery Pack



#### **Features**

- $R_{DS(on)} = 40 \text{m}\Omega$  @  $V_{GS} = 4.5 \text{ V}$ ,  $I_D = 5.0 \text{A}$
- $R_{DS(on)} = 50 \text{m}\Omega$  @  $V_{GS} = 2.5 \text{ V}$ ,  $I_D = 4.5 \text{A}$
- Low Profile-0.8mm maximum-in the new package MicroFET 2x2 mm
- HBM ESD protection level > 2.5kV typical (Note 3)
- Free from halogenated compounds and antimony oxides
- RoHS Compliant





# S 4 3 G D 5 D D Bottom Drain Contact

### Absolute Maximum Ratings T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
$V_{DSS}$	Drain-Source Voltage	30	V	
$V_{GSS}$	Gate-Source Voltage	±12	V	
	Drain Current -Continuous	(Note 1a)	5.0	_
'D	-Pulsed		20	_ A
D	Power dissipation (Steady State)	(Note 1a)	2.4	w
$P_{D}$		(Note 1b)	0.9	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range		-55 to +150	°C

#### **Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	52	°C/W
$R_{\theta,JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	145	*C/ <b>VV</b>

# **Package Marking and Ordering Information**

Device Marking	Device	Reel Size	Tape Width	Quantity
430	FDMA430NZ	7"	8 mm	3000 units

Max Units

# **Electrical Characteristics** $T_J = 25^{\circ}\text{C}$ unless otherwise noted

**Parameter** 

Off Characteristics								
B <sub>VDSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0V$ , $I_{D} = 250\mu A$	30			V		
$\frac{\Delta B_{VDSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, Referenced to 25°C		25.2		mV/°C		
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 24V, V_{GS} = 0V,$			1	μΑ		
I <sub>GSS</sub>	Gate-Body Leakage,	$V_{GS} = \pm 12V, \ V_{DS} = 0V$			±10	μΑ		

**Test Conditions** 

Min

#### On Characteristics (Note 2)

Symbol

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	0.6	0.81	1.5	V
$\Delta V_{GS(th)}$ $\Delta T_J$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\mu A$ , Referenced to 25°C		-3.2		mV/°C
D		$V_{GS} = 4.5V, I_D = 5.0A$		23.6	40	
		$V_{GS} = 4.0V, I_D = 5.0A$		23.9	41	mΩ
	Static Drain-Source On-Resistance	$V_{GS} = 3.1V, I_D = 4.5A$		25.4	43	
R <sub>DS(ON)</sub>	Statio Brain Godioe Cit Hesistande	$V_{GS} = 2.5V, I_D = 4.5A$		27.6	50	11152
		$V_{GS} = 4.5V$ , $I_{D} = 5.0A$ , $T_{J} = 150$ °C		37.0	61	
9 <sub>FS</sub>	Forward Transconductance	$V_{DS} = 5V, I_{D} = 5.0A$		25.6		S

#### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	$V_{DS} = 10V, V_{GS} = 0V,$	600	800	pF
C <sub>oss</sub>	Output Capacitance	f = 1.0MHz	110	150	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		75	115	pF
$R_G$	Gate Resistance	f = 1.0MHz	3.5		Ω

#### Switching Characteristics (Note 2)

t <sub>d(on)</sub>	Turn-On Delay Time		8.3	17	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{DD} = 10V$ , $I_D = 1A$	7.1	15	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{GS} = 4.5V$ , $R_{GEN} = 6\Omega$	18.1	37	ns
t <sub>f</sub>	Turn-Off Fall Time		6.0	12	ns
$Q_g$	Total Gate Charge	101/ 1 5 04	7.3	11	nC
$Q_{gs}$	Gate-Source Charge	$V_{DS} = 10V, I_{D} = 5.0A,$ $V_{GS} = 4.5V$	0.8	2	nC
$Q_{gd}$	Gate-Drain Charge	VGS - 4.5 V	1.9	3	nC

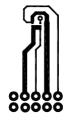
#### **Drain-Source Diode Characteristics and Maximum Ratings**

I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				2.0	Α
$V_{SD}$	Drain-Source Diode Forward Voltage V <sub>GS</sub> = 0V, I <sub>S</sub> = 2.0A			0.69	1.2	V
t <sub>rr</sub>	Diode Reverse Recovery Time	I <sub>F</sub> = 5.0A,			17	ns
Q <sub>rr</sub>	Diode Reverse Recovery Charge	de Reverse Recovery Charge di/dt = 100A/μs			5	nC

Notes: 1.  $R_{0JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.



a. 52 °C/W when mounted on a 1 in² pad of 2 oz copper.



b. 145 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width <  $300~\mu s$ , Duty Cycle < 2.0%3. The diode connected between the gate and the source serves only as proection against ESD. No gate overvoltage rating is implied.

### Typical Characteristics T<sub>J</sub> = 25°C unless otherwise noted

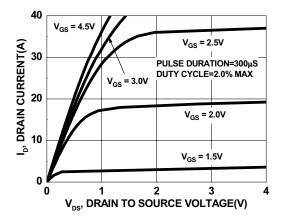


Figure 1. On Region Characteristics

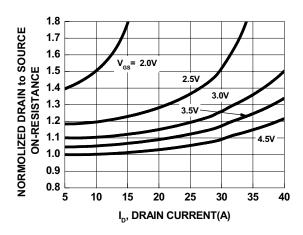


Figure 2. On-Resistance vs Drain Current and Gate Voltage

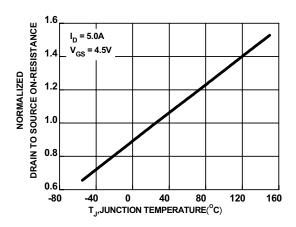


Figure 3. Normalized On Resistance vs Junction Temperature

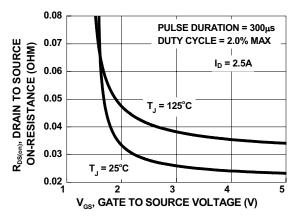


Figure 4. On-Resistance vs Gate to Source Votlage

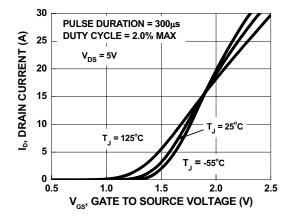


Figure 5. Transfer Characteristics

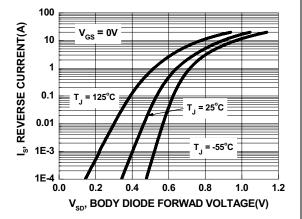
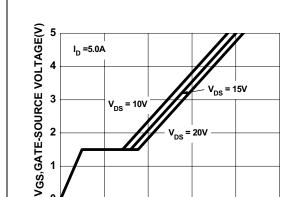


Figure 6. Source to Drain Diode Forward Voltage vs Source Current



Typical Characteristics T<sub>J</sub> = 25°C unless otherwise noted

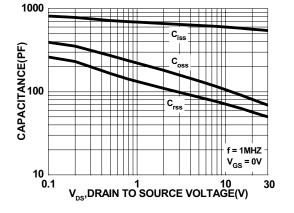
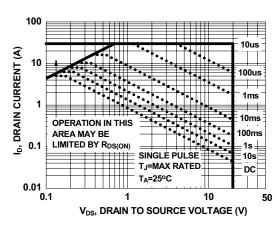


Figure 7. Gate Charge Characteristics

 $\begin{array}{c} 4 & 6 \\ \text{Qg,GATE CHARGE (nC)} \end{array}$ 

Figure 8. Capacitance vs Drain to Source Voltage



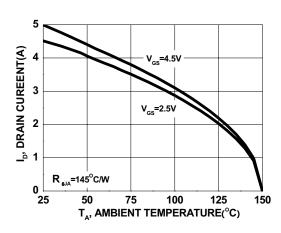
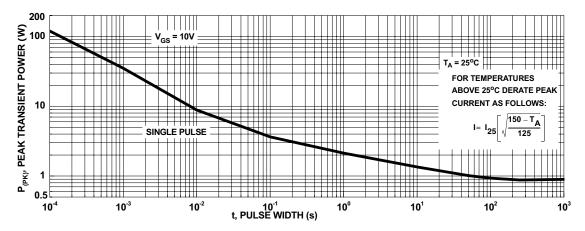


Figure 9. Safe Operating Area

Figure 10. Maximum Continuous Drain Current vs
Ambient Temperature



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Figure 11. Single Pulse Maximum Power Dissipation

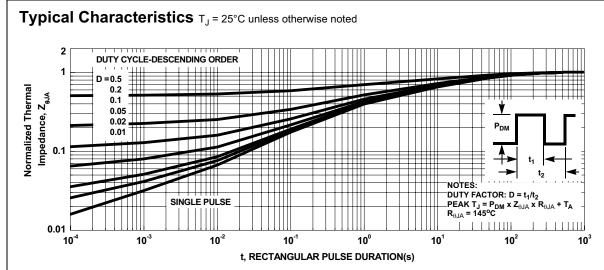
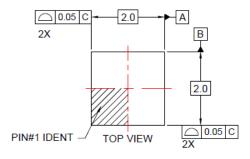
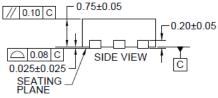
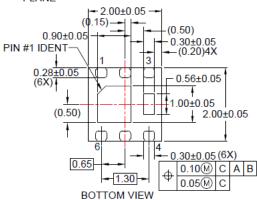


Figure 12. Transient Thermal Response Curve

## **Dimensional Outline and Pad Layout**

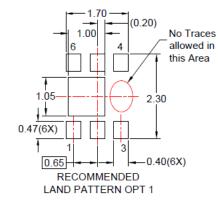


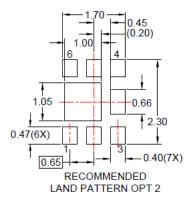




#### NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC MO-229 REGISTRATION
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- E. DRAWING FILENAME: MKT-MLP06Lrev4.







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