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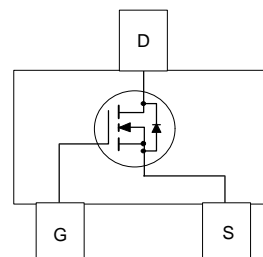
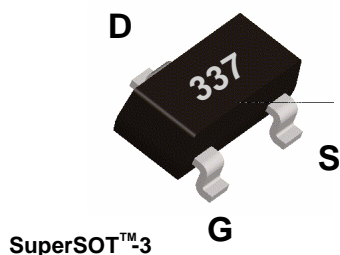
## FDN337N N-Channel Logic Level Enhancement Mode Field Effect Transistor

### General Description

SuperSOT™-3 N-Channel logic level enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications in notebook computers, portable phones, PCMCIA cards, and other battery powered circuits where fast switching, and low in-line power loss are needed in a very small outline surface mount package.

### Features

- 2.2 A, 30 V,  $R_{DS(ON)} = 0.065 \Omega @ V_{GS} = 4.5 \text{ V}$   
 $R_{DS(ON)} = 0.082 \Omega @ V_{GS} = 2.5 \text{ V}$ .
- Industry standard outline SOT-23 surface mount package using proprietary SuperSOT™-3 design for superior thermal and electrical capabilities.
- High density cell design for extremely low  $R_{DS(ON)}$ .
- Exceptional on-resistance and maximum DC current capability.



### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FDN337N	Units
$V_{DSS}$	Drain-Source Voltage	30	V
$V_{GSS}$	Gate-Source Voltage - Continuous	$\pm 8$	V
$I_D$	Drain/Output Current - Continuous - Pulsed	2.2	A
		10	
$P_D$	Maximum Power Dissipation (Note 1a) (Note 1b)	0.5	W
		0.46	
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	250	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	75	$^\circ\text{C/W}$

## Electrical Characteristics ( $T_A = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to $25\text{ }^\circ\text{C}$		41		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
			$T_J = 55\text{ }^\circ\text{C}$			10
$I_{GSSF}$	Gate - Body Leakage, Forward	$V_{GS} = 8\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate - Body Leakage, Reverse	$V_{GS} = -8\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
<b>ON CHARACTERISTICS</b> (Note)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.4	0.7	1	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to $25\text{ }^\circ\text{C}$		-2.3		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 4.5\text{ V}, I_D = 2.2\text{ A}$		0.054	0.065	$\Omega$
			$T_J = 125\text{ }^\circ\text{C}$		0.08	
		$V_{GS} = 2.5\text{ V}, I_D = 2\text{ A}$		0.07	0.082	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$	10			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 2.2\text{ A}$		13		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		300		pF
$C_{oss}$	Output Capacitance			145		pF
$C_{rss}$	Reverse Transfer Capacitance			35		pF
<b>SWITCHING CHARACTERISTICS</b> (Note)						
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = 5\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 4.5\text{ V}, R_{GEN} = 6\text{ }\Omega$		4	10	ns
$t_r$	Turn - On Rise Time			10	18	ns
$t_{D(off)}$	Turn - Off Delay Time			17	28	ns
$t_f$	Turn - Off Fall Time			4	10	ns
$Q_g$	Total Gate Charge		$V_{DS} = 10\text{ V}, I_D = 2.2\text{ A},$ $V_{GS} = 4.5\text{ V}$		7	9
$Q_{gs}$	Gate-Source Charge			1.1		nC
$Q_{gd}$	Gate-Drain Charge			1.9		nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
$I_S$	Maximum Continuous Drain-Source Diode Forward Current				0.42	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 0.42\text{ A}$ (Note)		0.65	1.2	V

Note:

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.

Typical  $R_{\theta JA}$  using the board layouts shown below on FR-4 PCB in a still air environment :

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .



a.  $250\text{ }^\circ\text{C/W}$  when mounted on  $0.02\text{ in}^2$  pad of 2oz Cu.



a.  $270\text{ }^\circ\text{C/W}$  when mounted on  $0.001\text{ in}^2$  pad of 2oz Cu.

## Typical Electrical Characteristics

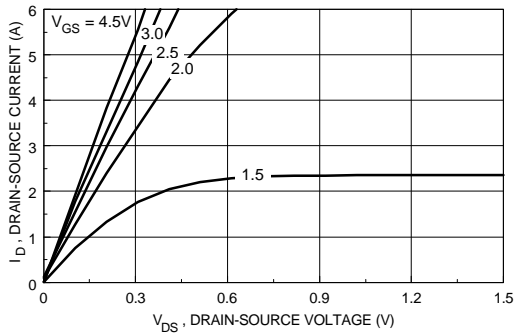


Figure 1. On-Region Characteristics.

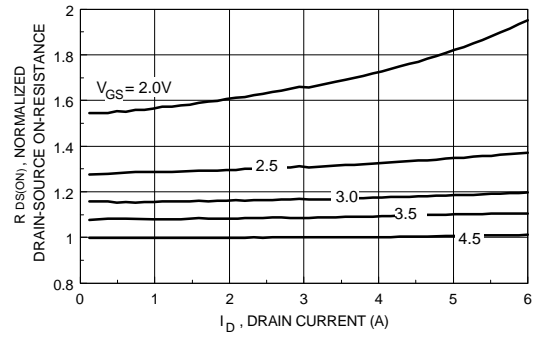


Figure 2. On-Resistance Variation with Drain Current and Gate

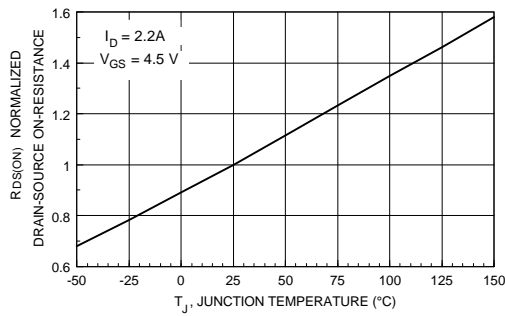


Figure 3. On-Resistance Variation with Temperature.

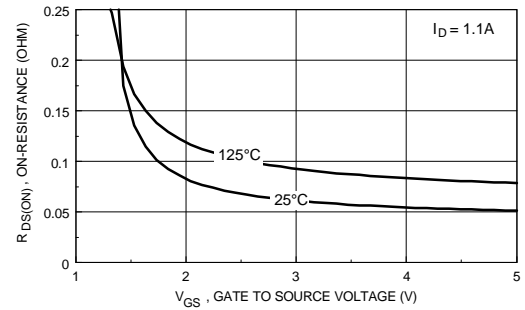


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

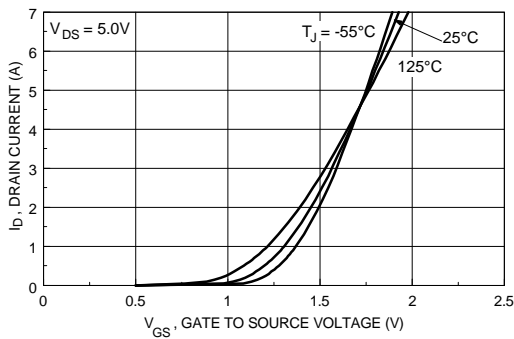
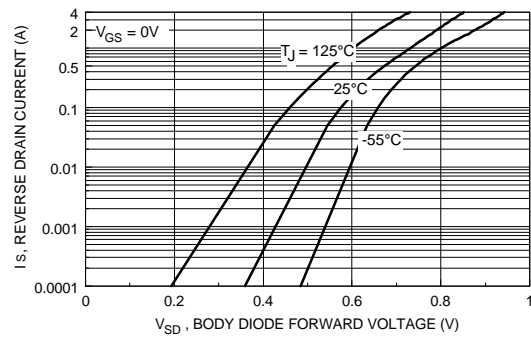


Figure 5. Transfer Characteristics.



## Typical Electrical Characteristics (continued)

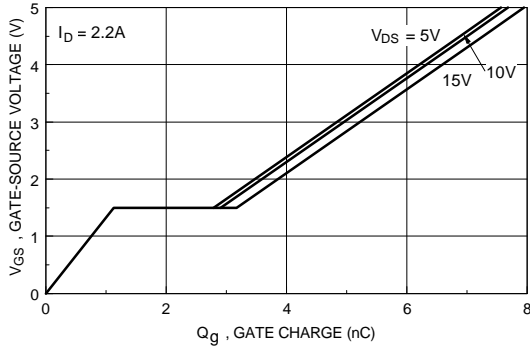


Figure 7. Gate Charge Characteristics.

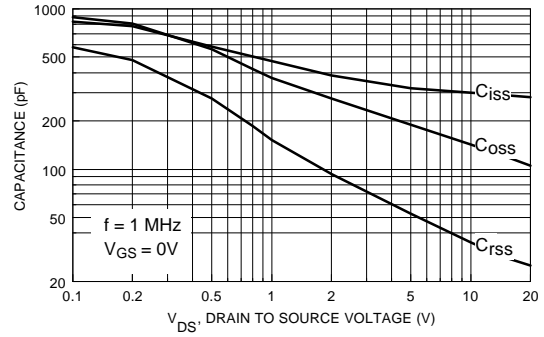


Figure 8. Capacitance Characteristics.

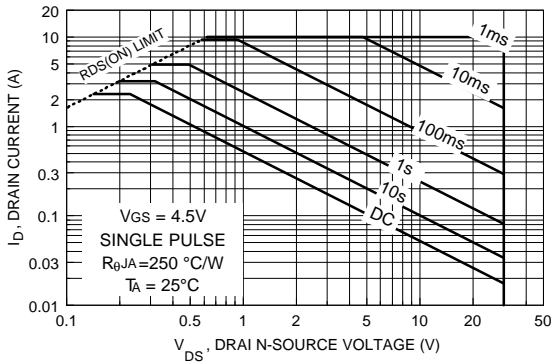


Figure 9. Maximum Safe Operating Area.

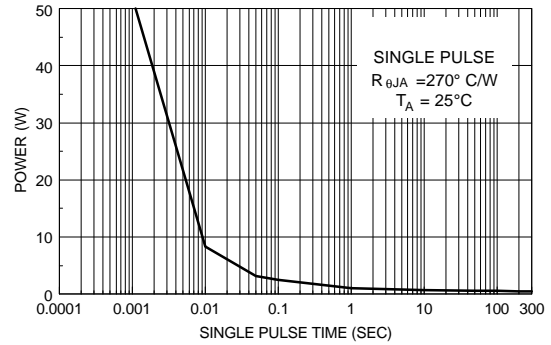


Figure 10. Single Pulse Maximum Power Dissipation.

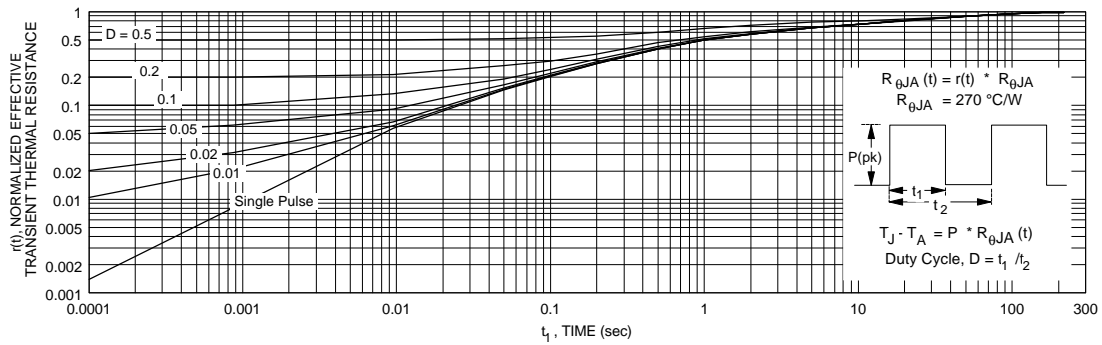


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in note 1b.  
Transient thermal response will change depending on the circuit board design.

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